Upgrade of the ATLAS Tile calorimeter electronics

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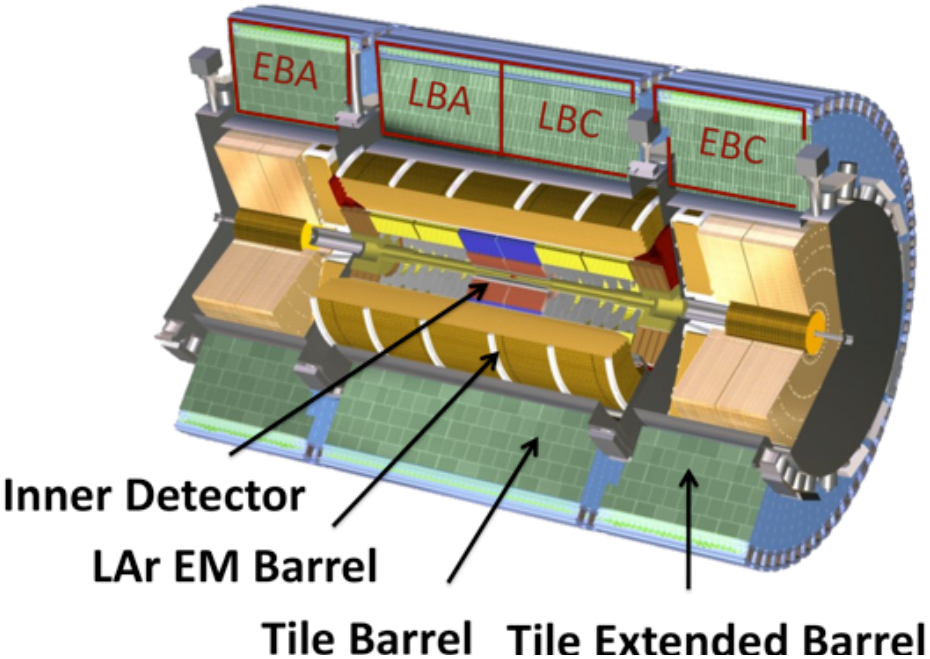
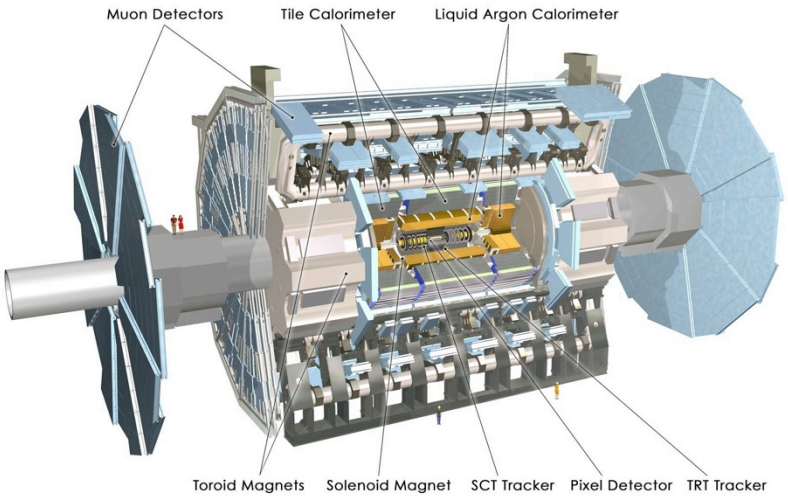
The ATLAS Tile calorimeter

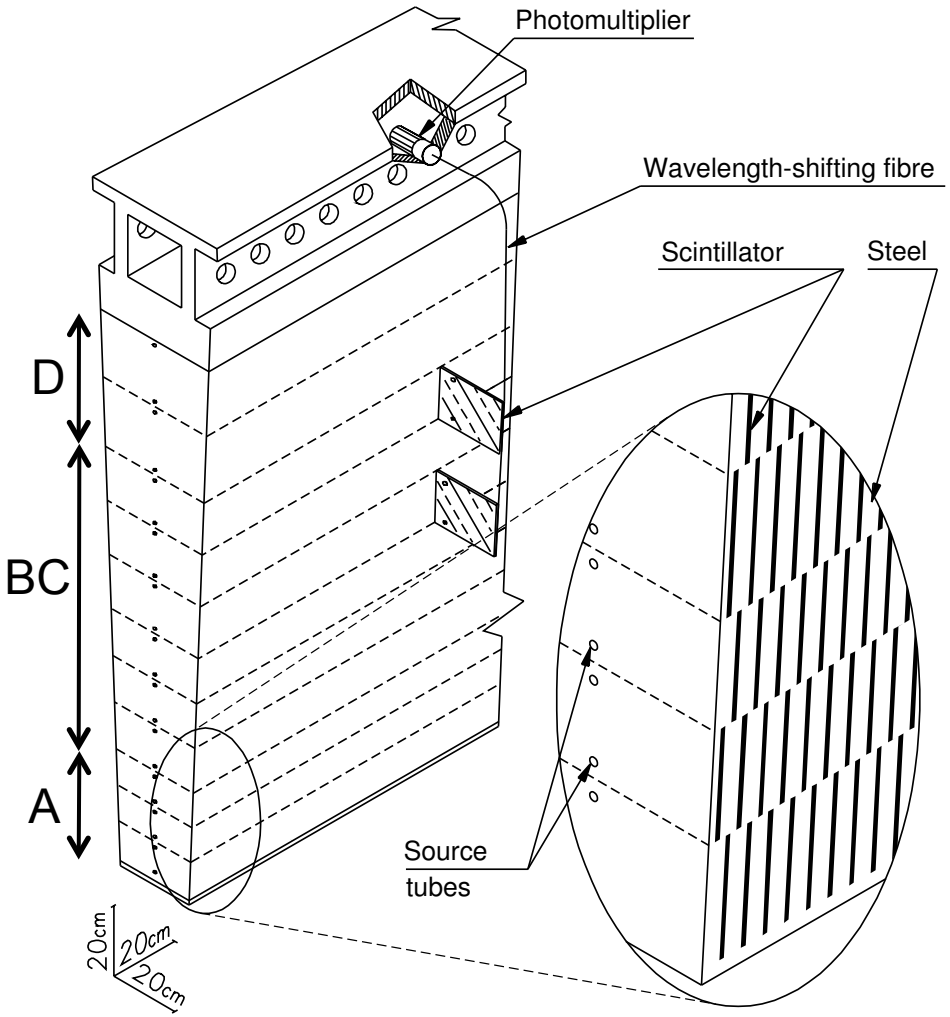
- The hadronic Tile calorimeter is a hollow cylinder that covers the range $|\eta| < 1.7$
  - Mechanically divided into three barrels and staggered in ϕ is the central structure of ATLAS and weighs 2900 tons
- Based on a sampling technique where plastic scintillating tiles are embedded in a steel absorber plates
  - Each tile is read-out on both sides by wavelength shifting (WLS) fibers
  - Groups of tiles are bundled together into cells, each of them is read-out by two photo-multiplier tubes (PMTs).
  - Front-end electronics and pipeline memories are located in the outer most region of the modules.





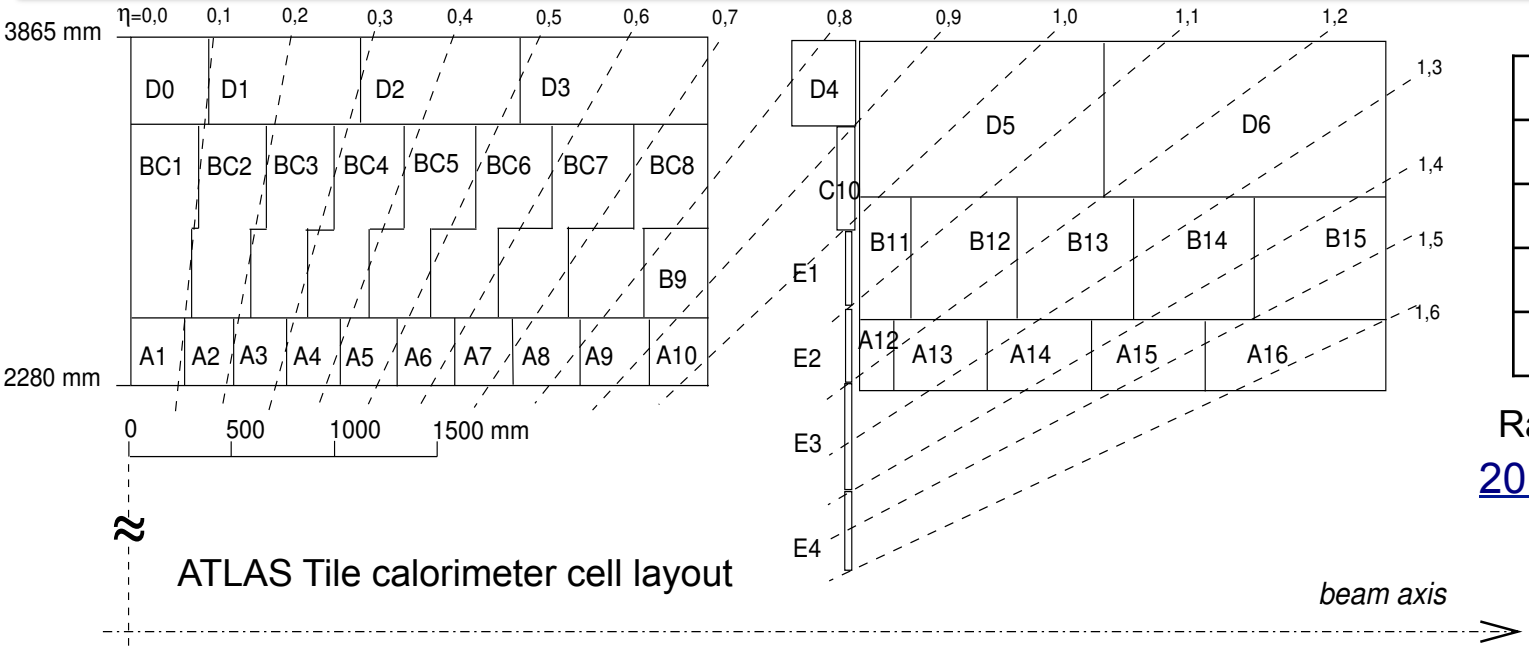
Note in ATLAS: $\eta = -log\,(tan(\theta/2))$

Tile modules



- Each barrel is divided into 64 modules providing a ϕ granularity of 0.1 rad
- Tiles are trapezoidal shaped scintillators which are placed in the gaps of the module, perpendicular to the beam direction
  - Eleven rows of tiles are used for each module
  - Two calibration source tubes cross each row
- Each tile is read-out on both sides by wavelength shifting fibers WLS that are coupled to the tiles along the external faces of the module
  - Read-out electronics are located in the outermost region of the module

Cell layout



ATLAS Tile calorimeter cell layout

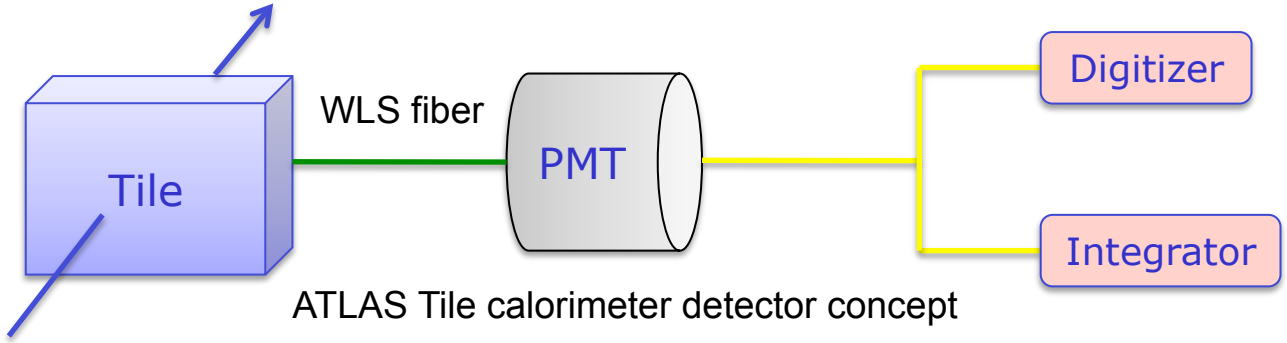
Layers	Size [mm]
10-11	187
7-9	147
4-6	127
1-3	97

Radial size of tile rows

2013 *JINST* **8** P01005

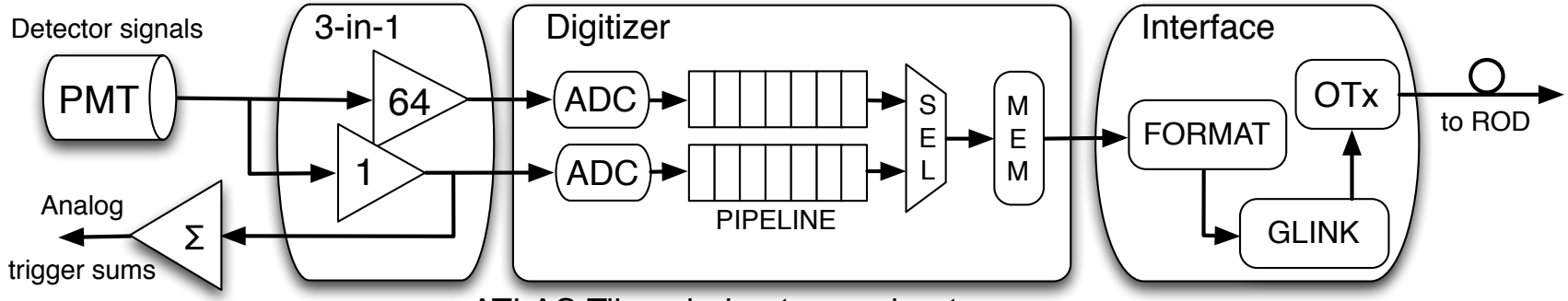
- Groups of tiles are bundled together into cells and read out by photo-multipliers tubes (PMTs)
- Cells are laid out in order to have a projective geometry around the interaction point in steps of $\Delta\eta = 0.1$
- Tile is made out of 5182 cells of three types A (1.5λ), BC (4.1λ) and D (1.8λ)

Detector concept



ATLAS Tile calorimeter detector concept

- The Tile calorimeter is based on a simple detector concept
  1. Scintillation light is produced in the tile
  2. Light is collected by 2 WLS fibers (1 cell is read out by 2 PMTs)
  3. Electrical pulse produced by the photo-multiplier (9852 in total)
  4. Signal is sampled (and also integrated)
- Samples are stored in pipeline memories located in the front-end electronics and transferred to back-end electronics on reception of a L1A signal



ATLAS Tile calorimeter read-out

Signal reconstruction

- The signal reconstruction in Tile is based on the Optimal Filtering
  - Amplitude and time are obtained through a linear combination of the digital samples
  - Weights are obtained from the signal pulse shape and the correlation matrix between the samples for an expected time of the pulse

$$A = \sum_{i=1}^{7} a_i S_i \quad \tau = \frac{1}{A} \sum_{i=1}^{7} b_i S_i$$

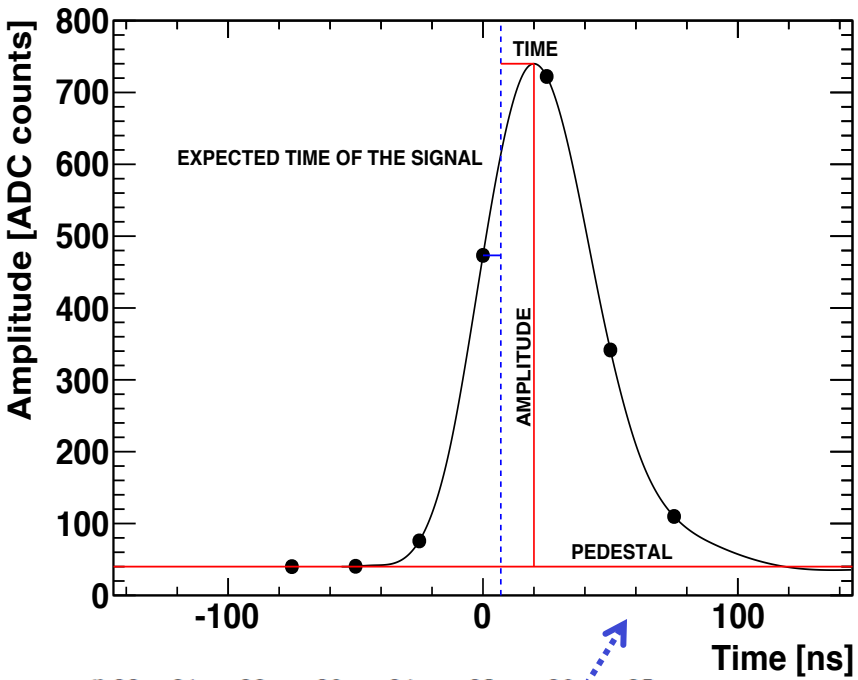
- Energy is proportional to the amplitude

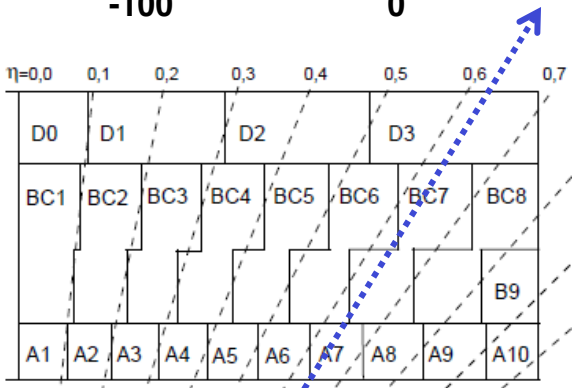
$$E_{PMT} \propto A$$

- Cell energy is the sum of the two PMTs

$$E_{cell} = E_{PMT1} + E_{PMT2}$$

- Fast and reliable for deterministic pulses.
  - Alternative reconstruction methods are under evaluation



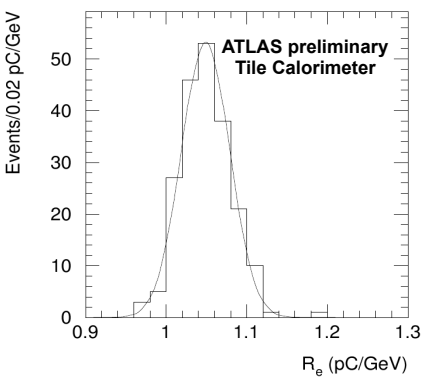


Signal deposits from particles originated in the IP should have reconstructed time equal to zero

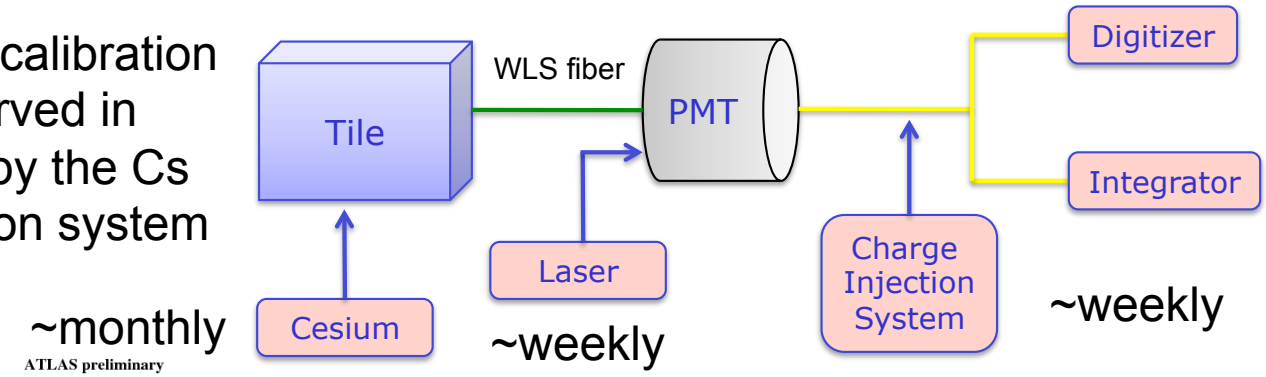
Energy calibration in Tile

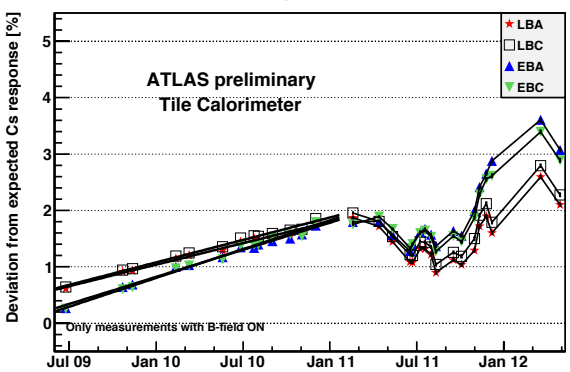
$$E_{PMT} = C_{pC \to MeV} \cdot \varepsilon_{Cs} \cdot \varepsilon_{Laser} \cdot C_{ADC \to pC} \cdot A$$

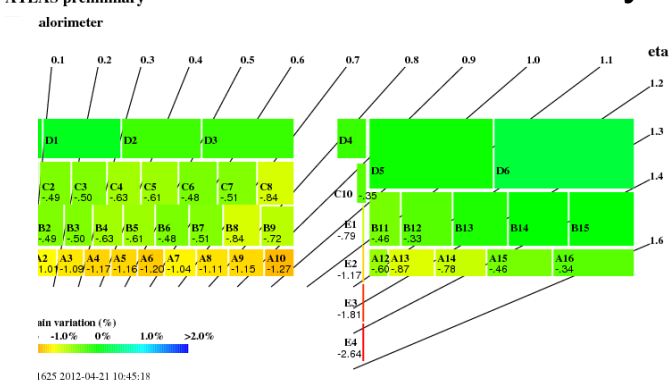
- Half cell energy
- EM constant
- Cesium equalization
- Laser equalization
- Charge Injection System
- Reconstructed amplitude

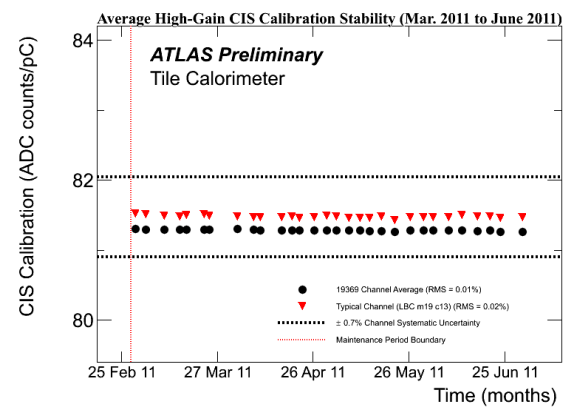


Tile EM calibration is preserved in ATLAS by the Cs calibration system



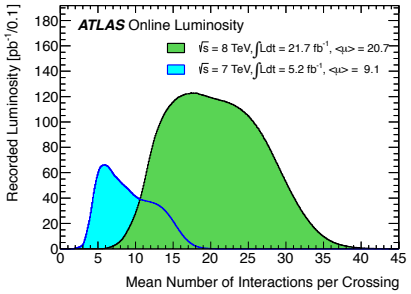


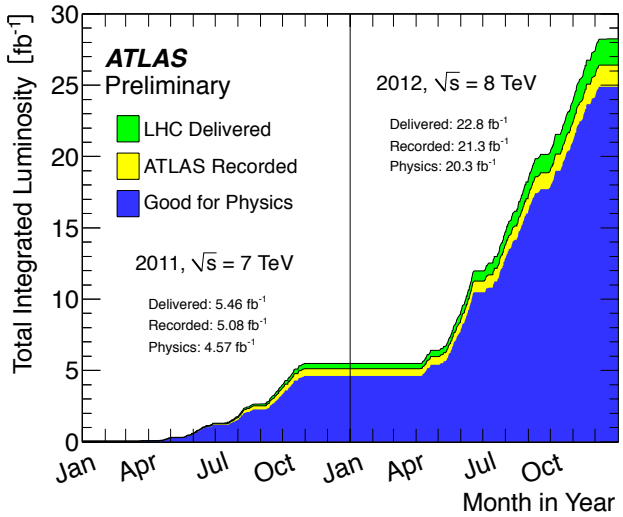


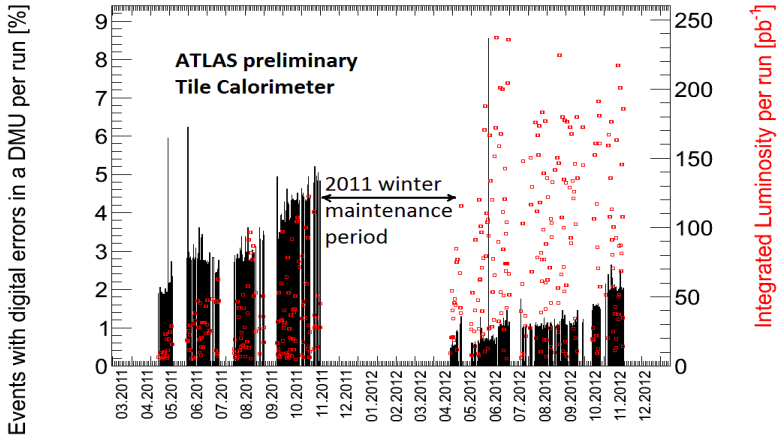


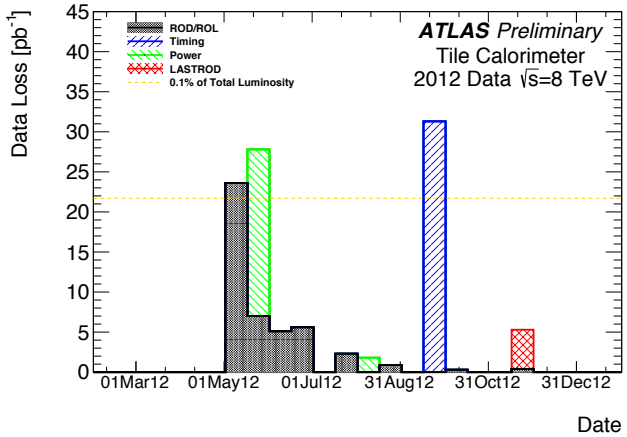
Tile operation summary in Run 1

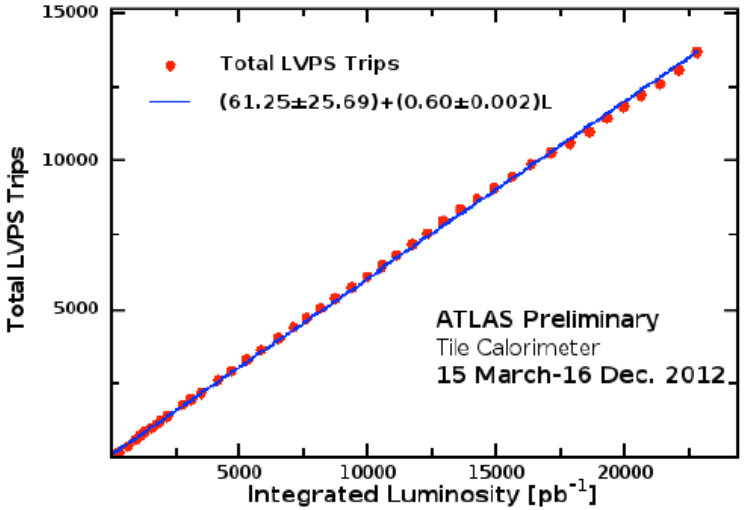
ATLAS Tile has been easy to operate in Run 1, despite...

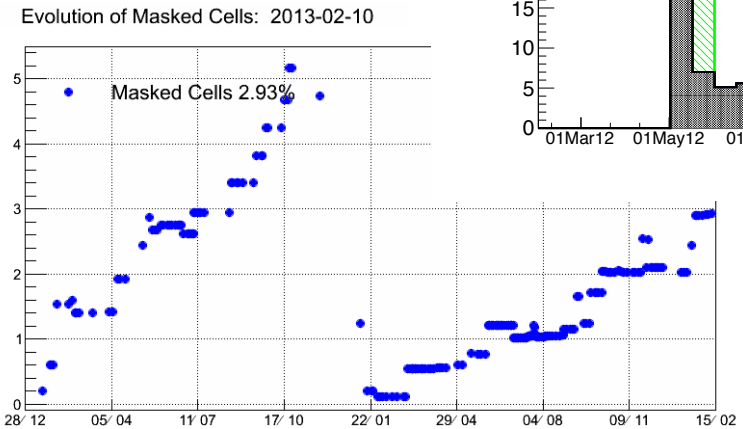






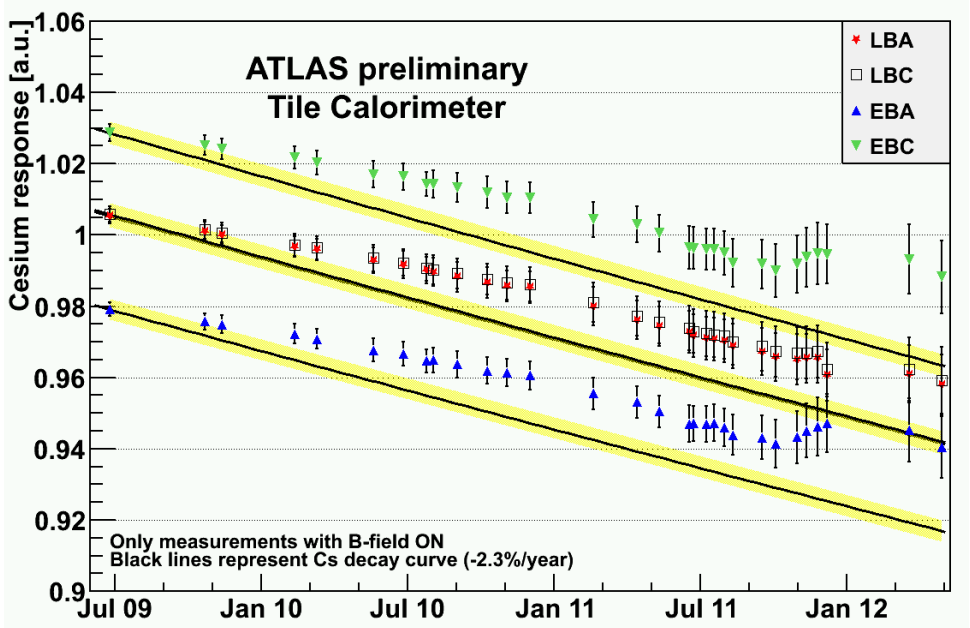


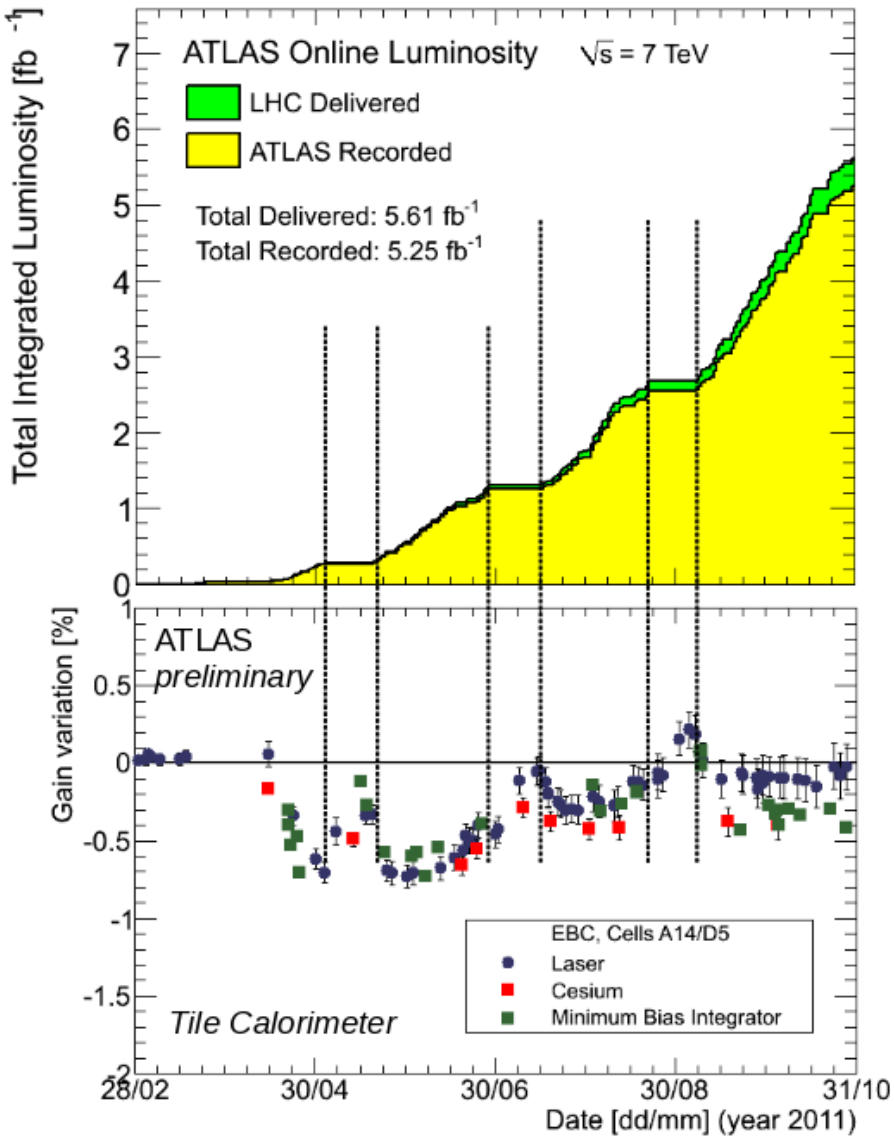




Response calibration in 2011

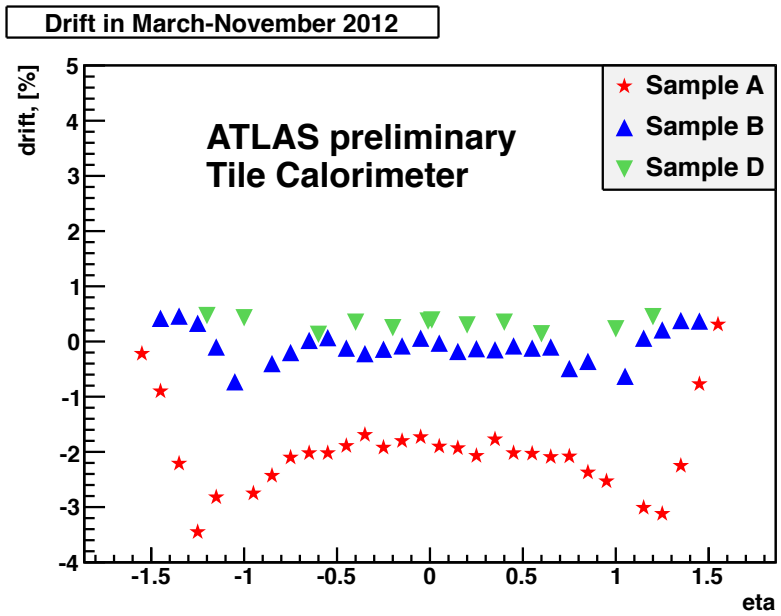
- 2010: up drift of Cs response (~1%)
- 2011: Up/Down drift oscillation (<1%) during beam/no beam periods
  - Consistent behaviour seen by all three calibration systems
  - Drift dominated by PMT gain effects
  - Corrections applied to the PMT response to compensate this effect

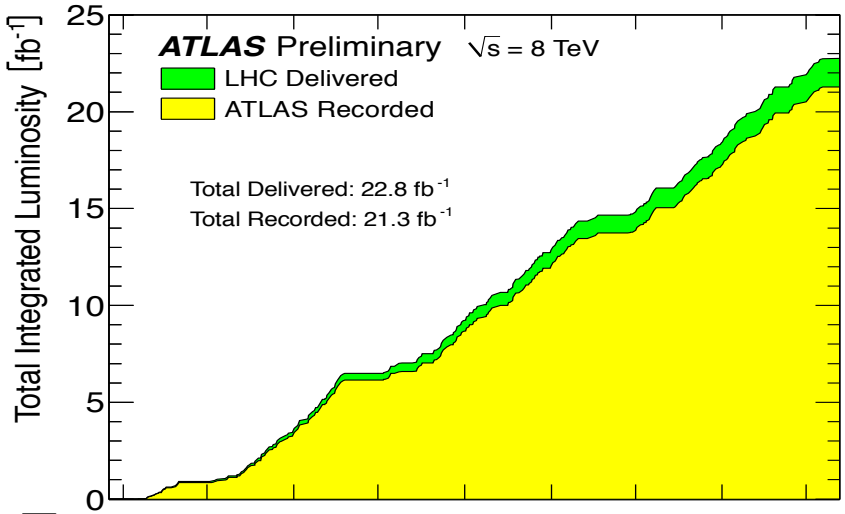


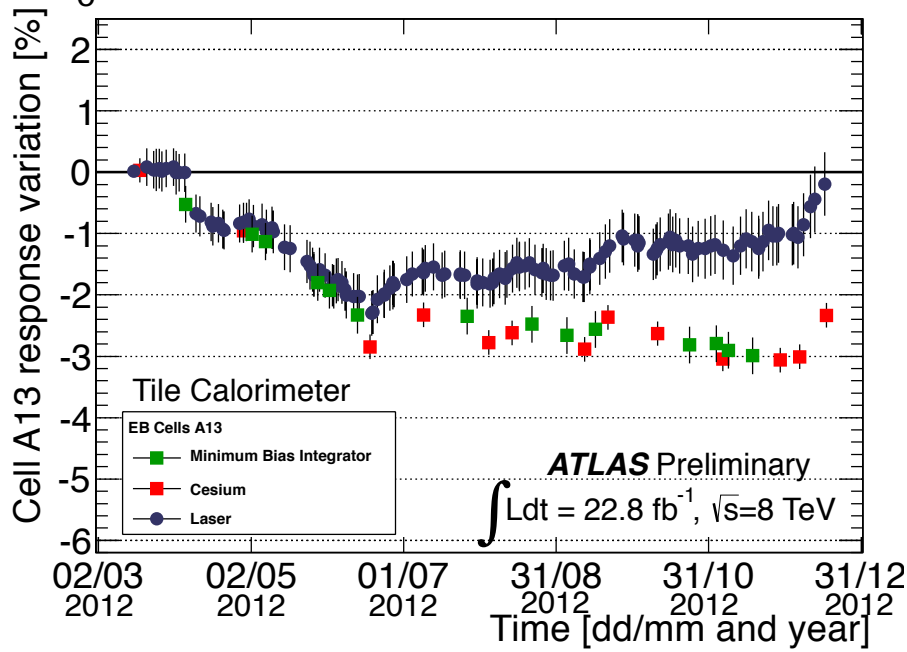


Response calibration in 2012

- Tile response was very stable, maximum drift was ~3.5% for A13 cell, inner most layer at |η|~1.3 in 2012 proton-proton run
  - Estimated ~50% PMT gain down-drift ~50% scintillator damage
- Up and down drifts follow data-taking and machine development periods
  - Recovery started after proton period ended
- Observed 2/3 of the total damage in 4 months after run start
  - Applied weekly calibration to PMT response

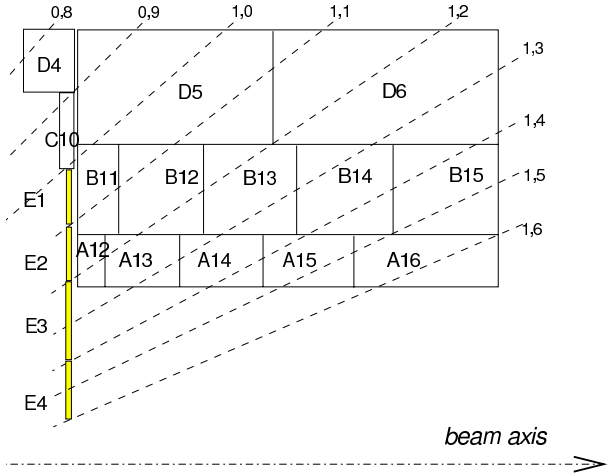


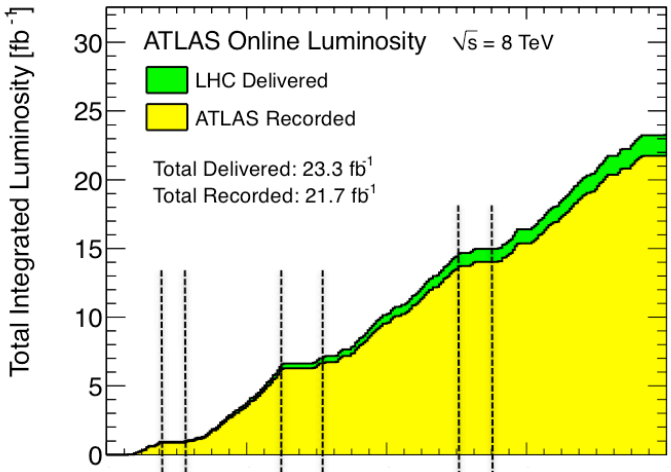


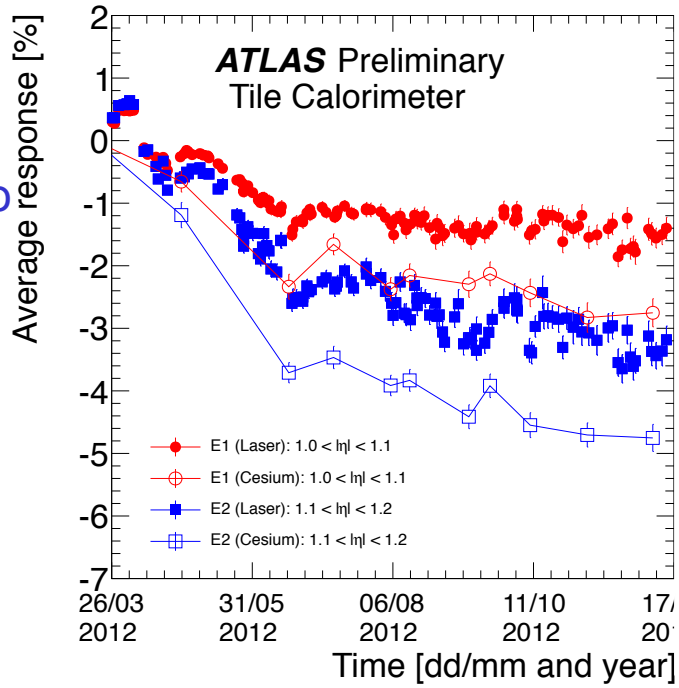


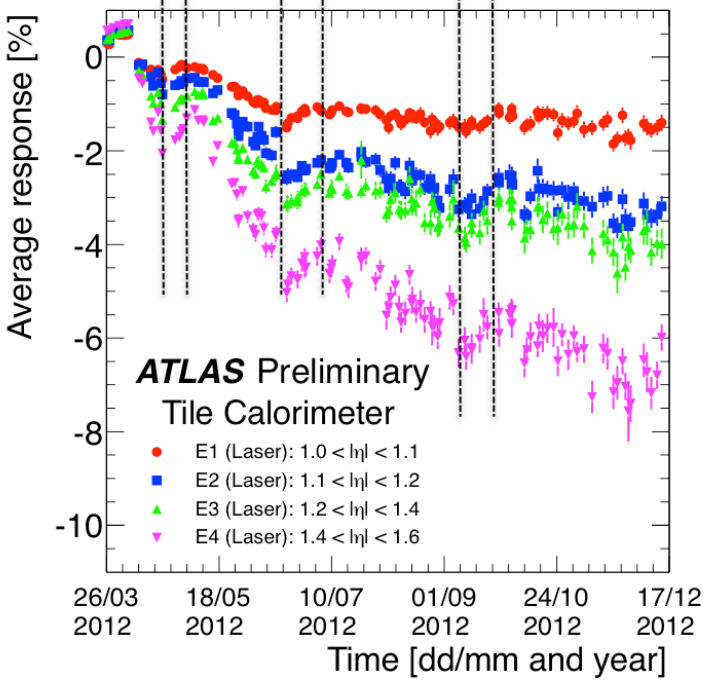
Most irradiated cells

- Gap/crack scintillators (E cells), located in 1.0 < η < 1.6 are the most irradiated cells in Tile
- Up to 6% down-drift was observed for E4 cell with Laser calibration
  - E3 and E4 cells don't have Cs calibration
- In E1 cells, ~50% down-drift was due to PMT drift
- In E2 cells, PMT drift was responsible for ¾ of the gain variation
- Expect additional 1-2% in E3, E4 cells



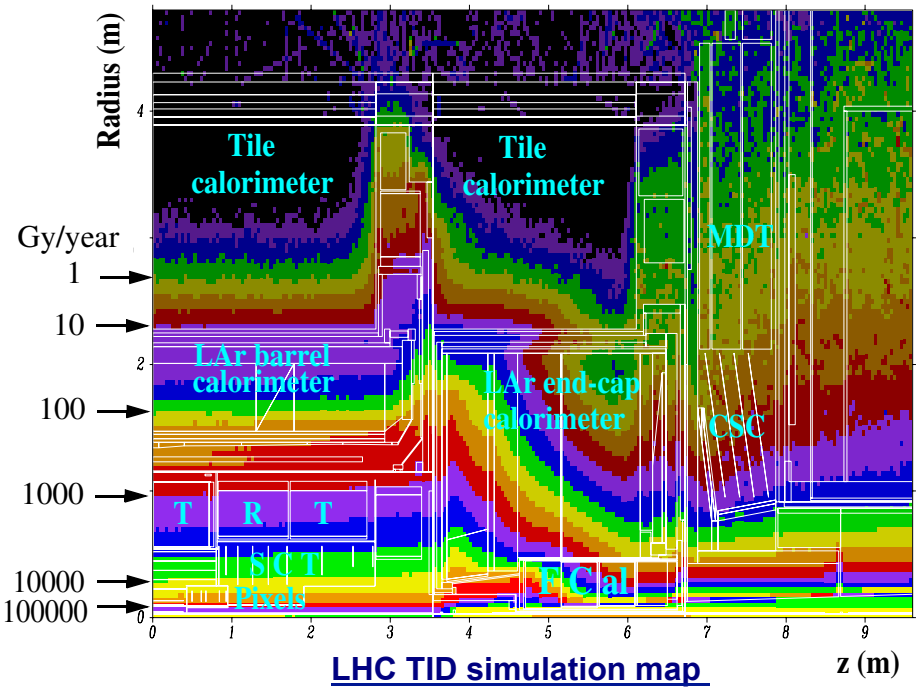






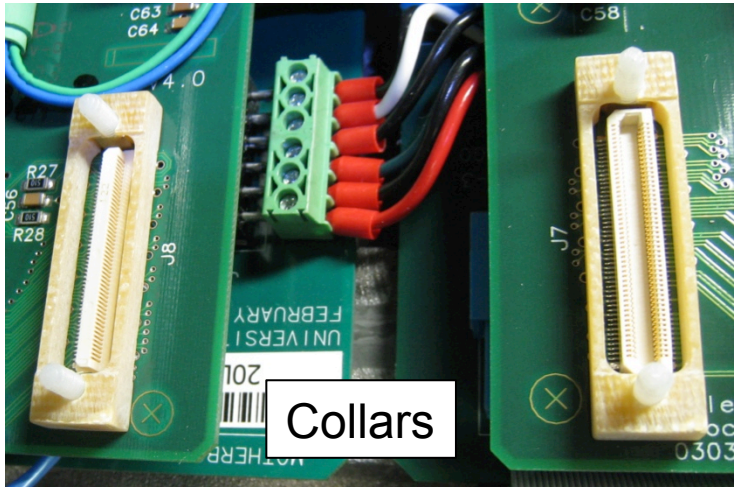
Upgrade of the Tile calorimeter

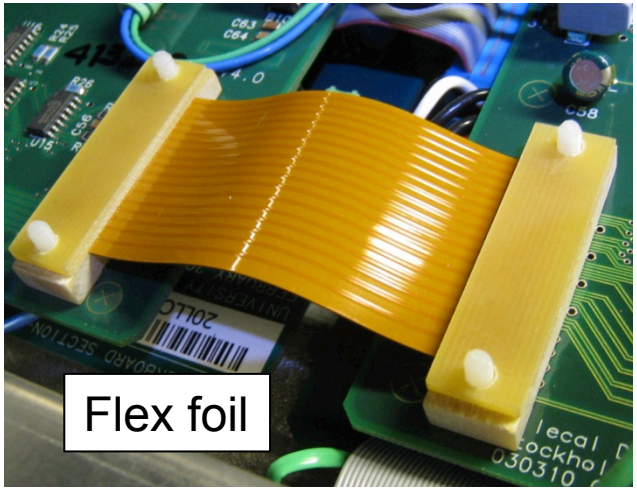
- During the LHC run 1, the performance of Tile calorimeter has been outstanding
  - The PMT and scintillator response drifts are well measured and compensated
  - Radiation damage only on most exposed scintillators (Gap/Crack and MBTS)
- Phase - 0 upgrade (2015)
  - Refurbishment of on-detector readout electronics
  - New low voltage power supplies
  - Replacement of laser system
  - Improvement of Cesium system
- Phase - I upgrade (2019)
  - D-Layer muon trigger
  - Replacement of gap and crack scintillators
- Phase - II upgrade (~2024)
  - Major upgrade of on- and off-detector electronics
  - New active HV dividers for the PMTs

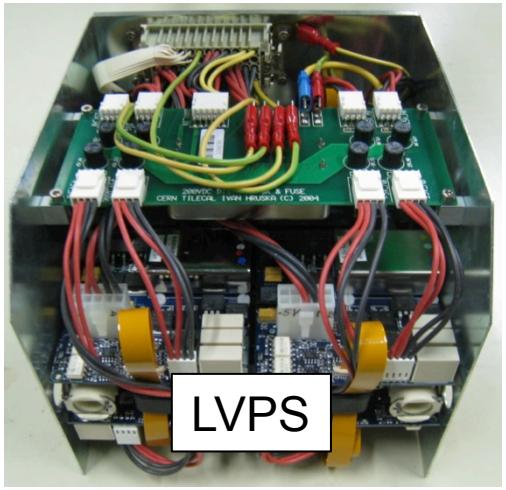


LHC TID simulation map

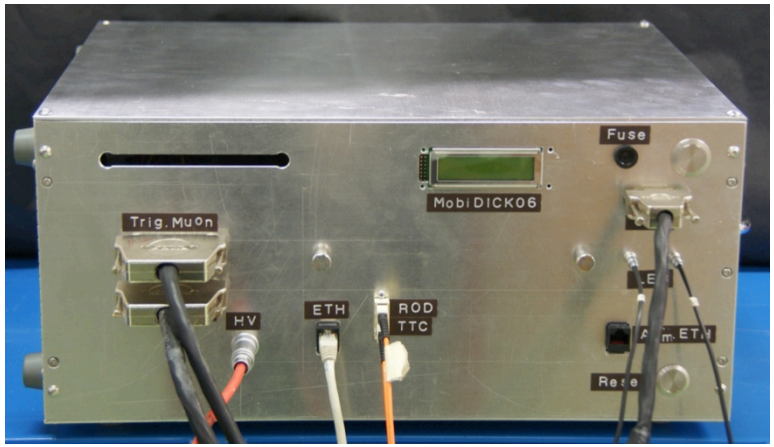
Phase-0 upgrade



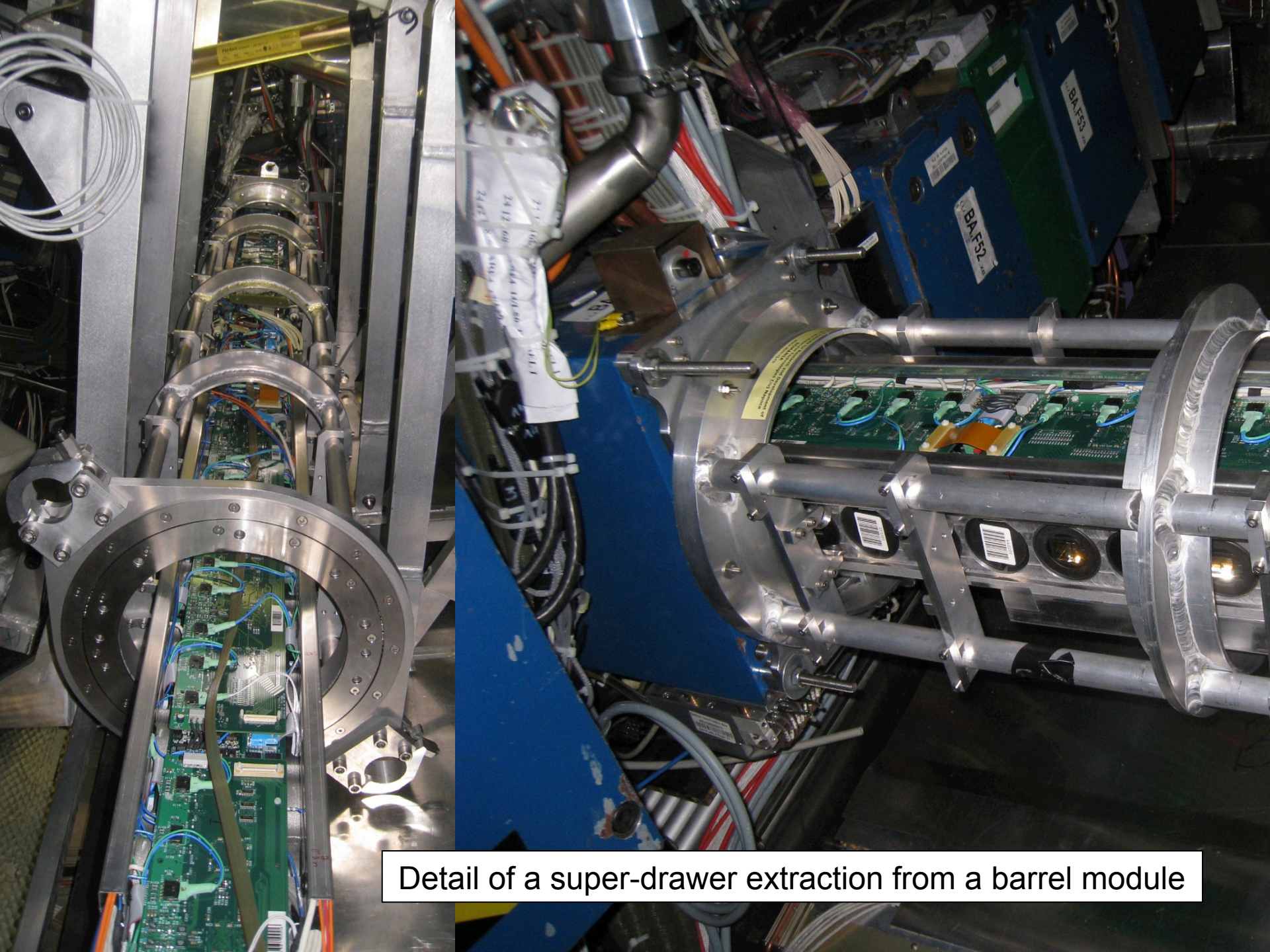




- The upgrade of the Tile calorimeter during LS1 (Phase-0) is to consolidate the front-end electronics
  - Finger low voltage power supply replacement
  - Flex foil replacement and addition of collars in connectors
  - Access to all 256 modules is mandatory
- In-situ QA is assessed on the modules with the MobiDICK system
  - Recently upgraded to extend lifetime and provide more precision measurements

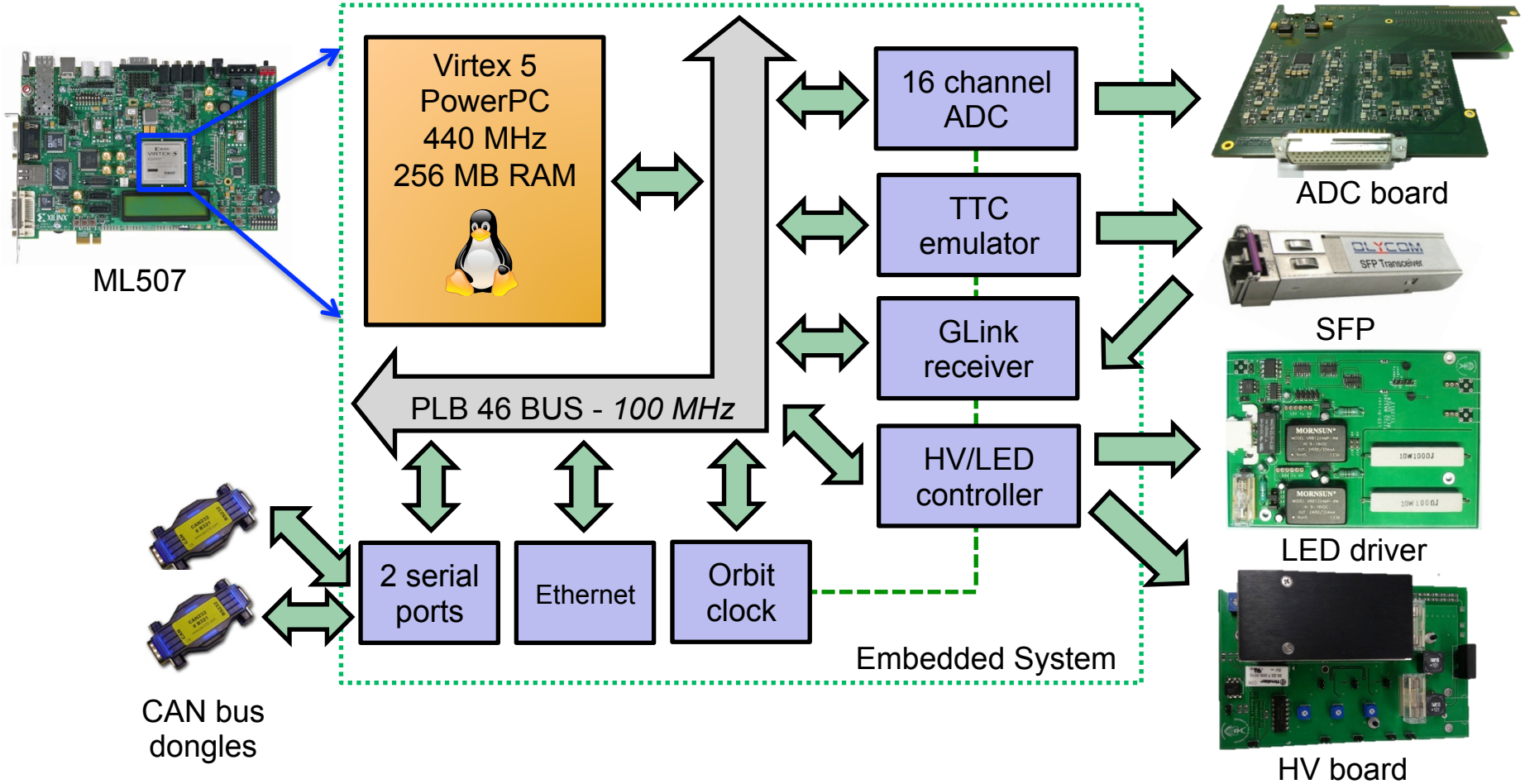


MobiDICK



Detail of a super-drawer extraction from a barrel module

A Mobile Data Integrity Check system



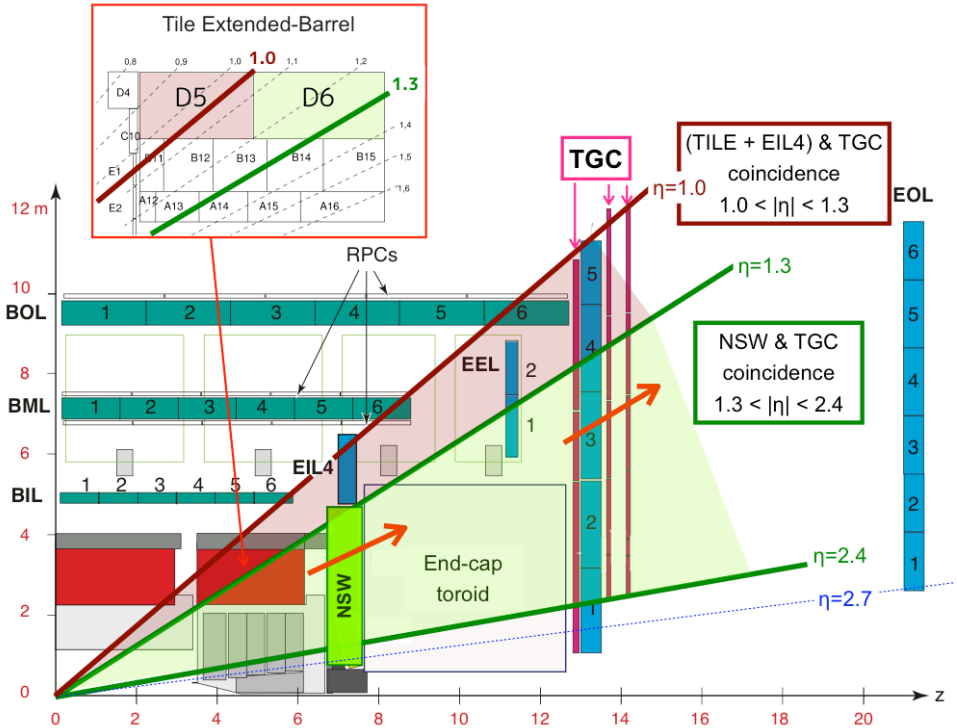
- Embedded OS controls custom hardware boards through dedicated firmware modules

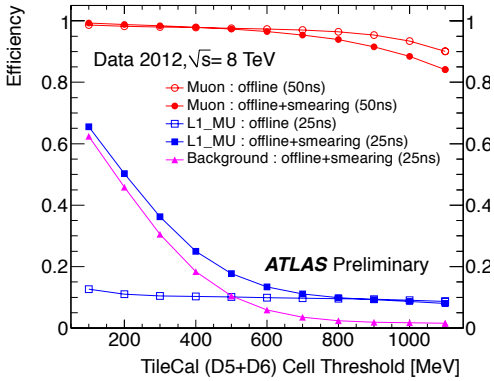
See talk by Titus Masike

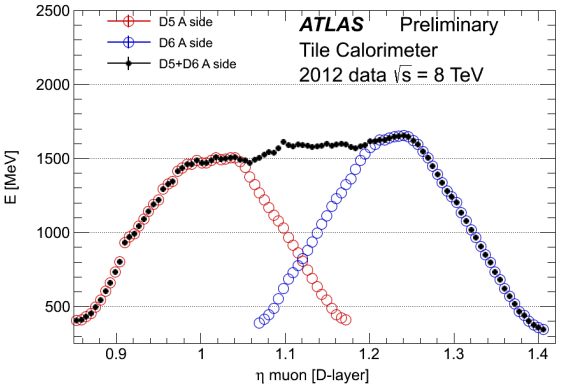
Phase-I upgrade

- Level 1 single Muon trigger at 20 GeV is expected to be 34 kHz but Trigger can only handle below 25 kHz
  - Should be reduced otherwise will be heavily scaled down randomly
- A New Small Wheel (NSW) covering 1.3 < η < 2.4 will do coincidence with TGC
- Complemented by the coincidence in the outermost radial layer of Tile (D-cell) covering 1.0 < η < 1.3
- Possibility to reduce the large fake rate in the end-cap region up to ~60%
  - In D5 D6 region we expect a 82% reduction rate at 500 MeV threshold

ATLAS TDAQ Phase-I Upgrade TDR

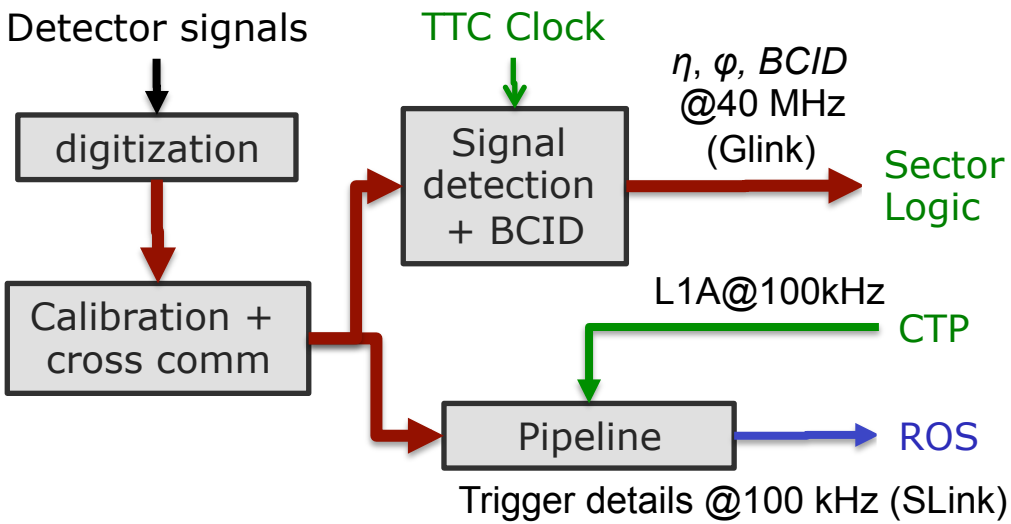




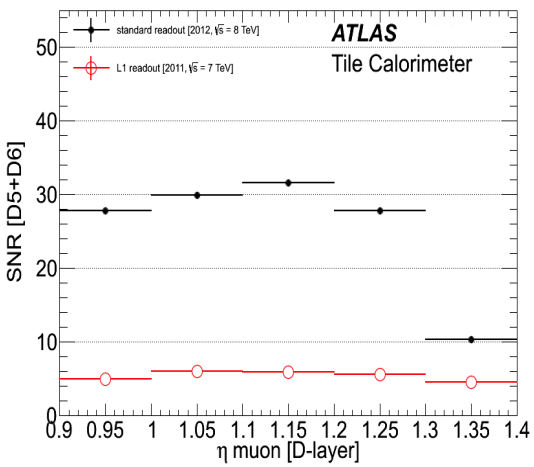


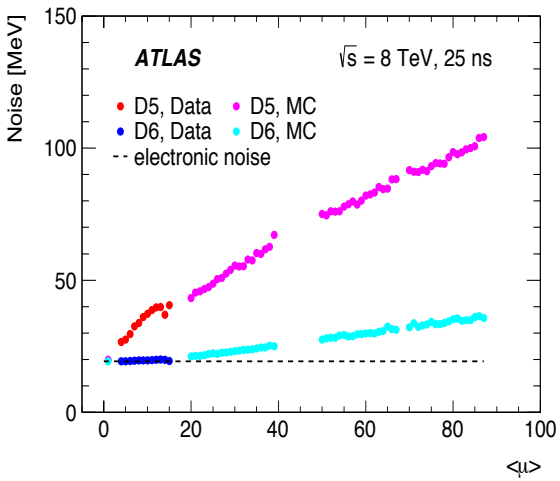
Tile Muon D-layer Board

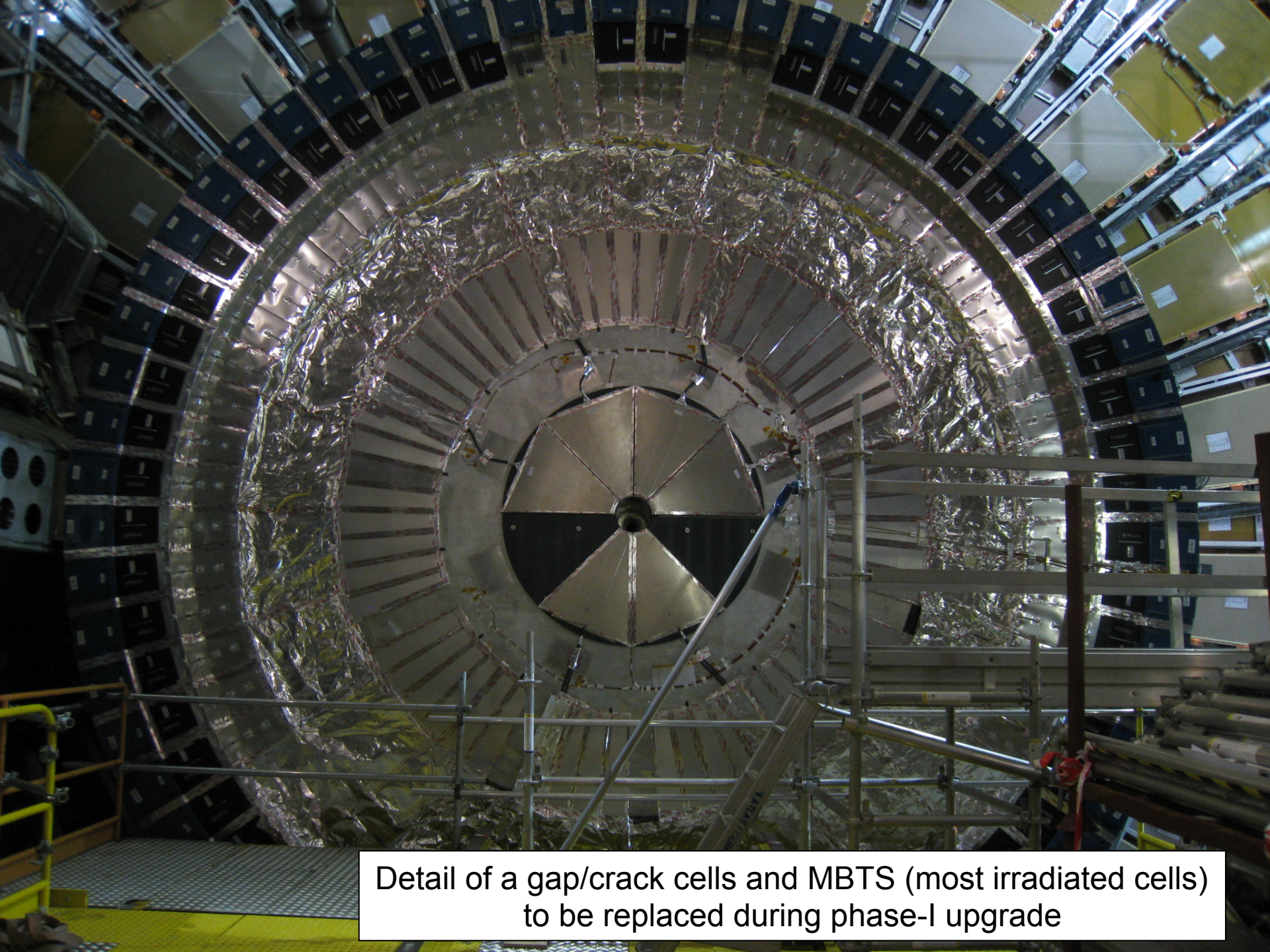
- New Tile Muon D-layer boards will read-out 512 muon outputs (64 modules x 2 barrels x 2 cells x 2 channels / cell), eight modules per board
- Provide the correct calibration and perform signal detection for each cell along with Bunch Crossing Identification
- Transmit the η, φ, and bunch number from the detected cells to the new sector logic board through GLink
- Connect to neighbour receiver boards due to different granularity in φ, 64 tile modules for 48 muon trigger sector logic
- Provide ROD data fragments to the DAQ system through SLink



Tile muon D-layer board block diagram



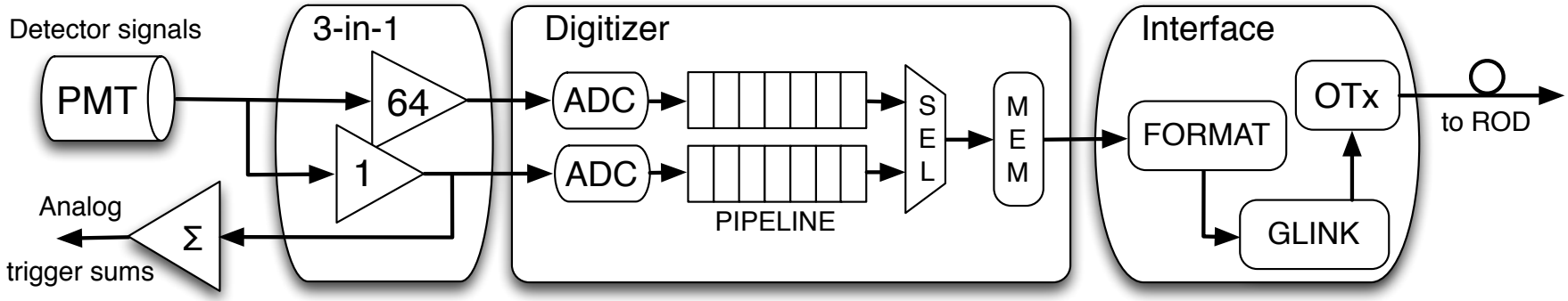




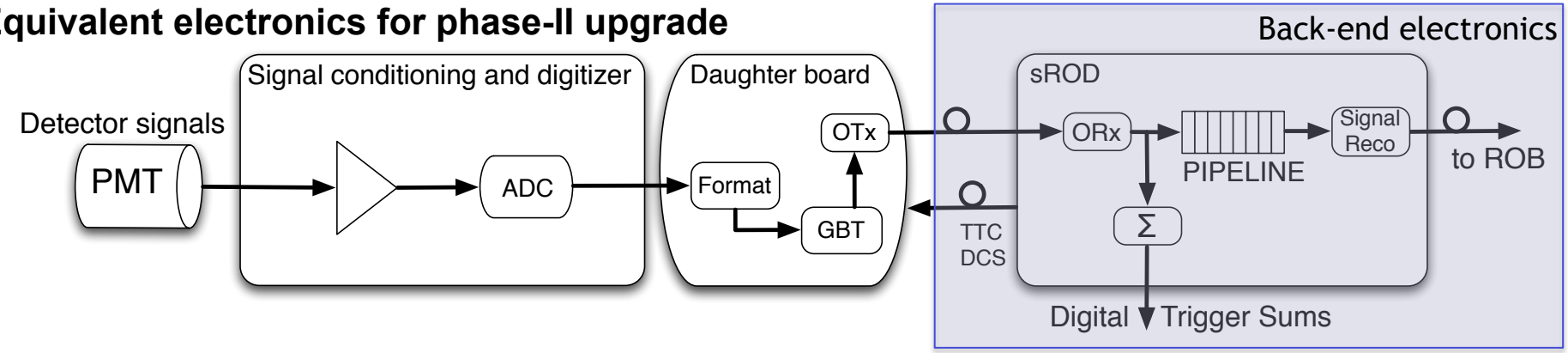
Detail of a gap/crack cells and MBTS (most irradiated cells) to be replaced during phase-I upgrade

Phase-II upgrade

Present front-end electronics



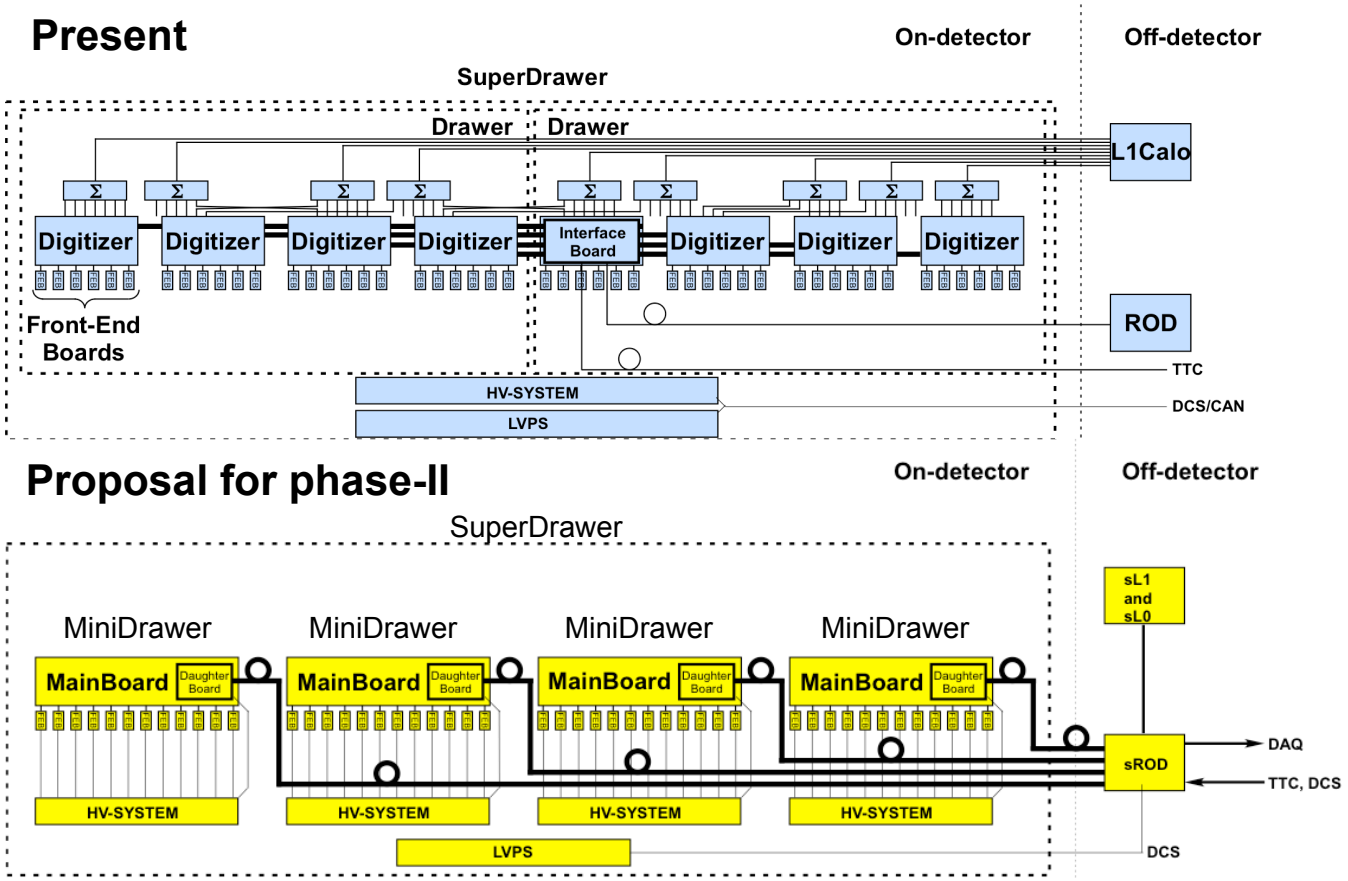
Equivalent electronics for phase-II upgrade



- Tile's plans for the upgrade phase-II of the LHC are to completely replace the front-end and back-end electronics introducing a new read-out strategy
  - Full digitization of signals at BC rate and transmission to off-detector electronics
  - Reduction of single point failures
  - Digital input to trigger Levels 0 and 1

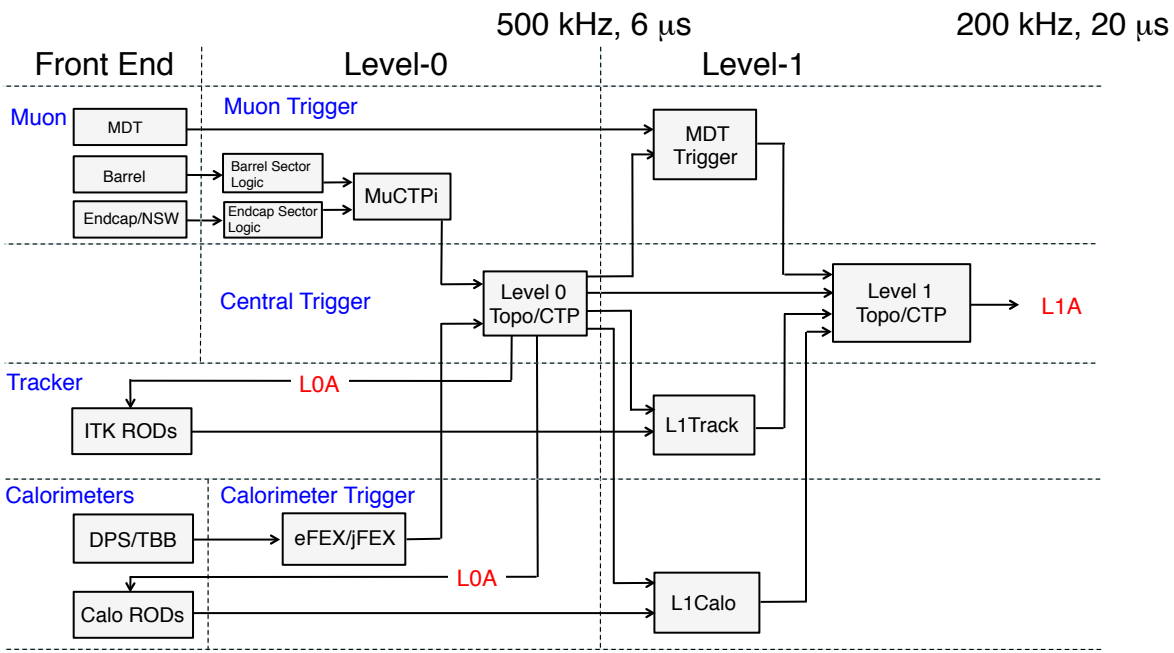
Changes in the front-end

- Aim to cope with luminosity increase and reduce single point failures (improve reliability)
  - **Fewer failure-prone connectors** in the new system, but also the challenge of routing **more fiber optic and LV cables**. Moving from dependent drawers to independent mini-drawers
  - **Increase the redundancy in the read-out path** from the cell to the backend
  - Similar **redundancy in the power distribution** and introduction of Point-Of-Load regulators



Changes in the back-end

	Present	Phase-II upgrade
Total bandwidth	~165 Gb/s	~40 Tb/s
Front-end links	256	4096
Bandwidth per link	640 Mb/s	10 Gb/s
Links per super-drawer	1 (+1 redundant)	4x4 (+4x4 redundant)
Bandwidth per super-drawer	640 Mb/s	160 Gb/s



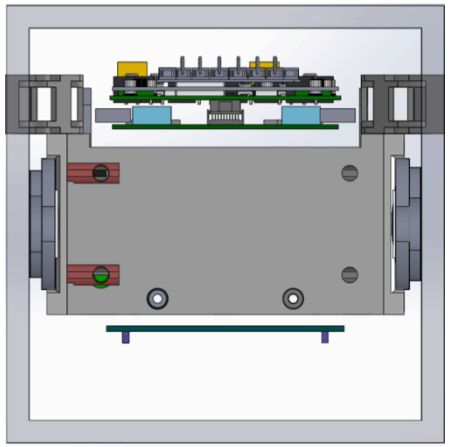
Block diagram of the Level-0/Level-1 hardware trigger

Tile upgrade demonstrator

- In order to test the technology for phase-II upgrade we are developing a hybrid demonstrator slice containing the new components but compatible at the functional level with the current design
  - Redundancy against SPF
  - Radiation tolerance up to 100 kRad
  - Error correction and triple redundant designs
  - Sampling and read-out in all BCs
  - Precision of 16 bits above noise level in two 12 bit gains

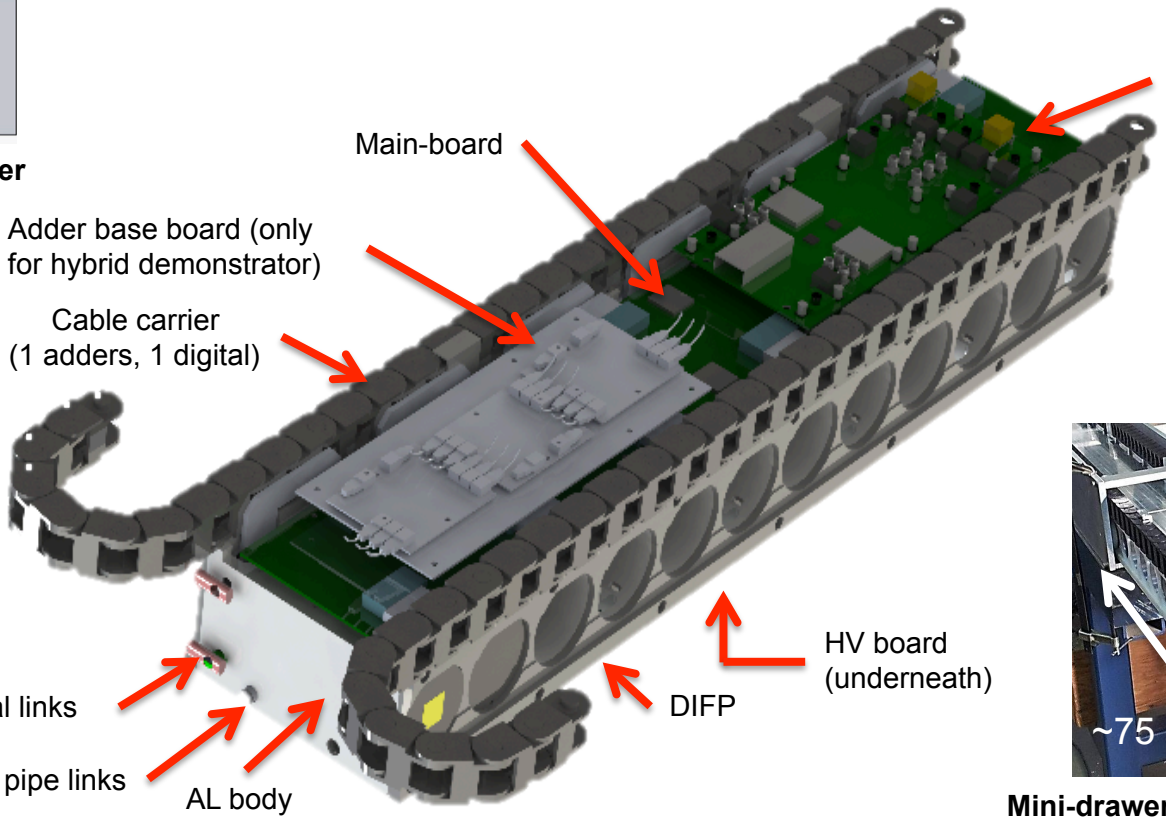
Mini-drawers

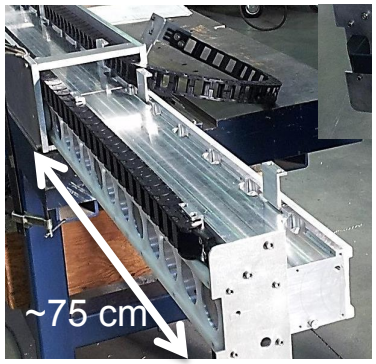
- Super-drawer demonstrator will be composed of 4 mini-drawers, each one containing
  - 12 front-end boards: 1 out of 3 different options
  - 1 main-board: for the corresponding FEB option
  - 1 daughter-board: single design
  - 1 HV regulation board: 1 out of 2 different options
  - 1 adder base board + 3 adder cards: for hybrid demonstrator



Cross section of a mini-drawer

Empty cable carrier

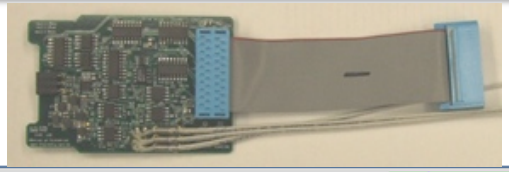


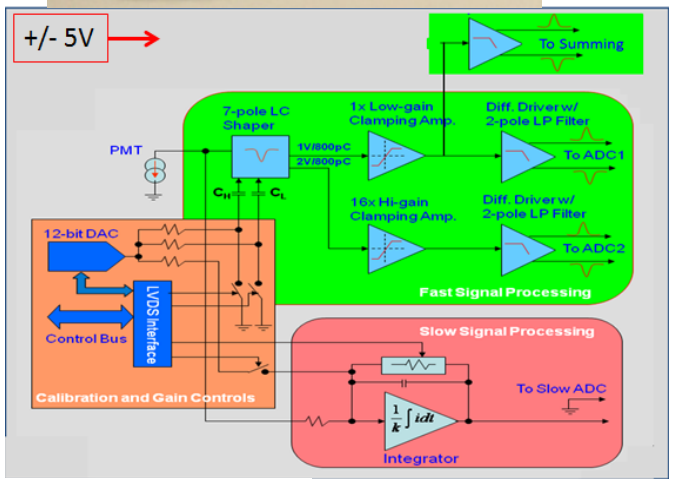


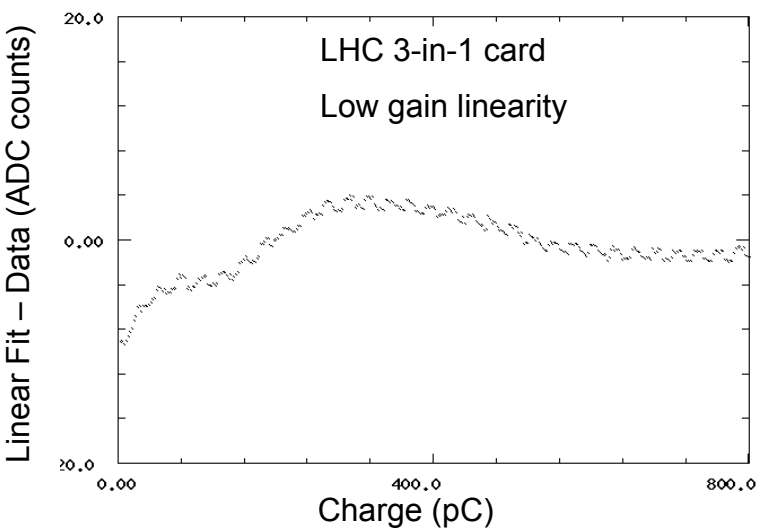
Mini-drawer with cable carriers

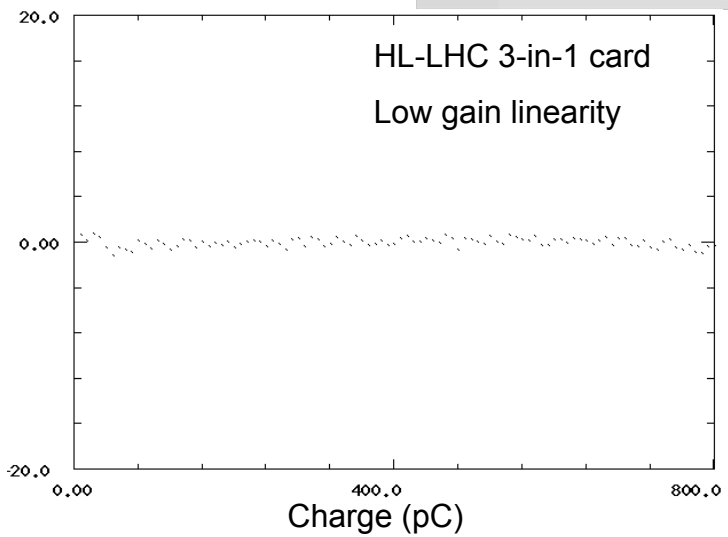
Front-end board option 1: New 3-in-1 Only option for first demonstrator

- Based on current 3-in-1 cards that provides 3 functionalities
  - High and low gain analog outputs
  - Charge injection calibration
  - Integrator read-out for dedicated and in-physics calibration data
- HL-LHC design has higher radiation tolerance and better performance
  - One component failed radiation test for sLHC, reverted to previous
  - Longer cable needed to accommodate parity flip



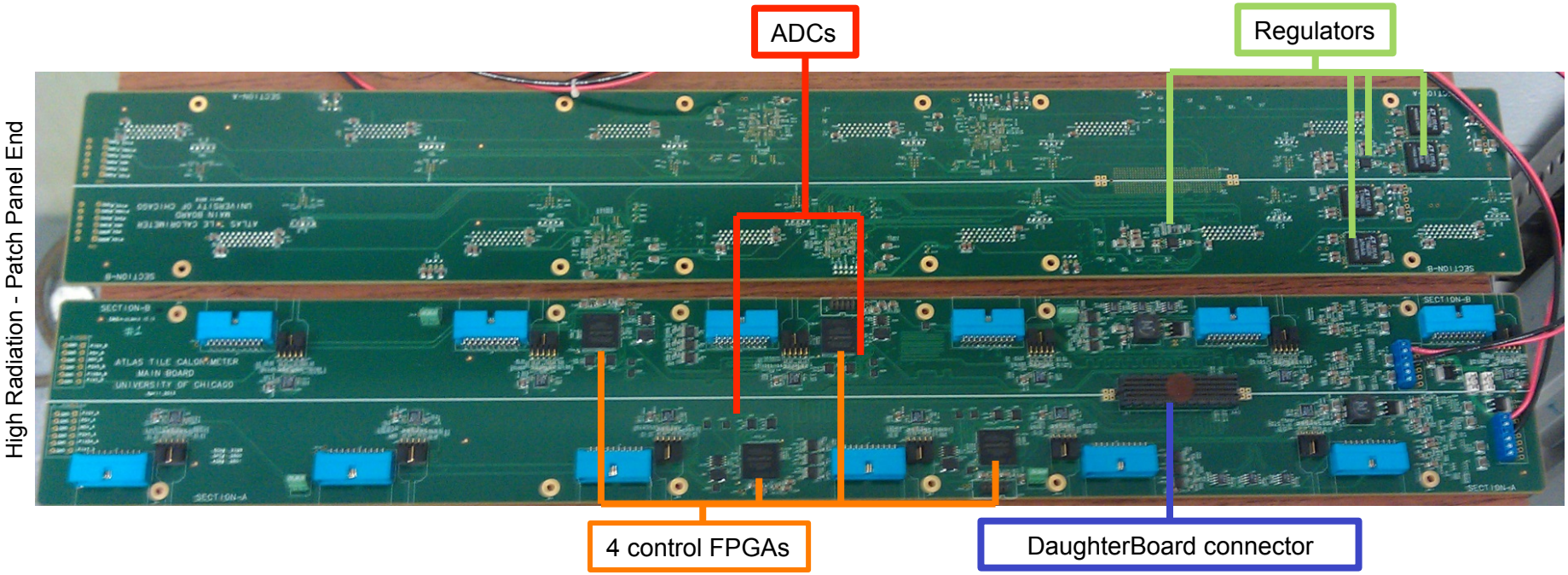






This option will be used in the hybrid demonstrator since it can provide the analog output to the present Level 1 trigger

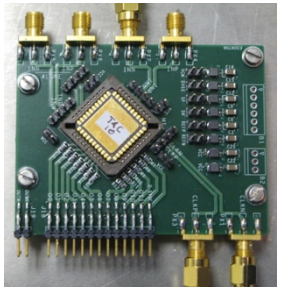
Mainboard for new 3-in-1 FEBs only option for first demonstrator



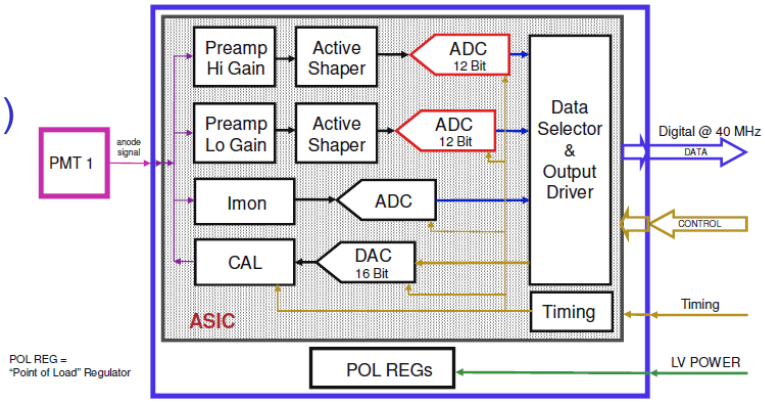
- Mainboard digitizes signals from FEBs with independent discrete ADCs
  - Mainboard is split into two halves
  - Each cell will be read-out by two PMTs, one on each side of the mainboard
  - Samples are transferred serially to the daughterboard at 600 MHz
  - Commands are sent in parallel to 2 control FPGAs on each side
- This front-end board + mainboard option will be evaluated together with the other two in test beams starting in 2015

Front-end board option 2: FE-ASIC

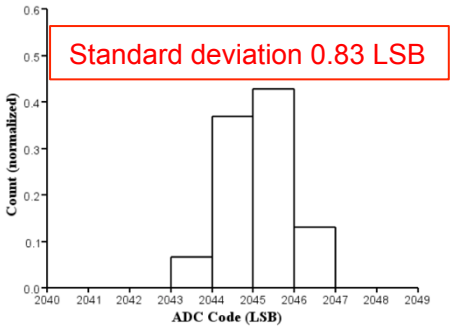
- Second option for a front-end board is based on an ASIC using IBM CMOS 130 nm technology
- FATALIC ASIC provides shaping in 3 gain ranges (1,8,64)
  - Third version being tested
- TACTIC ADC is a 12-bit ADC@40 MHz
  - First version delivered in January
  - Power consumption 61 mW
  - Measured noise smaller than one LSB
  - Bad integral non linearity due to bad coupling of amplifier capacitors
  - Second version needed
- Next steps
  - Tests with Cesium source before end of 2013
  - Design front-end board with FATALIC and TACTIC for spring 2014
  - Design of fourth version of FATALIC with 3 TACTIC ADCs embedded by May 2014 for delivery by November 2014
  - Design of Mainboard for this Front-end board option

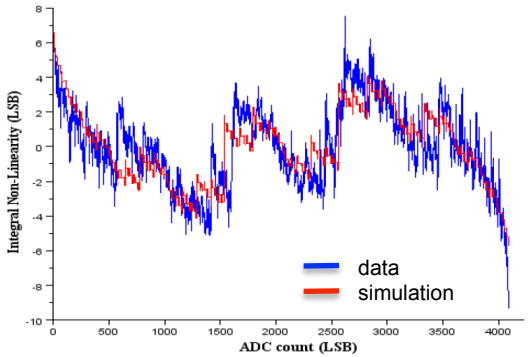


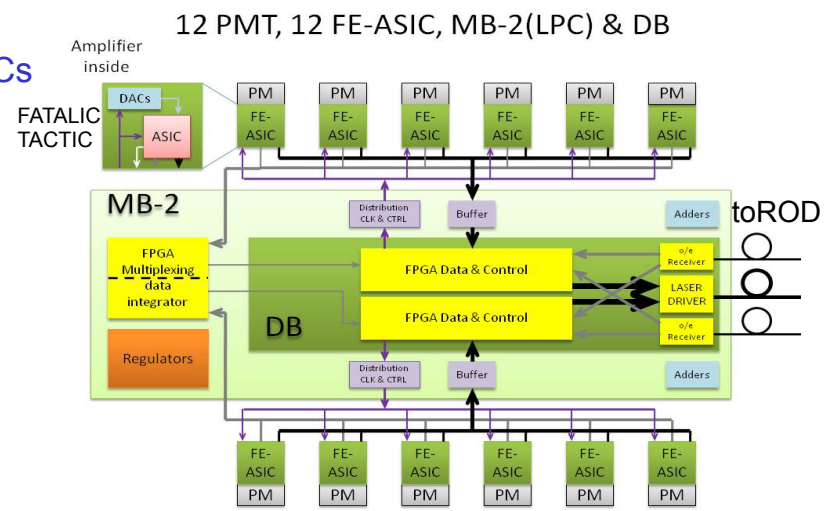
TACTIC ADC



Conceptual Design of FE-ASIC Front-End Board

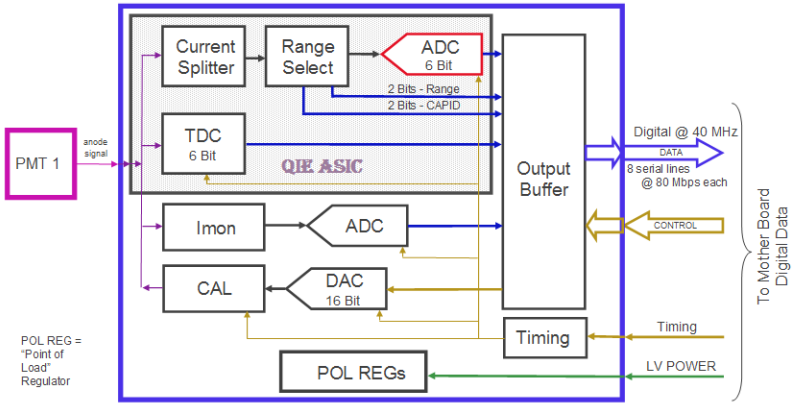




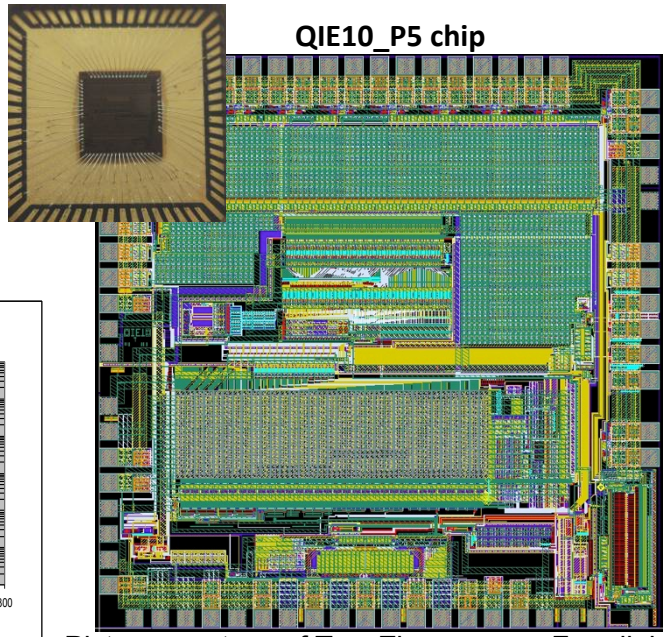


Front-end board option 3: QIE ASIC

- Third option for the front-end board is a charge integrator (different concept)
  - Performs a on-chip digitization with radiation tolerant design
  - Needs 4 clock cycles to acquire the data
  - Outputs a 17-bit dynamic range in 10 bits: 6-bit ADC value, 2 bits range (4 ranges), 2 bits CAPID
  - Clean measurement every 25 ns: No pulse shaping
  - Can be very useful against pile-up but requires technology change decision
  - Collaboration between ANL and FNAL
- Status with QIE10 design
  - 20 chips in hand, another 40 coming
  - Passed noise, dynamic response and TDC tests
  - OK for TID test up to 50 kRad
  - No SEUs in Shadow Register up to 6E12 p/cm2
- Next steps:
  - Front-end board for this option soon
  - Full drawer tests in summer 2014 and Test beam in 2015

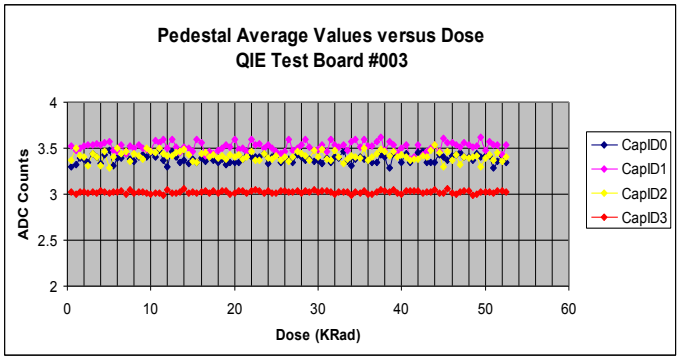


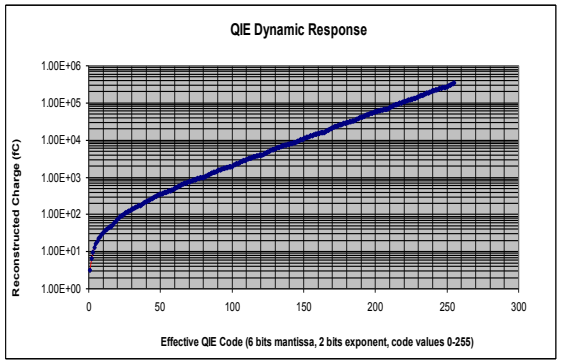
Conceptual Design of QIE Front-End Board



QIE10_P5 chip

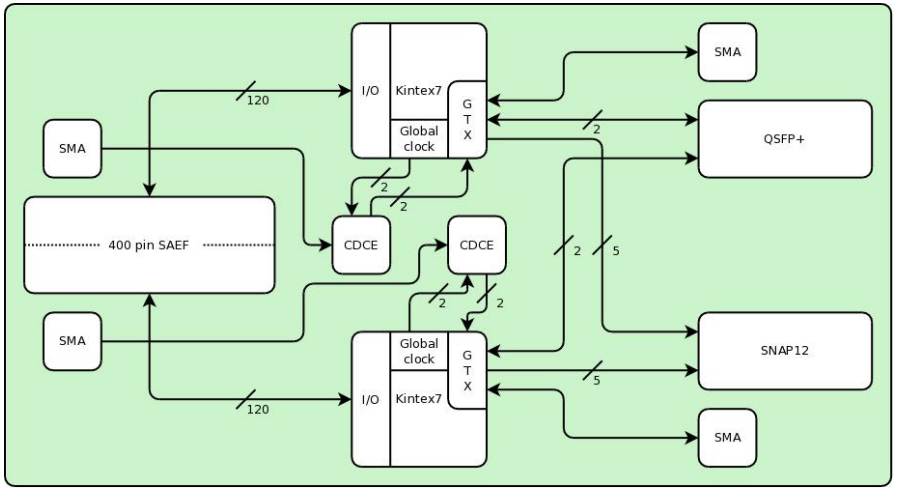
Picture courtesy of Tom Zimmerman, Fermilab



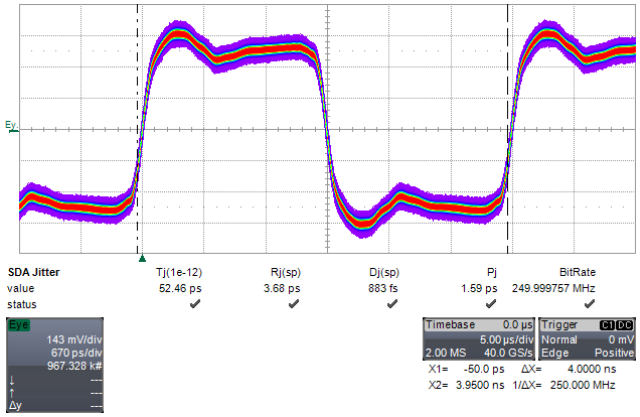


Daughter-board

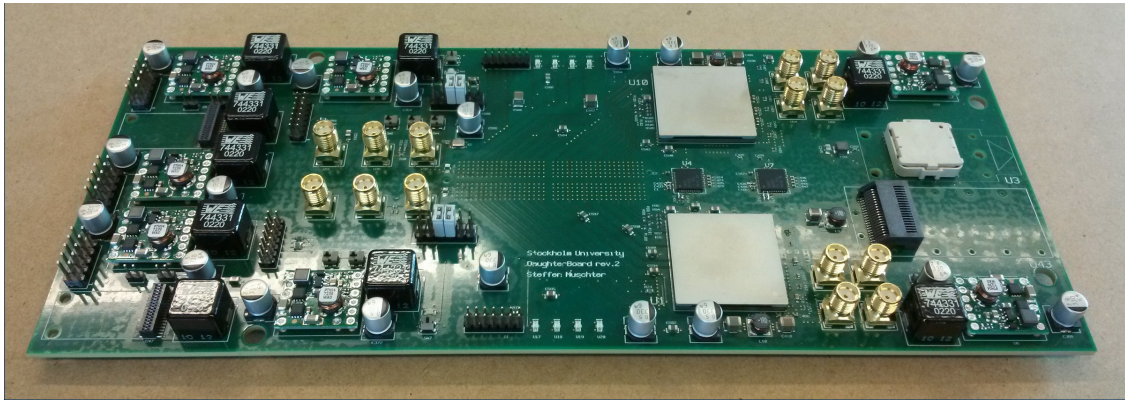
- Daughter-board provides GBT communication with back-end electronics
  - Implementing a **redundant** system on a single PCB + triple redundant FPGA programming
  - Two Kintex 7 FPGAs and two QSFP Modulators at 40 Gb/s
  - Firmware can be also uploaded through the optical link
- Status
  - First prototype tested in 2011
  - Second prototype manufactured in 2012 managed to provide continuous data stream to back-end
  - Third prototype under design



Conceptual design of daughter-board (second prototype)



CDCE62005 output signal synthesized from 100 MHz input



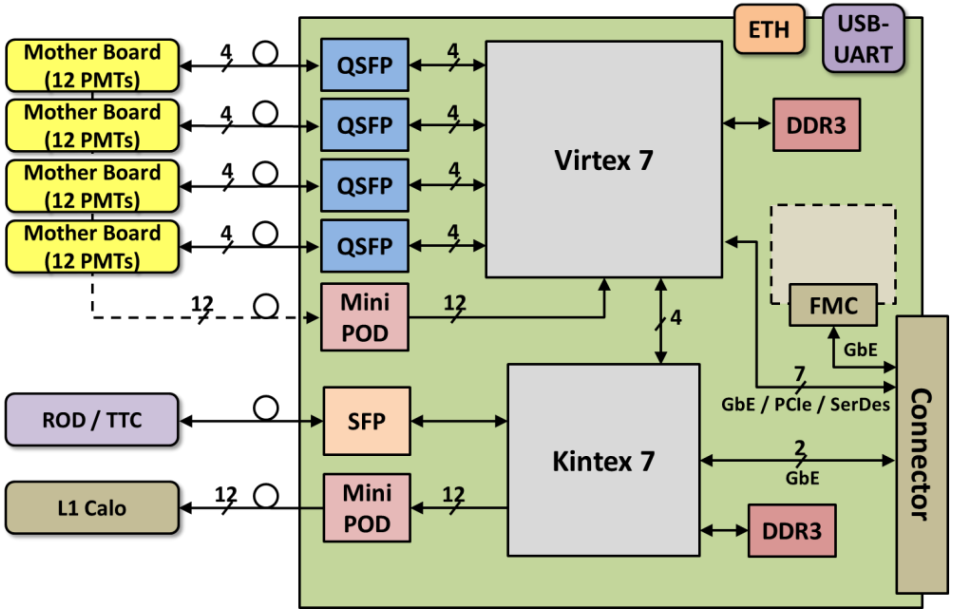
Second prototype of daughter-board (still with one modulator and one PPOD)

Super Read-Out Driver prototype

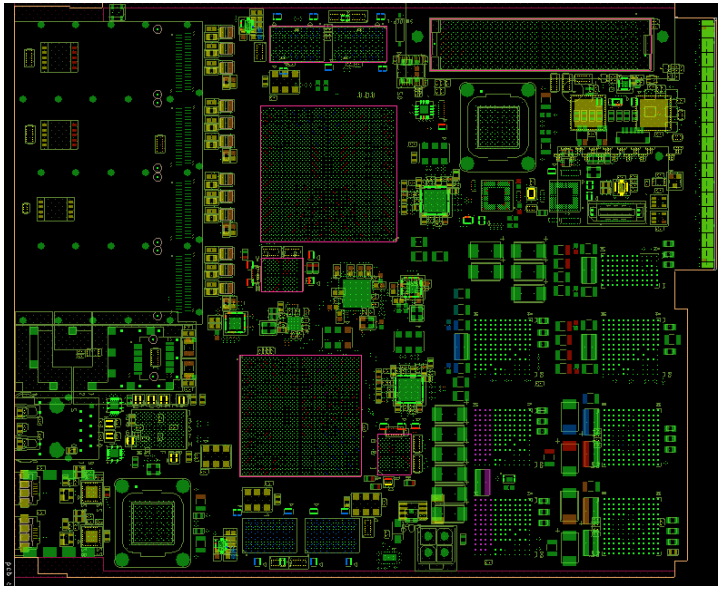
- Super-ROD is the core back-end electronics component
  - Prototype compliant with mid size AMC (180.6 mm x 148.5 mm)
  - Read-out of a complete super-drawer (4 mini-drawers) with QSFPs
  - Corresponding to ¼ of input links of the design for phase-II
  - 1 Xilinx Virtex 7 FPGA (XC7VX485T-2FFG1558) 48 GTX@10Gb/s for data/DCS input and TTC/DCS output
  - 1 Xilinx Kintex 7 FPGA (XC7K420T-2FFG901) 28 GTX@10Gb/s to interface current ROD/TTC and L1Calo
  - 512 MB DDR3 SDRAM and 1 Gb flash per FPGA
- First prototype almost ready for manufacturer
  - Stack-up 18 layers in ~1.7 mm (10 power, 8 signal)

ATCA shelf

See talk by Robert Reed

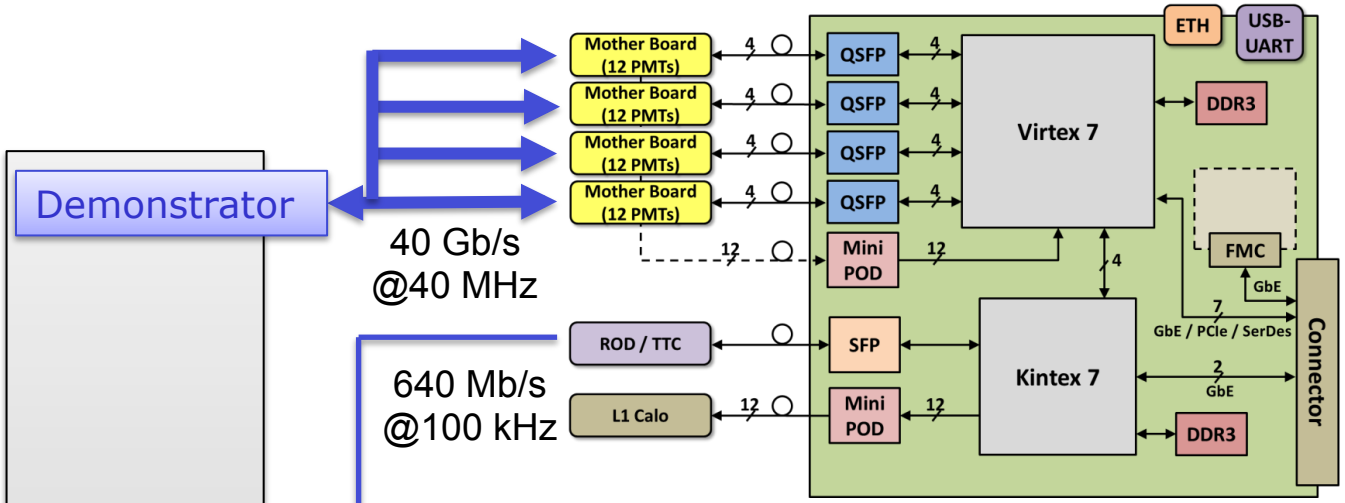


Conceptual design of super-ROD prototype

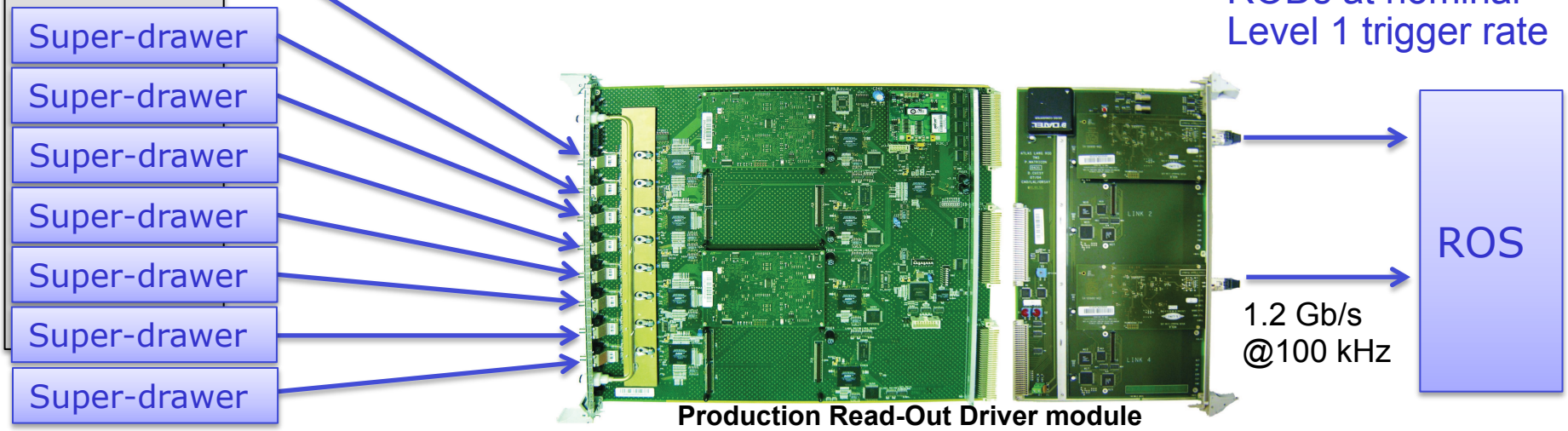


Super-ROD prototype layout view

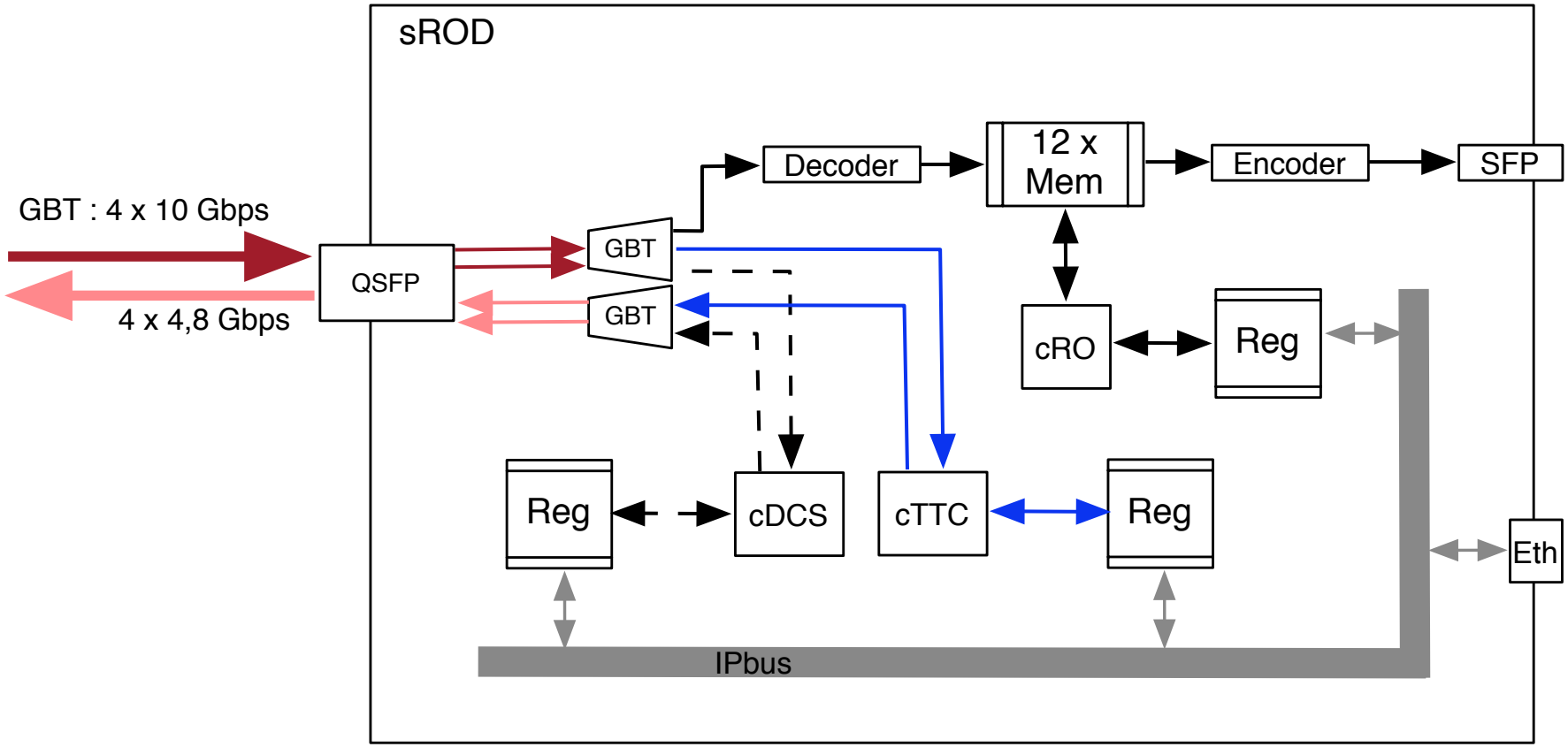
Integration of the demonstrator



- A demonstrator super-drawer of the upgrade phase-II front-end electronics will be installed in ATLAS during Run 2
- A super-ROD prototype will read-out all the samples from the front-end and transfer a data frame to current RODs at nominal Level 1 trigger rate



Block diagram of sROD prototype



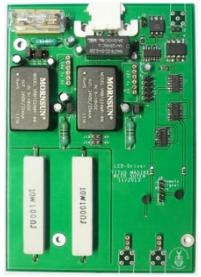
A portable test-bench for upgraded electronics

- A portable readout module for mini-drawers (Prometeo) is under development
  - Stand-alone test-bench to assess the QA the electronics
- Hardware
  - Based on a Virtex 7 evaluation board
  - QSFP module provides optical connection
  - HV and LED driver boards test response of PMTs
  - 16 channel ADC mezzanine to digitize the output of trigger cables from previous test-bench
- Software
  - Based on IPbus, QT framework
  - Modular implementation to allow particular test implementation
- Status
  - All hardware components in hand, casing and cabling in progress
  - Firmware under design

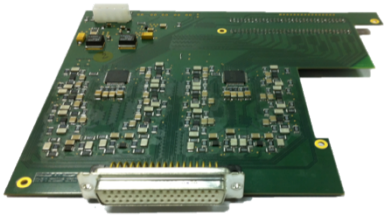
Virtex7 evaluation board

QSFP FMC module

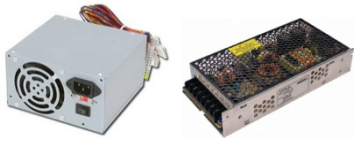
HV PS



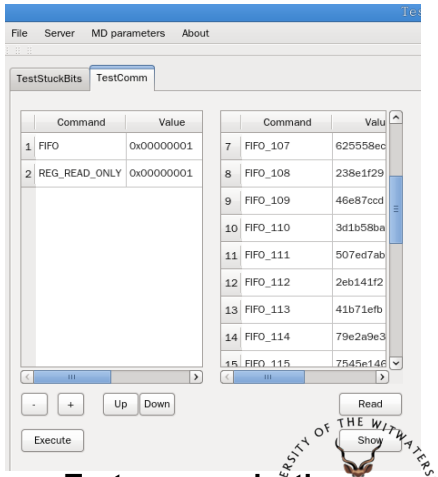
LED driver



16 channel ADC (hybrid demonstrator only)



System power supply (commercial ATX + 24V)

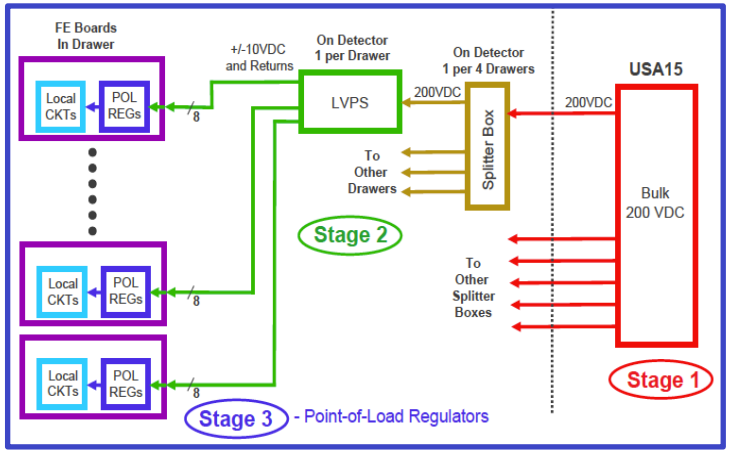


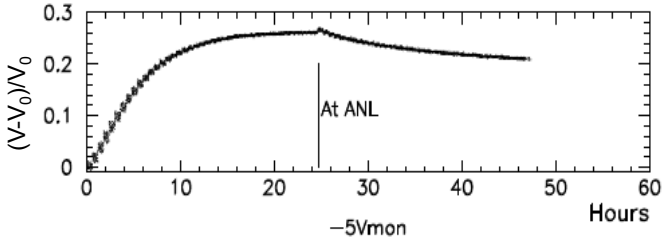
Test communication software panel

See talk by Xifeng Ruan

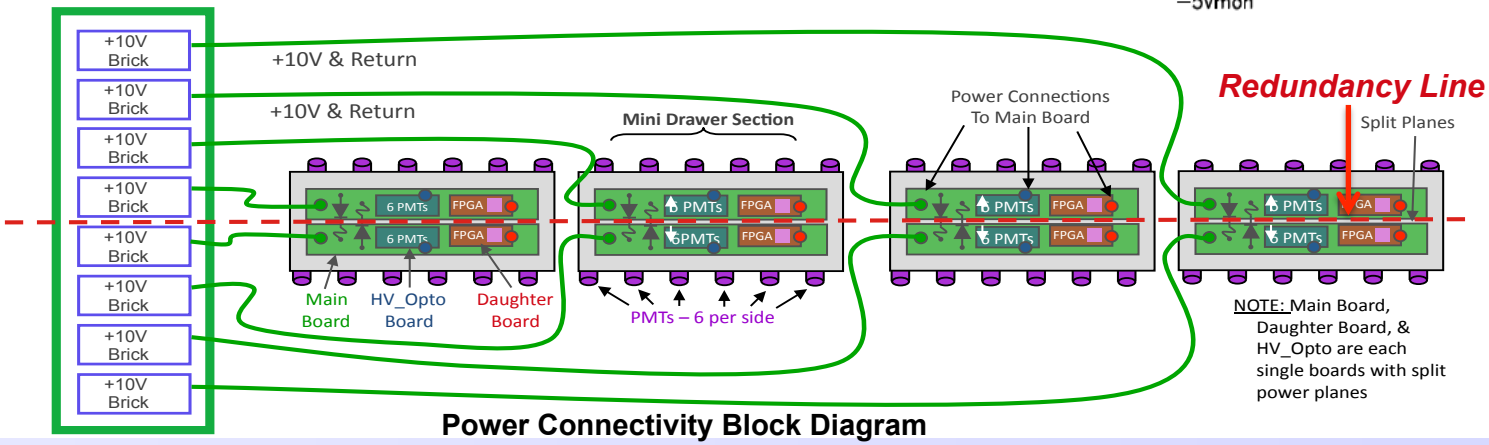
Low Voltage Power Distribution

- Based on a three stage power distribution system
- Stage 1: bulk 200VDC PS in USA15
  - Provide power to four super-drawers
- Stage 2: LVPS boxes in front of super-drawers
  - New design providing only +10V in 8 separate bricks
  - Each brick serving half a mini-drawer
  - Require a factor 2 in the current output for redundancy
  - Already produced 3 units ready and shipped to CERN
- Stage 3: Point-of-Load regulators
  - Point to point connection from brick to mainboards
  - If one brick stops working, redundancy supply provides power through diode on the mainboard
  - Completed TID tests on 5 commercial off-the-shelf regulators with marginal results for -5V regulator
  - NIEL and SEU tests to be done in December 2013





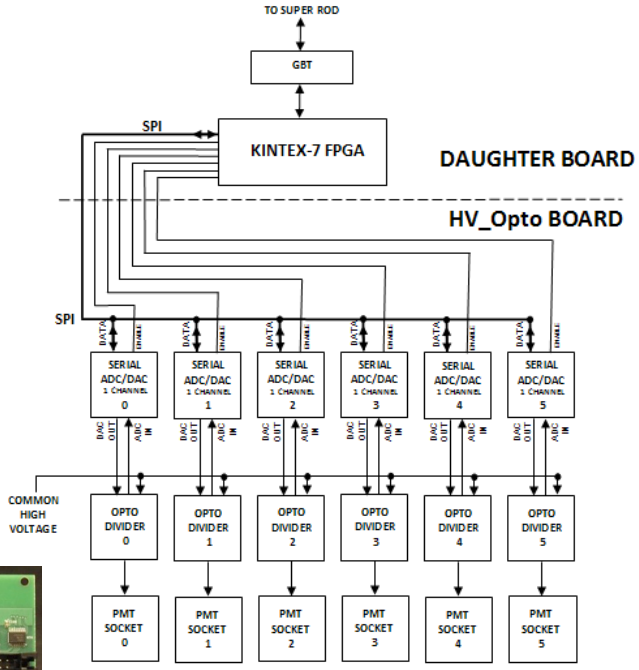
V8.0.1 brick

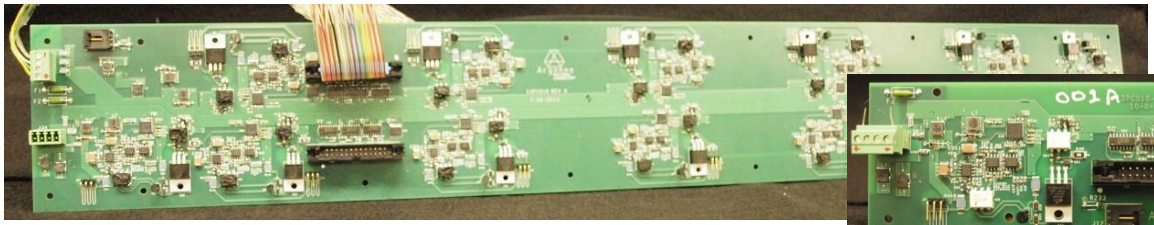


Power Connectivity Block Diagram

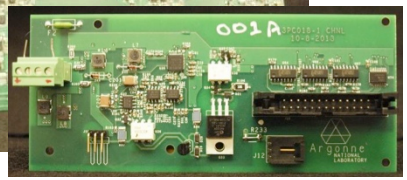
High Voltage Power Distribution

- Two solutions are under evaluation to provide HV to the front-end based on commercial off-the-shelf components
  - Voltage regulation in USA15 vs front-end (HV_Opto board)
- First version of the HV_Opto board largely based on existing design
  - Introducing possibility of switching on/off individual PMTs
  - HV_micro replaced by the Kintex-7 FPGA in the daughter-board: Specifications being defined
  - Interface to DCS through super-ROD: Discussions in progress
  - Control of HV settings via VHDL module: Implementation in progress
  - First board completely tested and performance meets specifications





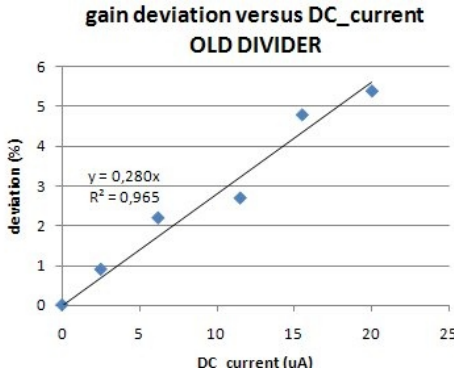
First prototype of HV_Opto board ready for mini-drawer tests

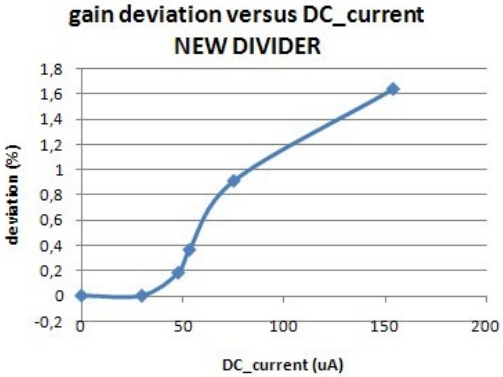


Single Channel Board for radiation tests

- Passive HV dividers of PMTs will be replaced by active ones to maintain stability
  - Tested for NEIL up to 1.5×10^{13} 1 MeV n/cm^2
  - Rejected huge number of first batch due to bad HV cable welding
  - Massive test of active dividers in Run 2

Old Dividers: ~2% non linearity at ~7.5 μA
New Divider: ~1% non linearity at ~75 μA





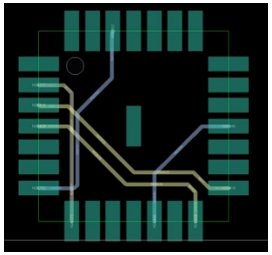
Optical links

- Directly modulated lasers (including VCSELs)
  - Have been qualified at ~10 Gb/s per link with a Bit Error Rate (BER) ~10^{-12}
  - Increasing bandwidth increases problems
  - Commercial VCSEL arrays (SNAP12) have shown Single Event Upset (SEU) at ~10^{10} p/cm^2
  - Also these use Multi Mode fibers which are more expensive

10^{-12} BER = ~900 errors per day

10^{-18} BER = 1 error in ~1000 days

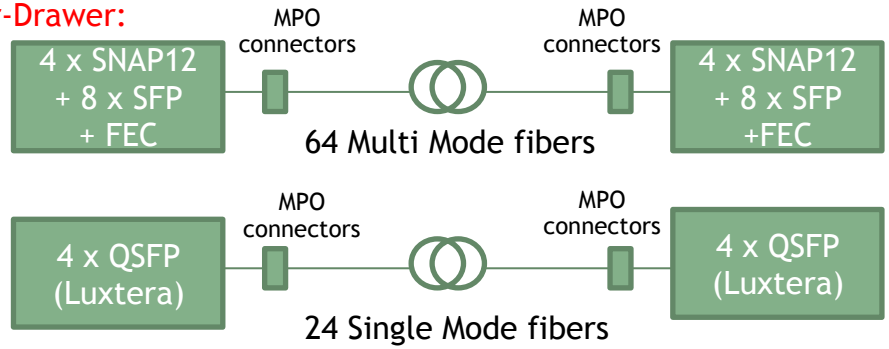
- A commercial off-the-shelf solution exists that uses single mode fibers at high transfer rates from Molex using Silicon Photonics technology developed by Luxtera (QSFP Active Optical Cable)
  - Can operate above 40 Gb/s (4x10) with BER < 10^{-18}
  - Made out of 130 nm Silicon On Insulator CMOS which should be very radiation hard
  - Radiation tests showed no SEU at TID of 165 kRad and fluence of 8×10^{11} p/cm^2
  - Problem is the PIC microcontroller used for configuration and monitoring survives ~20 kRad
  - A PIC replacement board has been designed, and control done from FPGA
  - Firmware to initialize the electro-optical chip has been developed
  - Several anti-fuse FPGAs are being evaluated and will be tested for radiation tolerance



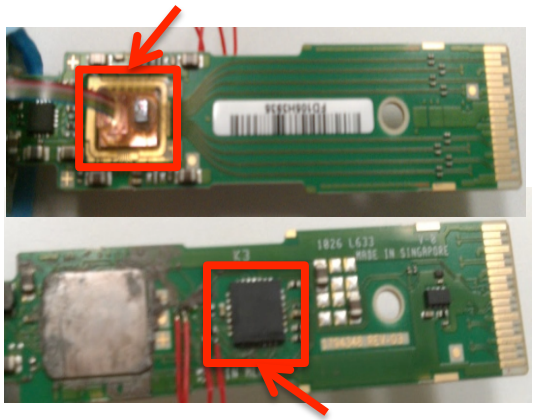
PIC Replacement Board

- QSFPs are the preferred option for the demonstrator
  - Less fibers vs lower clock frequency

Per Super-Drawer:

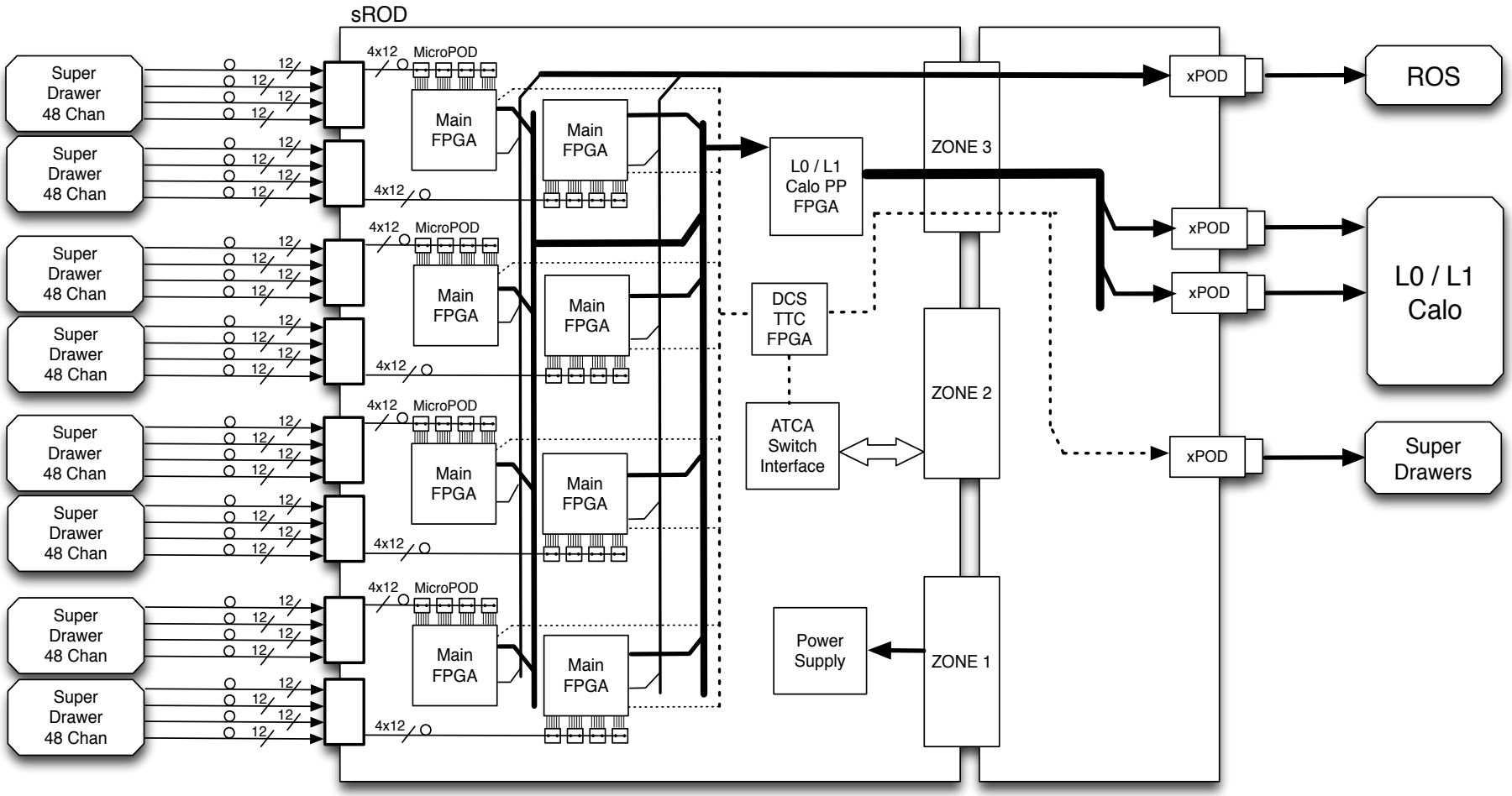


Modulator

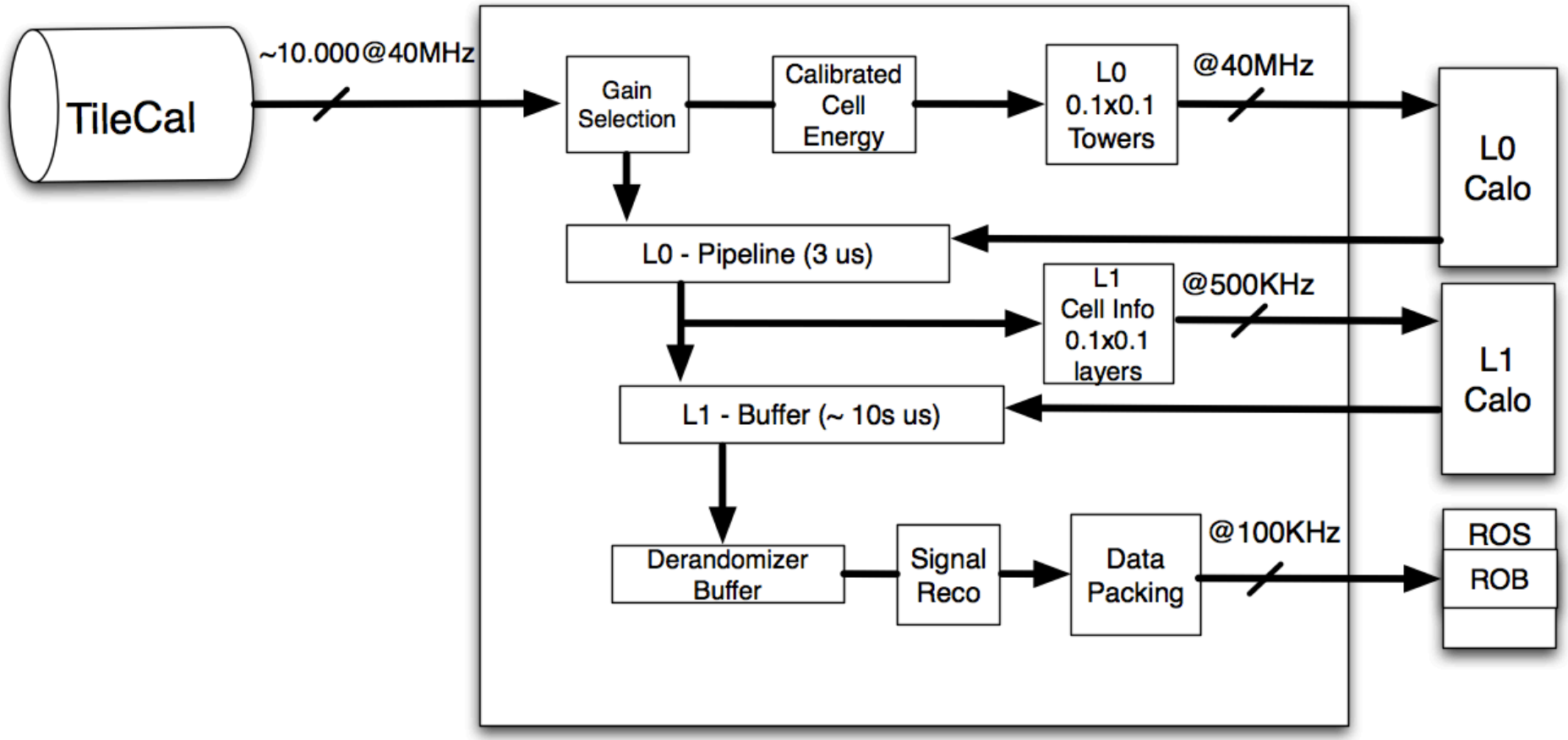


PIC Microcontroller

Super ROD for phase-II

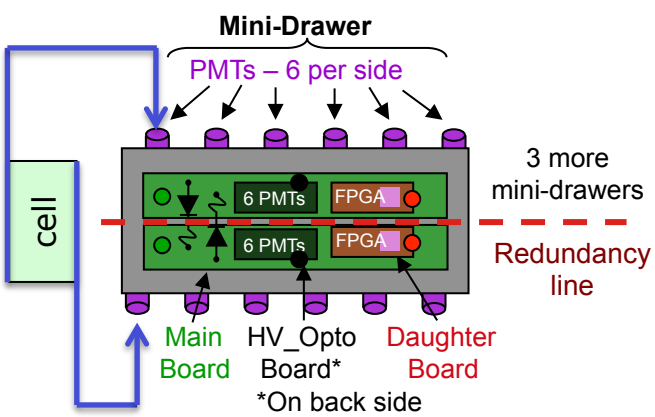


sROD block diagram

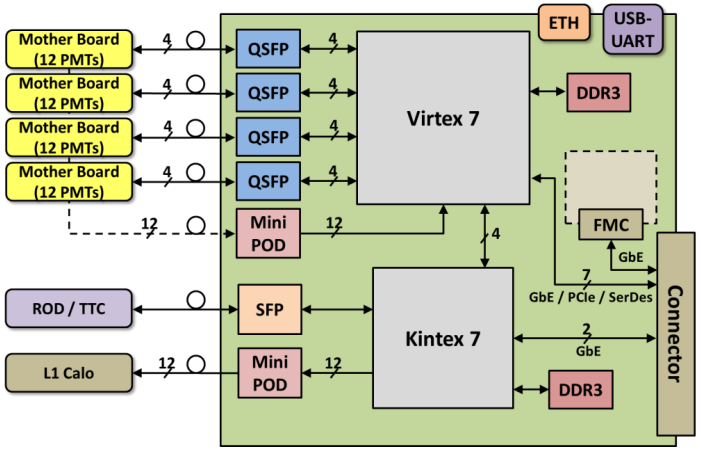


Conclusions

- Upgrade phase-0 aims to consolidate the detector
- Biggest challenge for upgrade phase-I is the read-out of the D-Layer cells to contribute to the Level 1 muon trigger
- The plans for the upgrade phase-II are to completely replace the front-end and back-end electronics introducing a new read-out strategy
- The upgrade of the ATLAS Tile calorimeter for the HL-LHC requires
  - increase in radiation hardness and front-end redundancy
  - Increase in the throughput and computing power of the back-end electronics



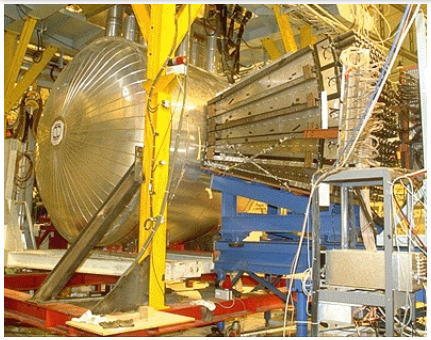
Cartoon of a mini-drawer for phase-II upgrade



Cartoon of a read-out driver for the phase-II upgrade

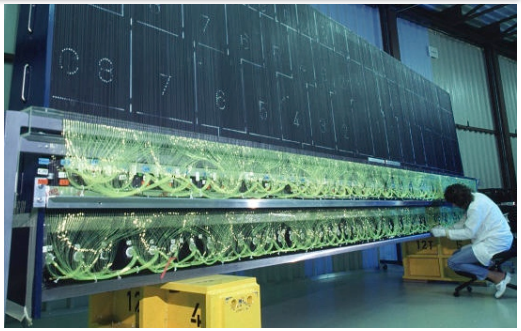
Backup

A bit of ATLAS history

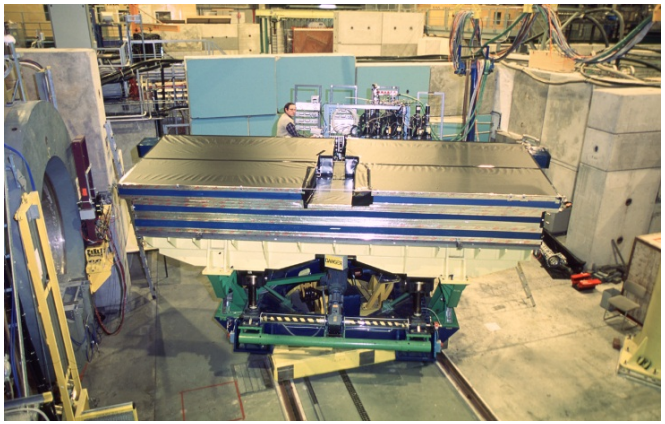


1993 – 1995: R&D

1996 – 2002: Construction



1999 – 2002: Instrumentation

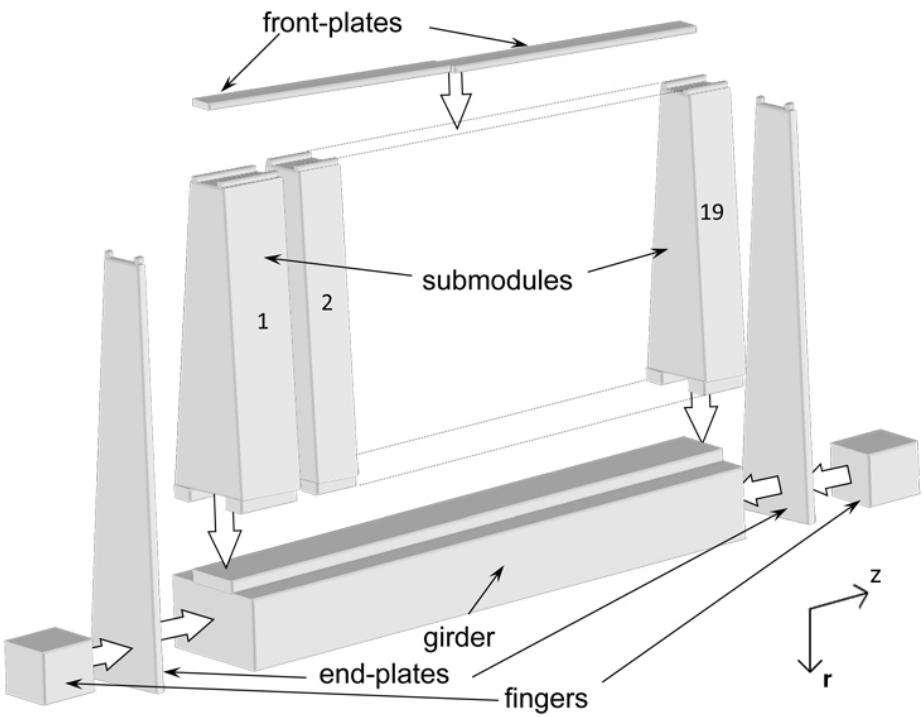


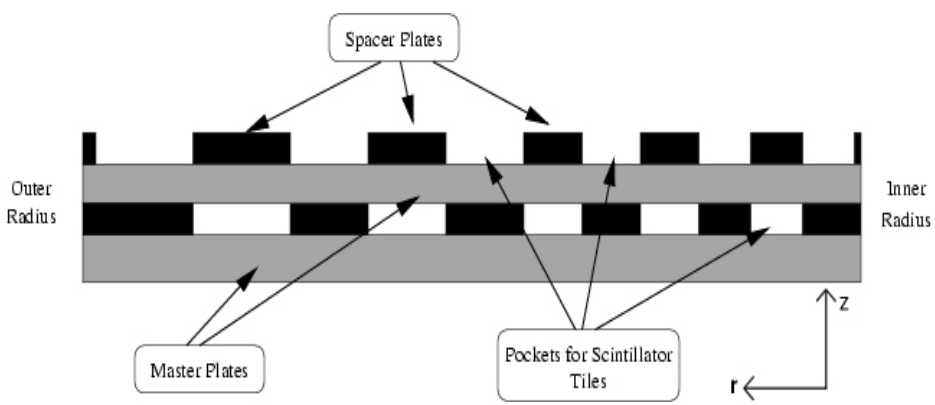
2000 – 2004: Test-beam

2004 – 2006: Installation

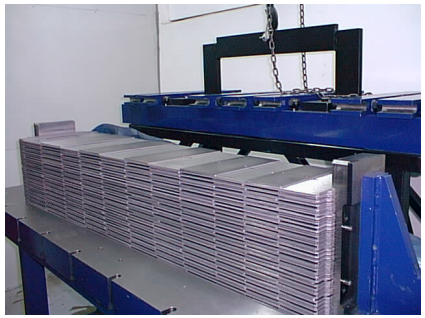
2005 – 2009: Commissioning with particles and calibration systems
2010 – 2013: Operation in LHC run 1
2013 – 2015: Electronics consolidation during Long Shutdown 1

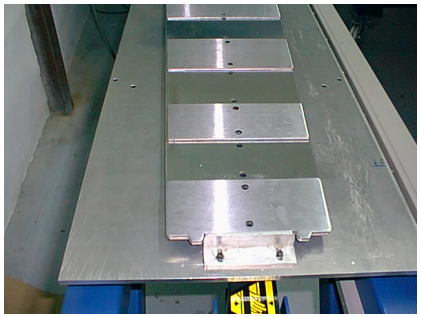
Tile module construction



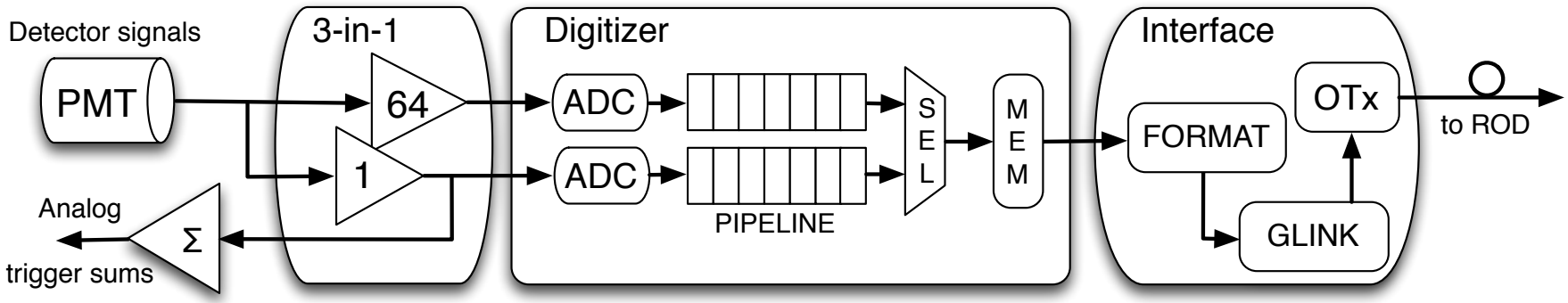


- Each module is built out of 19 sub-modules (~29 cm) which are attached to the girder
  - Constructed independently and before the optics instrumentation
- Spacer plates (4 mm) are placed in between two master plates (5 mm) leaving the space for the tiles (3 mm)
  - Periodicity of 18 mm
  - More details in 2013 JINST 8 T11001
- WLS fibers are placed along the spacer plates between two master plates without any compromise for extra space
- Similar assembly procedure can be followed for the LHeC detector



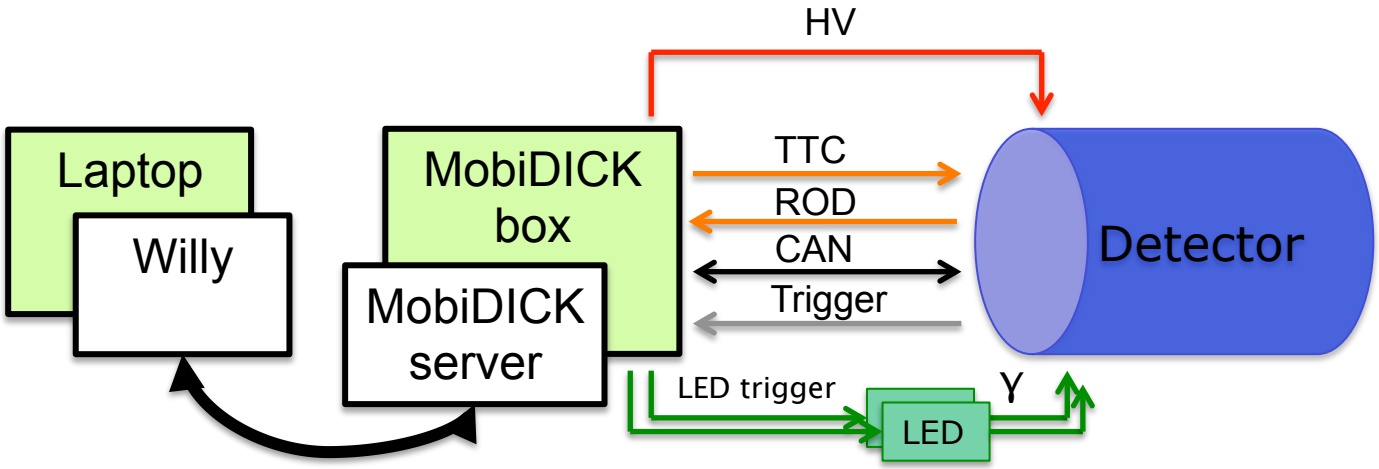


Functional representation



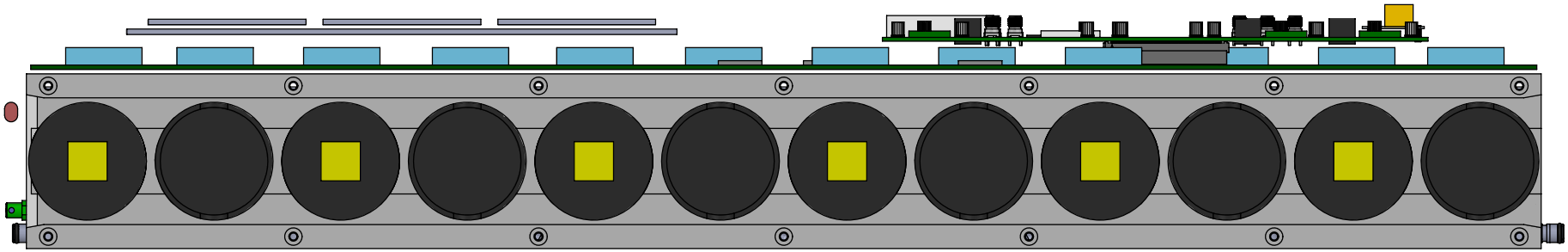
- The analog pulses from the PMTs undergo shaping and amplification in the 3-in-1 cards in two gains (low and high) with a ratio of 1:64. Low gain signals which are summed in groups by adder boards are provided to the Level 1 Calorimeter Trigger. The analog pulses are received by digitizer boards where the signal is converted into digital samples every 25 ns, which are stored in the front-end pipeline memories, the so called Data Management Units (DMU). Upon Level 1 accept, an event-frame--selector selects high gain samples unless the highest sample is saturated in which case the low gain samples are used and stores them in a buffer. Event frames are pulled from the DMUs by the Interface card which formats the data and transfers the frames to the off-detector Read-Out Drivers (RODs).

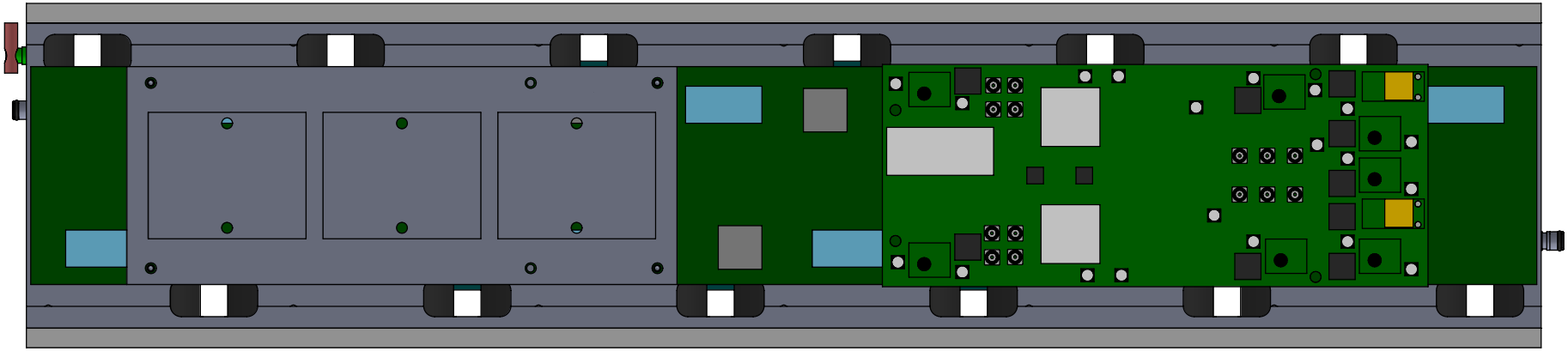
Overview of the MobiDICK4 system



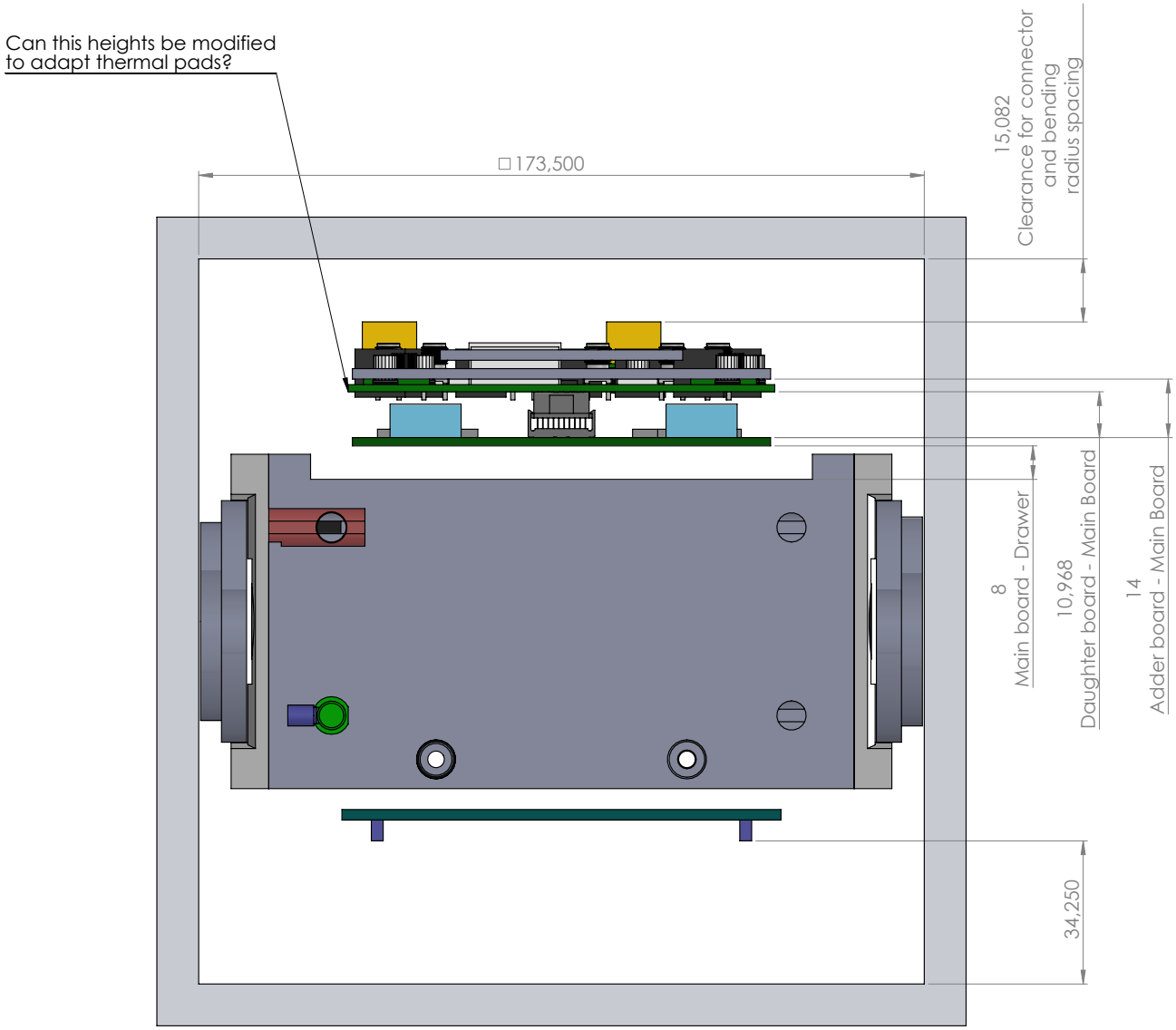
- MobiDICK box houses hardware needed to communicate with super-drawers
- MobiDICK server is the control application of the box
- Willy is the client software from which tests are executed
- Standard linux laptop runs Willy

Mini-drawer CAD view

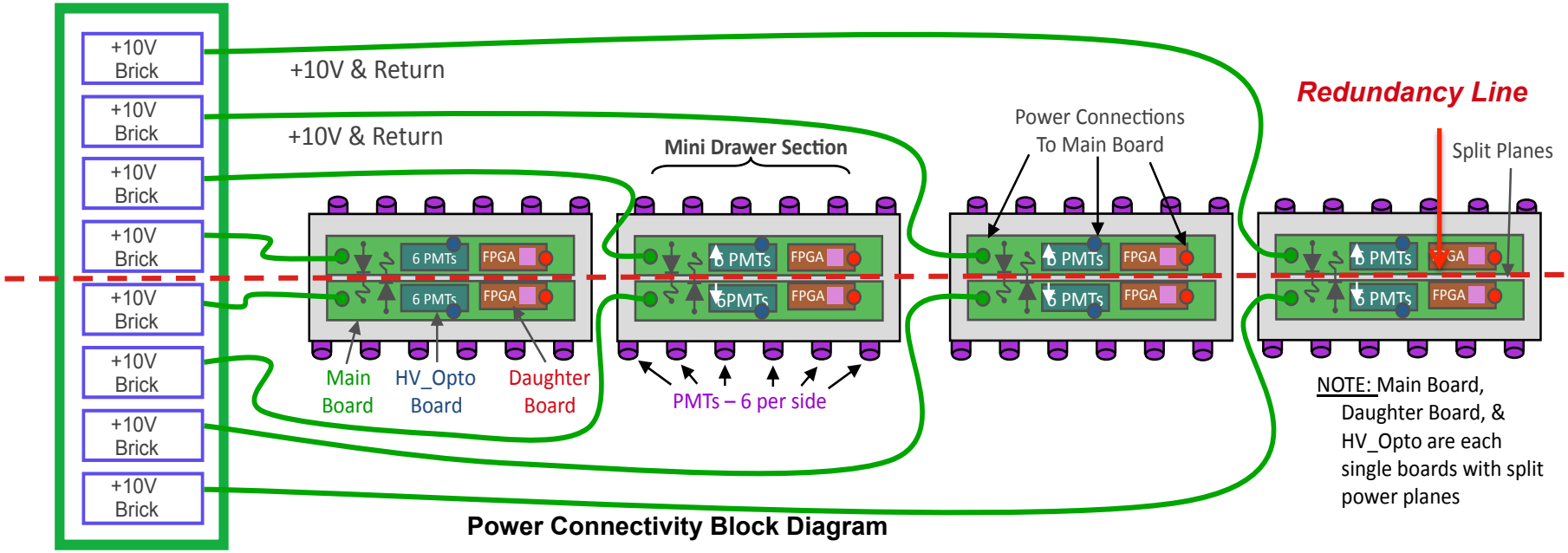




Mini-drawer cross section view



Redundancy in the electronics



- One of the lessons we have learnt from the electronics consolidation process in ATLAS during the LS1 is that we need to think the electronics to maximize the redundancy in case of failure, minimize the coverage damage in case of failure
- A double read-out for the cell should be accompanied by a redundant data path from the PMT up to the back-end electronics
  - Split the super-drawers into four independent mini-drawers
  - Split each mini-drawer into two independent halves (one cell read-out by one side)
  - Use redundant powering scheme

Second HV option

- External HV regulated from USA15 based on commercial off-the-shelf components
  - Regulated HV for each PMT distributed via multiconductor cables 100 m long
- Good progress: measured small noise and small voltage drop (~10 mV in 800V)