Single Event Effects qualification of candidate components for the ATLAS Tile Calorimeter Phase-II Upgrade Low Voltage power supply Bricks

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Pan-African Astro-Particle and Collider Physics Workshop (Online)

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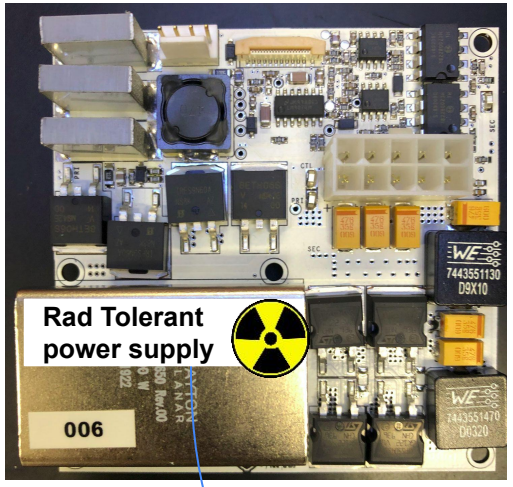
INSTITUTE FOR COLLIDER PARTICLE PHYSICS
UNIVERSITY OF THE WITWATERSRAND

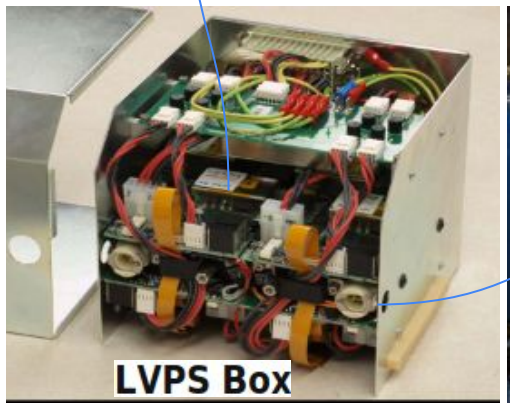
NRF National Research Foundation

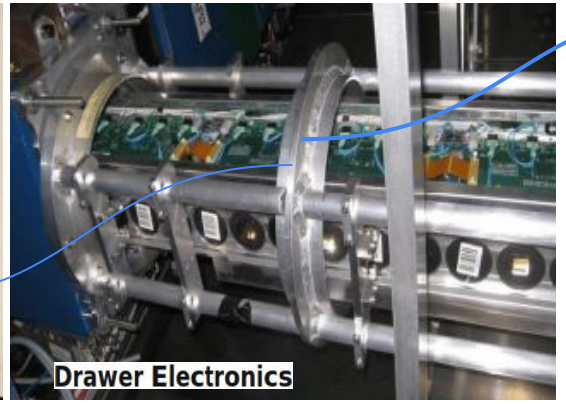
Context

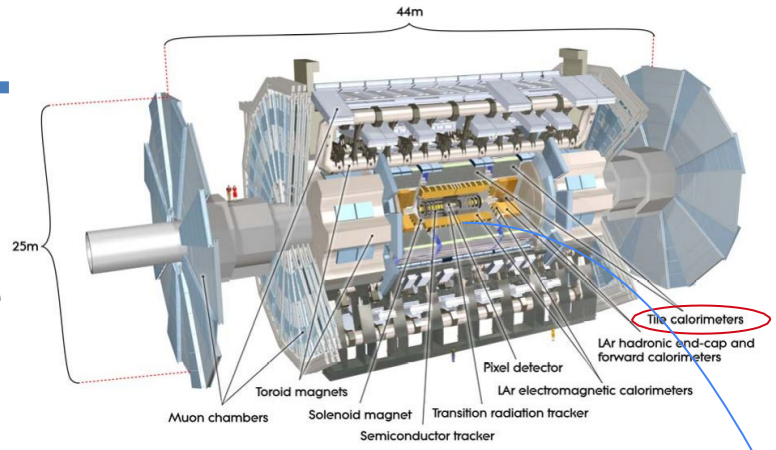
- **256** modules in detector, **~10,000** readout channels.
- **Iron** as absorber and **plastic scintillator** as active material.

SA contribution: 50% for TileCal

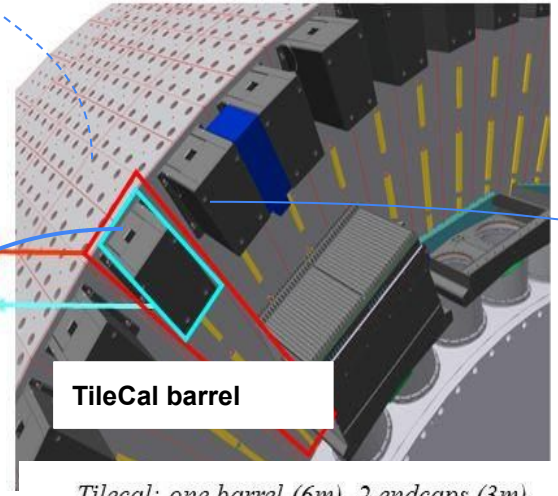




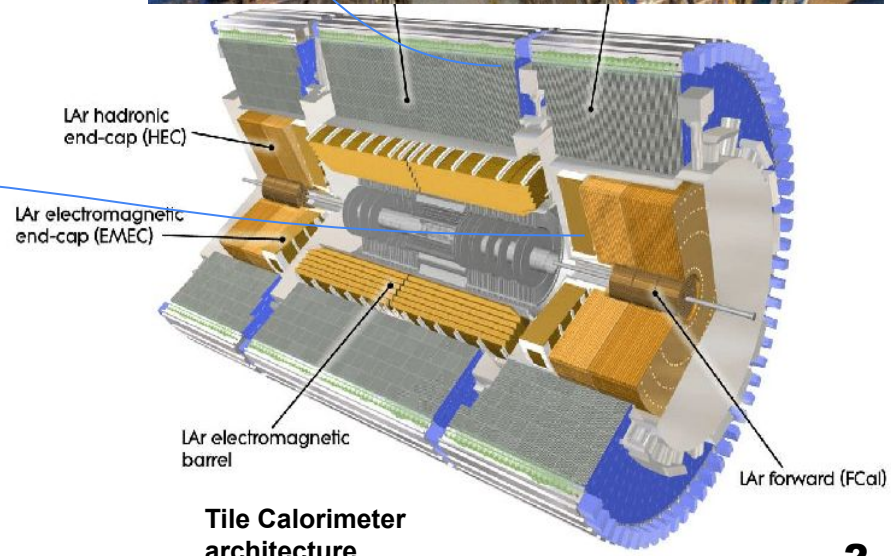




ATLAS detector



Tilecal: one barrel (6m), 2 endcaps (3m).
- 256 drawers with front end electronics.
- 256 power supplies, 300W each.



Tile Calorimeter architecture

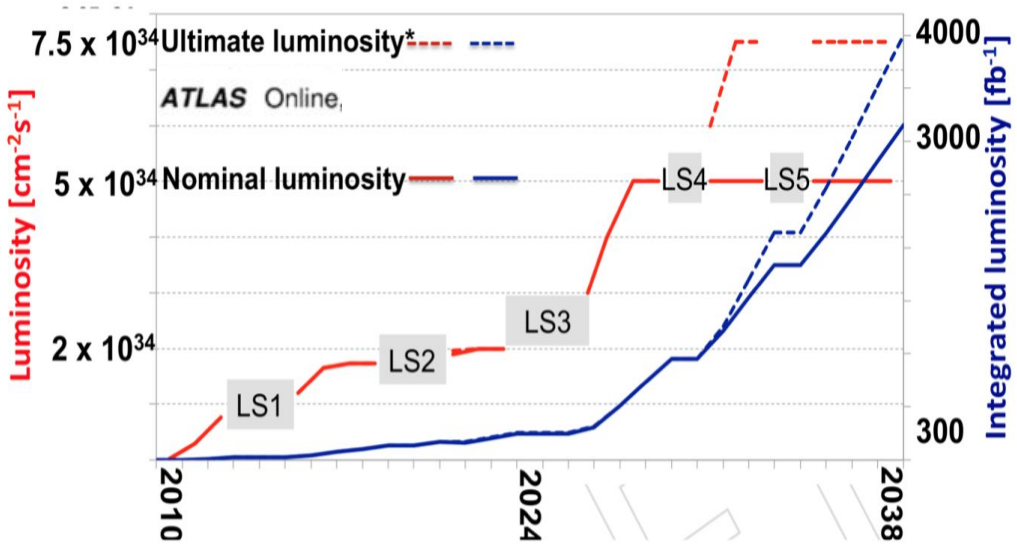
TileCal LVPS Redesign Project

Redesign project

- Community working on replacing all readout electronics because of long-term reliability with increased luminosity

- Involves replacing all electronics and increasing the radiation hardness for handling a maximum total integrated radiation dose ~400 Gy of TID, 4 x 10^{12} n/cm^2 of NIEL and 2.5 x 10^{12} p/cm^2 of SEE estimated over 15 years of operation.

- Require efficient, low-ripple, stable and reliable with the increased luminosity



Features:

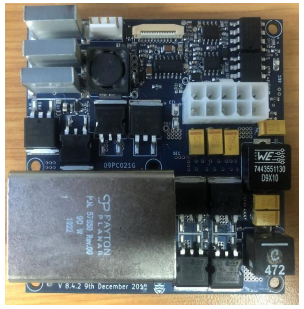
- Customly built, compact,
- Water cooled using Al_2O_3 components ;
- 10 V Bricks, 2.3 A
- Environment: Magnetic field; Radiation tolerant
- Efficiency target: 75%

Reliability is important, difficult access to detector!

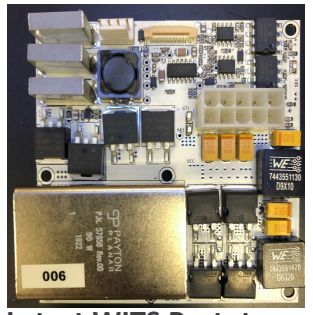
Original Bricks to latest design

6.5.1 Original Brick

v 7.5 ANL brick



Old 8.1.0 WITS Prototype



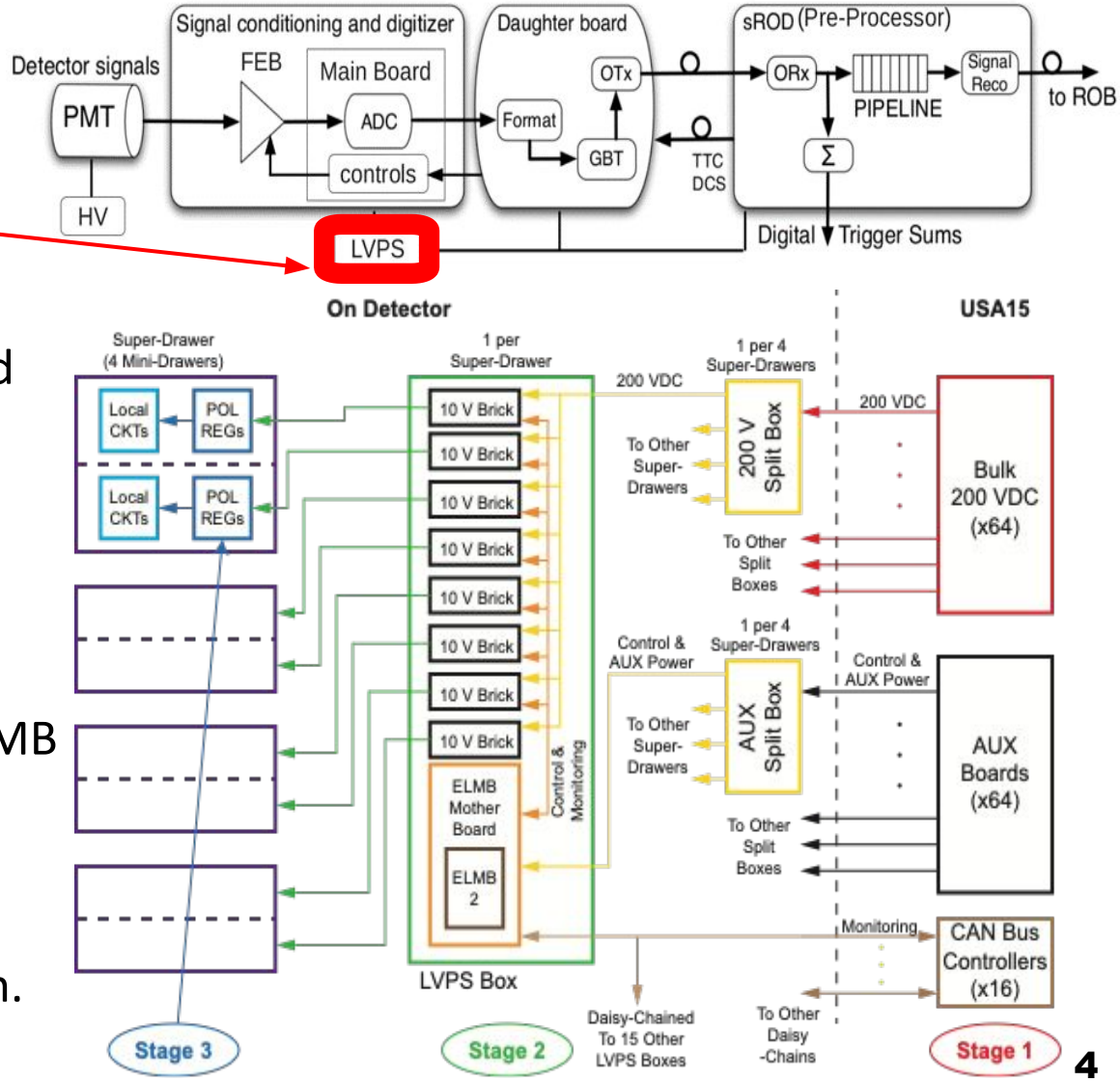
Latest WITS Prototype 8.4.2

1. ATLAS Tile Calorimeter Phase-II Upgrade Technical Design Report : https://cds.cern.ch/record/2302628/
2. Upgrade of Tile Calorimeter of the ATLAS Detector for the High Luminosity LHC Journal of Physics, DOI:10.1088/1742-6596/928/1/012024,2017.

Power and Read out Architecture

Number of power stages that will do the job?

- Upgrade from a ***2-stage to 3-stage*** power powering system distribution system to accommodate the FE upgrades.
  - Front-end power supplies all ± 10V
  - New: Point-of-load regulators
- Converts **200 V DC** to **10 V** DC to provide power to front-end electronics.
- All eight power supplies have the same **specifications** and **performance** requirements.
- LVPS monitoring system is still in progress but will utilize ELMB (**Embedded local monitoring board**) for control and monitoring of individual brick.
- LVPS's represent a **single point failure** in the readout system. i.e. – loss of data from a module.



Radiation Criteria: ATLAS Radiation Policy

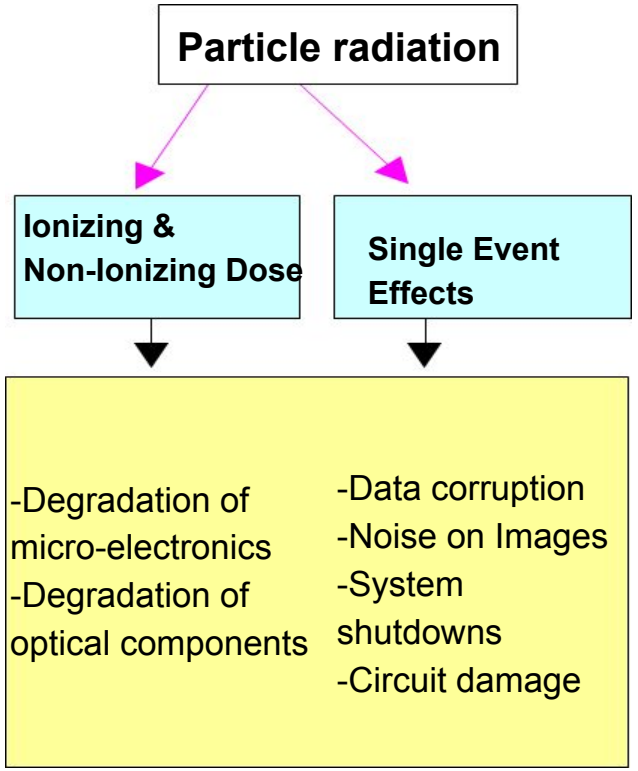
- **ATLAS Extraction Tool** enables to locate the highest irradiated area, close to the edges of the Tilecal Long Barrel
- Safety factors are introduced by the ATLAS Electronics Coordination Group as specified in Table below to account for error margins associated with the different types of radiation tests.
- Safety Factors: SF_{sim} (Safety Factor on the simulation giving the Doses or Fluences) and SF_{lot} (Safety Factor corresponding to the variation from lot to lot of components)
- **General guidelines** for radiation testing for ATLAS specify that 10 units be tested with actual load[3].
- An **active measurement** of the response of the Bricks and components under irradiation was desired, thus a reasonable time period to search for any detrimental effects was chosen to be 30 minutes

Radiation Type	Location	Simulated Dose/ Fluence	SF_{sim}	SF_{lot}	Target Dose/ Fluence
TID [Gy]	Barrel	53.6	1.5	5	(321)
	End-caps	34.3	1.5	5	(206)
SEE [p/cm$_2$]	Barrel	5.3×10^{11}	1.5	2	4.24×10^{12}
	End-caps	9.8×10^{10}	1.5	2	7.84×10^{11}

3. ATLAS Radiation Policy: https://inspirehep.net/literature/1195265

Radiation Testing: Component-Level tests

- **Component-level tests** of single batch to find candidates with
  - No/acceptable degradation with Total Ionizing Dose (TID) & Neutron Ionizing event loss (NIEL)
  - As well as no catastrophic failures due to Single Event Effects (SEE)
- **Challenges**
  - Huge number of (active) components to test and additional requirements i.e single lot components
  - Large variations in test conditions vs operating conditions
  - Availability of test facilities used for radiation testing of bricks: proton beams, gamma irradiation



- **Radiation testing** for SEE/TID performed (***Focus of presentation***) at Proton Irradiation Facility, PSI, Switzerland

Radiation testing is time and resource intensive,
Try optimize and reuse already tested components from older designs

Radiation Testing: Component-Level tests

There are two types of SEEs: non-destructive and destructive:

- Non-destructive, or soft, SEEs can be recovered by a system reset, re-programming/re-configuring the device or reprocessing of affected data.
- When a device fails, destructive or hard SEEs occur, resulting in lasting device or system damage.

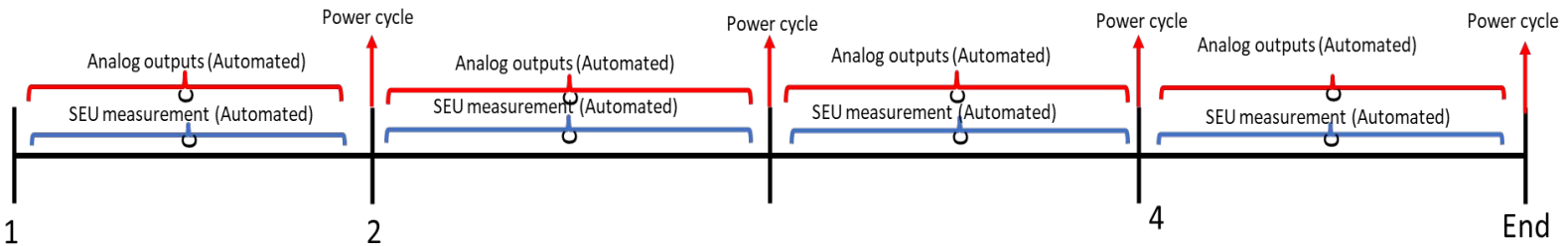
The components that were tested:

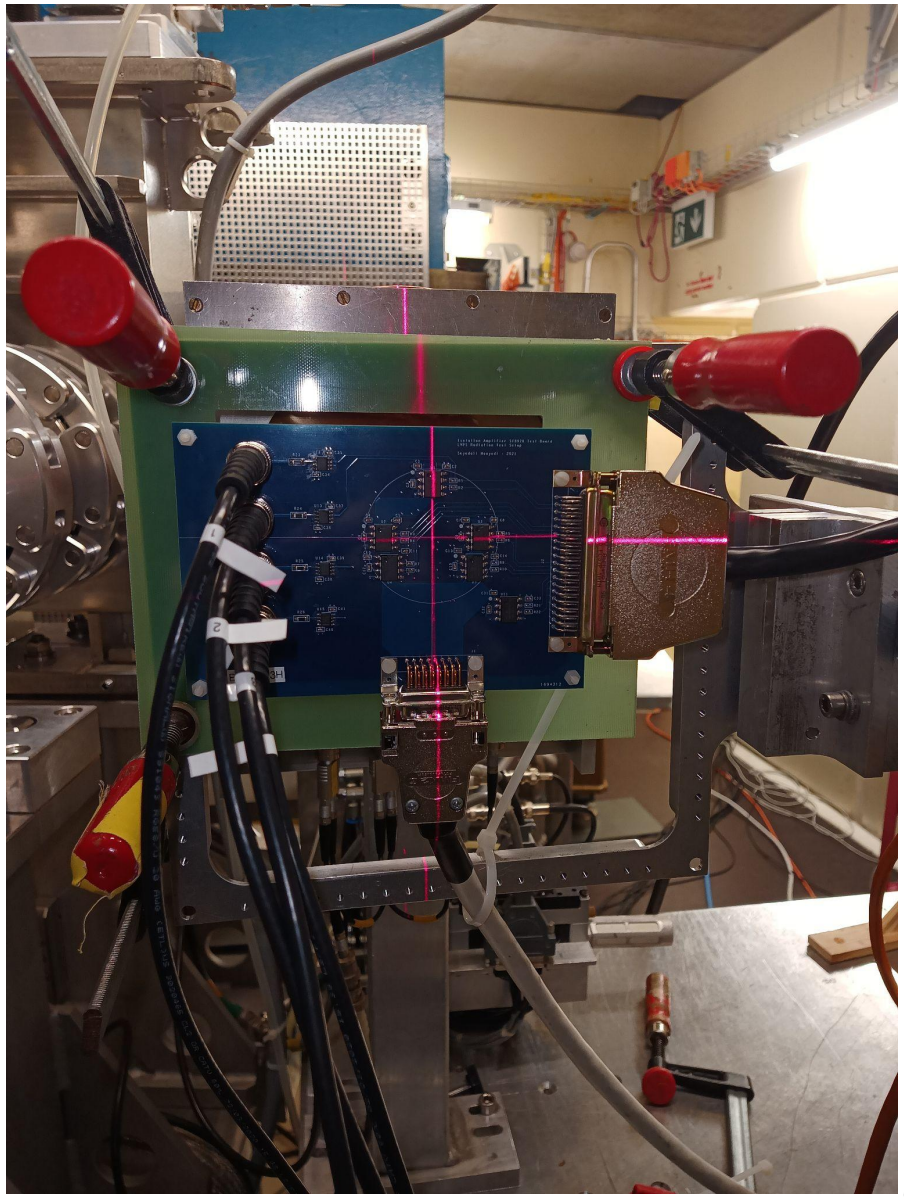
- **IR2110** MOSFET driver (10 pieces radiated + 1 reference piece all from the same batch)
- **SIHFS9N60A** MOSFET (16 pieces radiated + 4 reference pieces all from the same batch)
- **SI8920BC-IP** isolation amplifier (30 pieces radiated + 3 reference pieces from 3 batches) - *First results on presentation*

Component	Part number	Required dose (Gy)	Board tested
Power MOSFET	SIHFS9N60A-GE3	200	2
MOSFET driver	IR2110	200	1
Isolation amplifier	SI8920	400	3

Experimental set-up: Component-Level tests

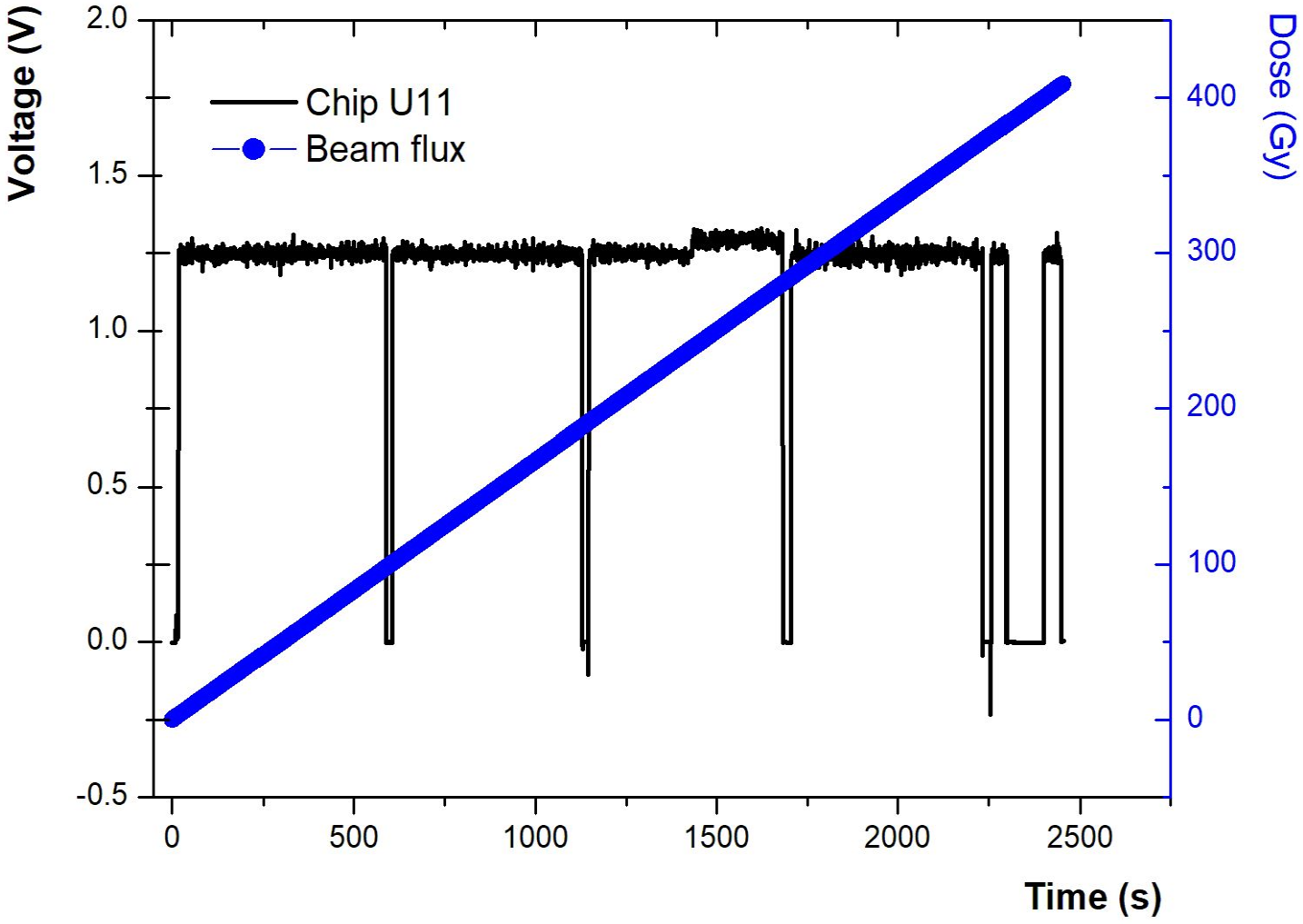
- The tests were performed with **200 MeV** proton beam with a flux of 3.5 x 10^8 p/cm^2/s
- Each board was tested for around 30 minutes to reach 6.47 x 10^{11} p/cm^2 (equivalent to 400 Gy)
- The chip has a fixed gain of 8.1, and by setting an input voltage of 0.15 V on all the chips, we expected to have an output voltage of 1.22 V
- All the 11 output voltages were being read by DAQ, and the output voltages of two of the chips (Chip #2 and Chip #10) were connected to a scope to see possible SETs.
- The result will only focus on the SI8920 Isolation amplifier





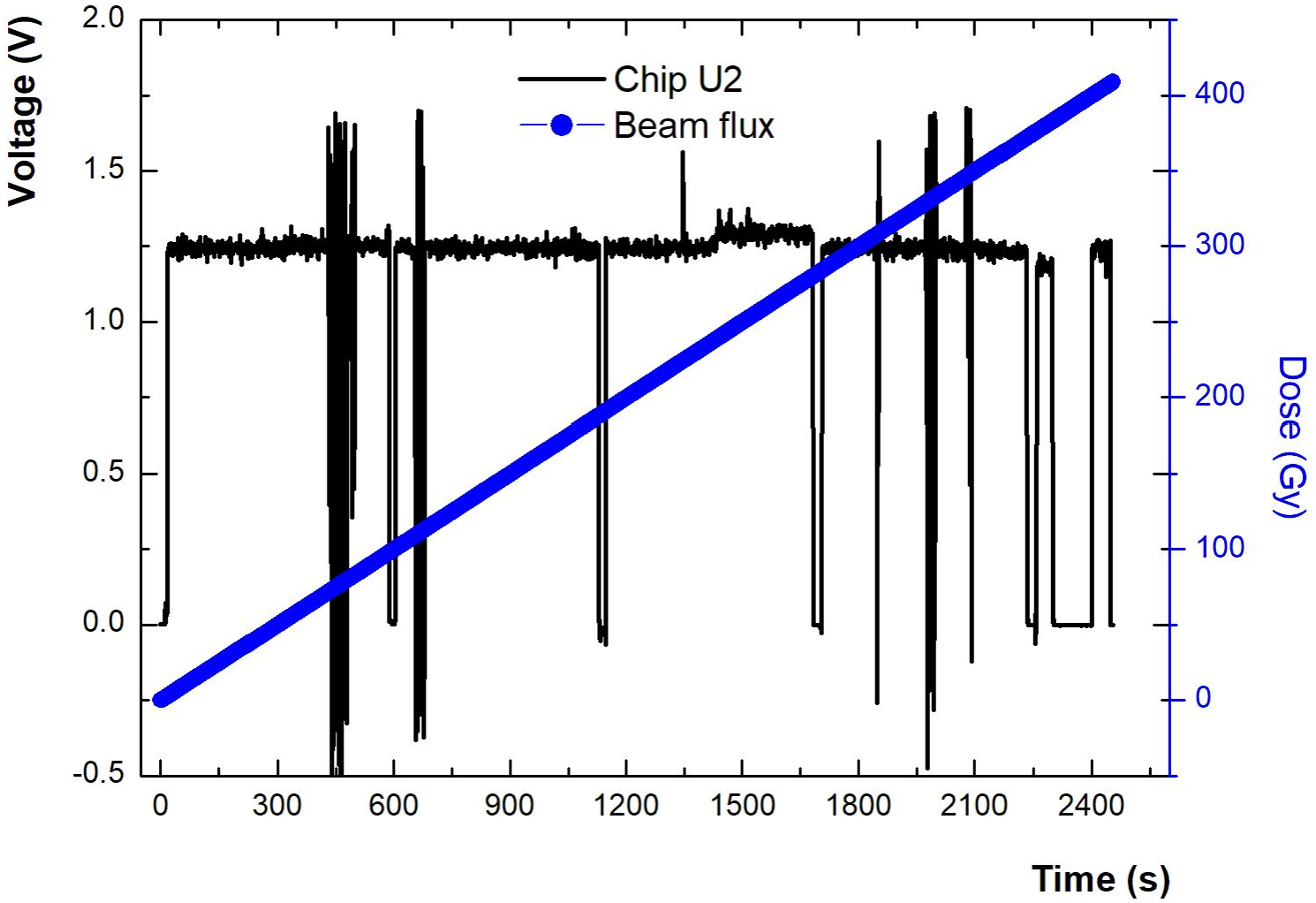
Latest Results: Component-Level tests

- The tests were performed in 4 runs, and there were a power cycle between each two consecutive runs
- There were also two power cycles at the end of the tests, just to see if any of the faulty chips will behave correctly after power cycle, or if any working chip will continue to work
- The results from the reference chip (chip #11) shows that this chip behaved completely normal during the test



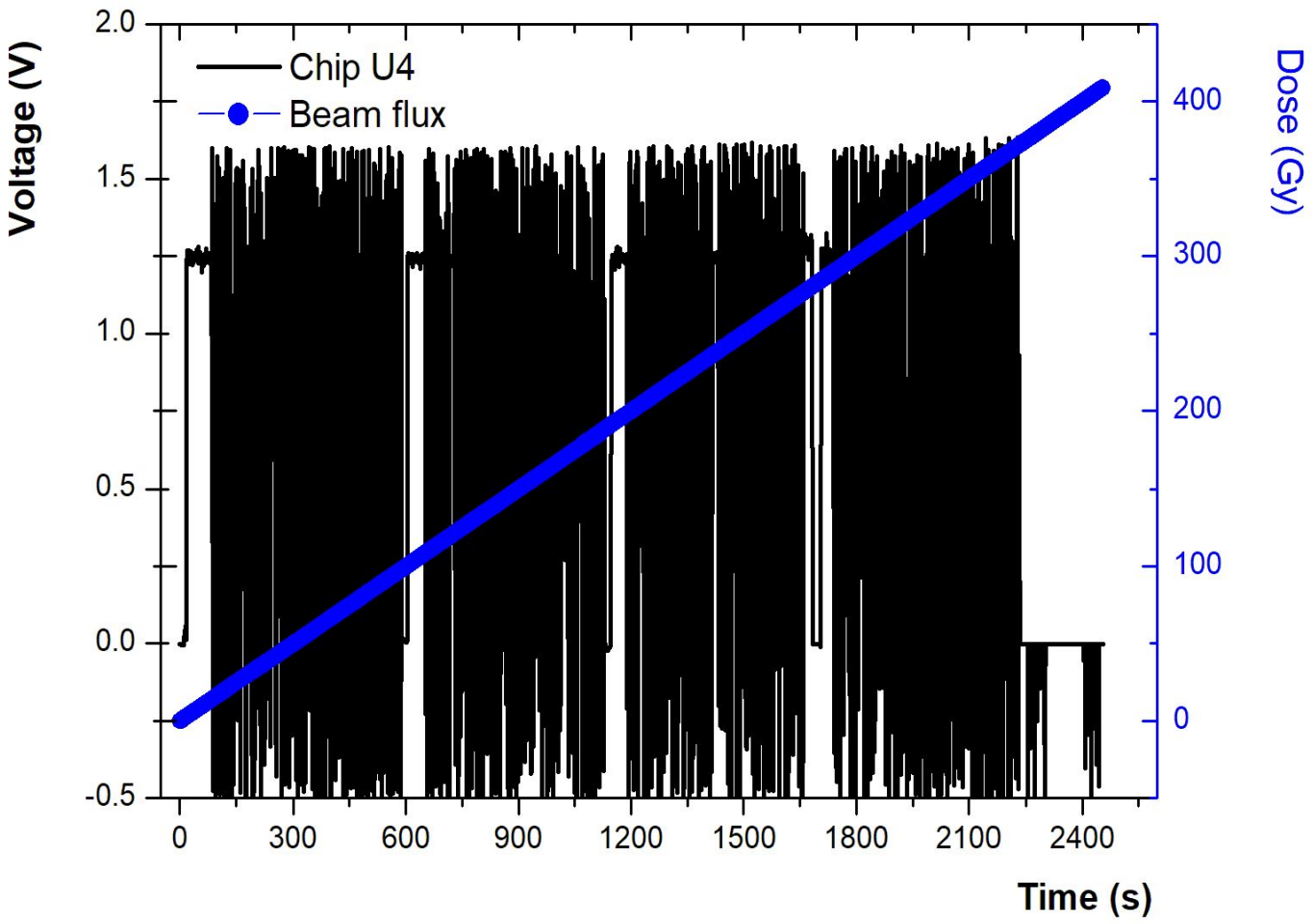
Latest Results: Component-Level tests

- The results from Chip #2 show that this chip almost behaved like the reference chip during the whole test, except for some time during the first, second and fourth runs, where it showed some fluctuations
- The fluctuations from Chip #2 went away without a need to power cycle
- The chip also survived the test after receiving 400 Gy



Latest Results: Component-Level tests

- The results from Chip #4 show that in all of the 5 runs, it goes to an unstable mode, where the output voltage fluctuates a lot
- The fluctuations started almost at the beginning of each run
- The fluctuations did not stop when the beam was stopped at the end of each run (a power cycle was needed)
- After the last run (receiving 400 Gy), the chip stopped working properly (due to TID effects), and even the two power cycles did not fix the issue



Latest Results: Component-Level tests

The MOSFETs were tested for SEEs by connecting the gate to source, and looking for transients on the drain

- ❑ No SEEs were observed
- ❑ The chips still has to be tested for characterization after they are back from PSI

The MOSFET drivers were tested for SEEs and for any possible drift in pulse shapes

- ❑ No SEEs or possible drifts were observed. They will be tested again after arriving at CERN
- ❑ Preliminary results for these two chips are very satisfactory

Component	Part number	Required dose (Gy)	SEE observed
Power MOSFET	SIHFS9N60A-GE3	200	No
MOSFET driver	IR2110	200	No
Isolation amplifier	SI8920	400	Yes (4 out of 10 Chips)

Conclusion

- Re-design of power supply project on track and identified isolation amplifier to be replaced
- For large scale projects, ensure expertise, cooling, testing, schedule before and during a project
- SEE/TID irradiation testing runs occurred without any problems with MOSFET and MOSFET driver chip, however experienced detrimental instabilities with the isolation amplifier chips
- Radiation testing of a new isolation amplifier chip will commence in 2nd Quarter of 2022
- Looking forward to start of Pre-production late 2022

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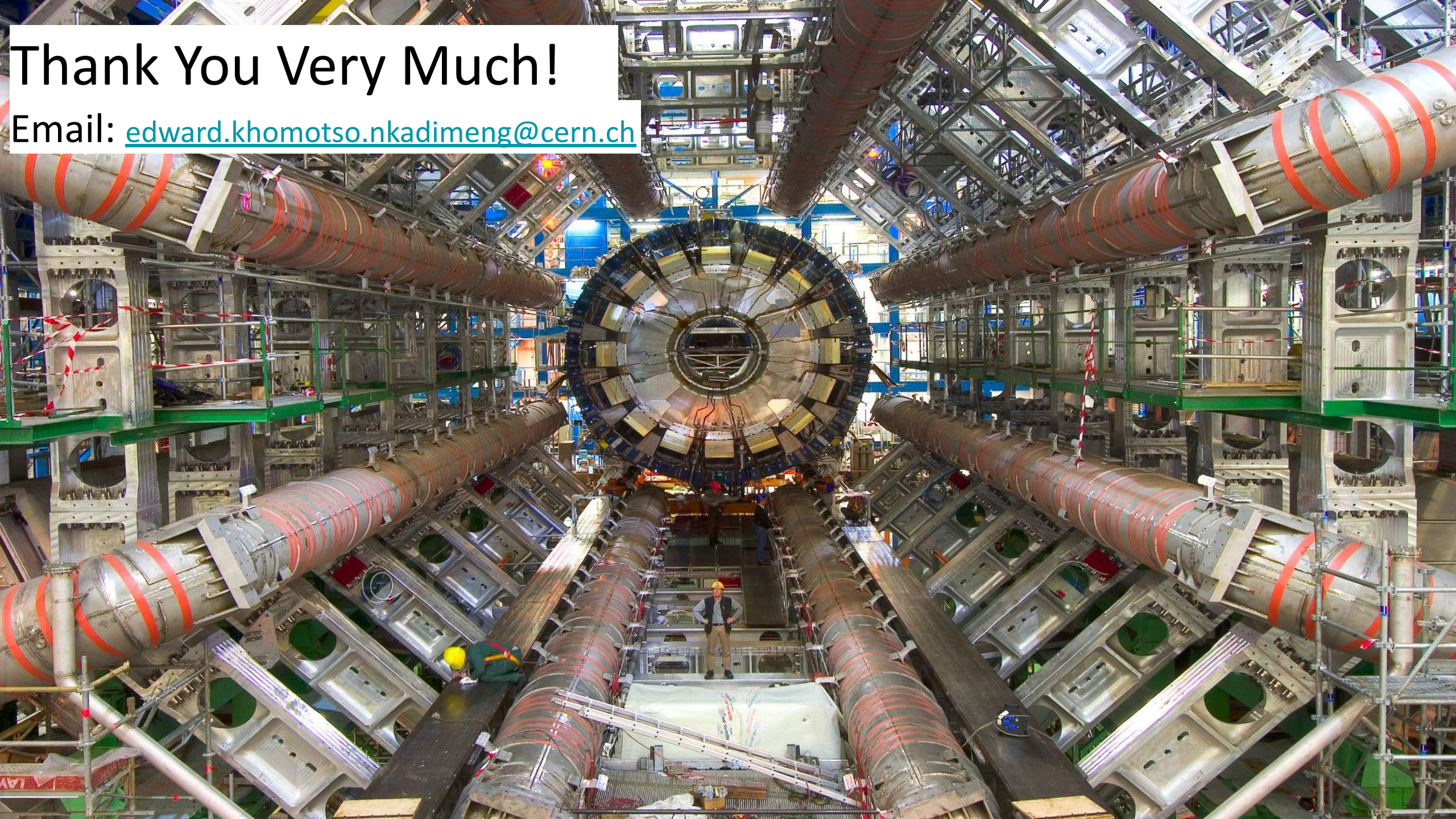
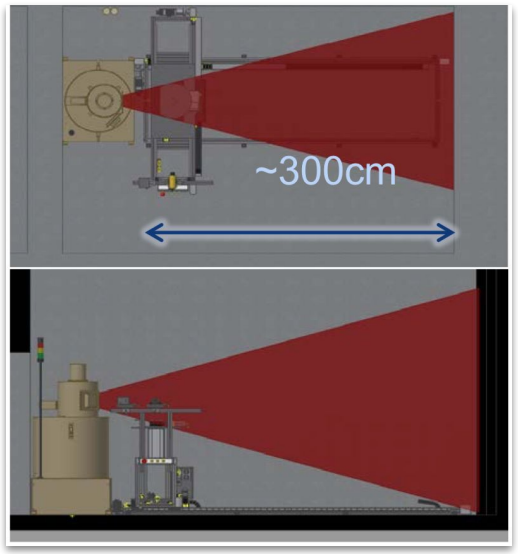


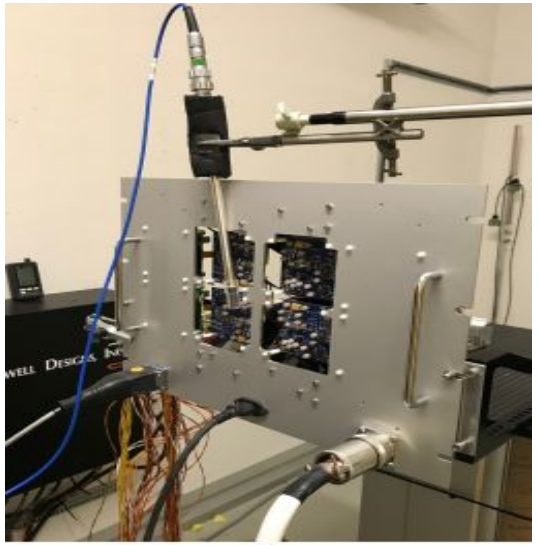
Thank You Very Much!

Email: edward.khomotso.nkadimeng@cern.ch

Radiation testing results: Gamma (CC60 Facility)

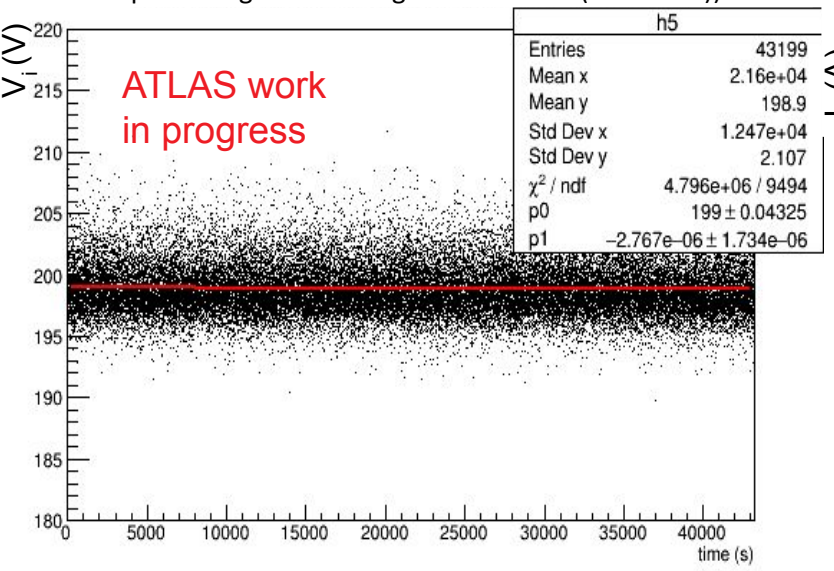
- We tested 8 bricks up to a target dose of close to 500 Gy.
- All the 8 bricks were running monitoring during up to end of the tests with only an output voltage drop of 1 mV/Gy.
- This drop is completely acceptable due to wide range of input voltage for our front end electronics.
- Parameters show expected behaviour as a function of time.



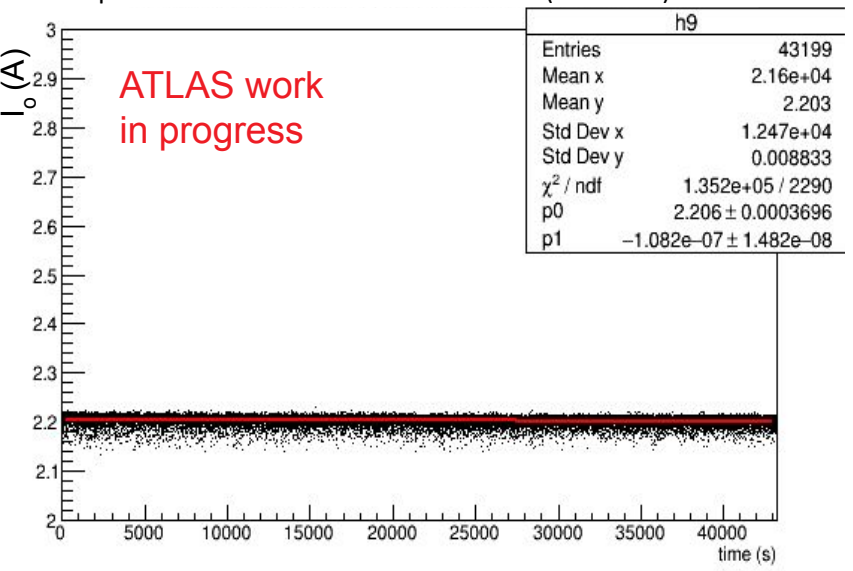


TID tests of LVPS boards in CC60 facility

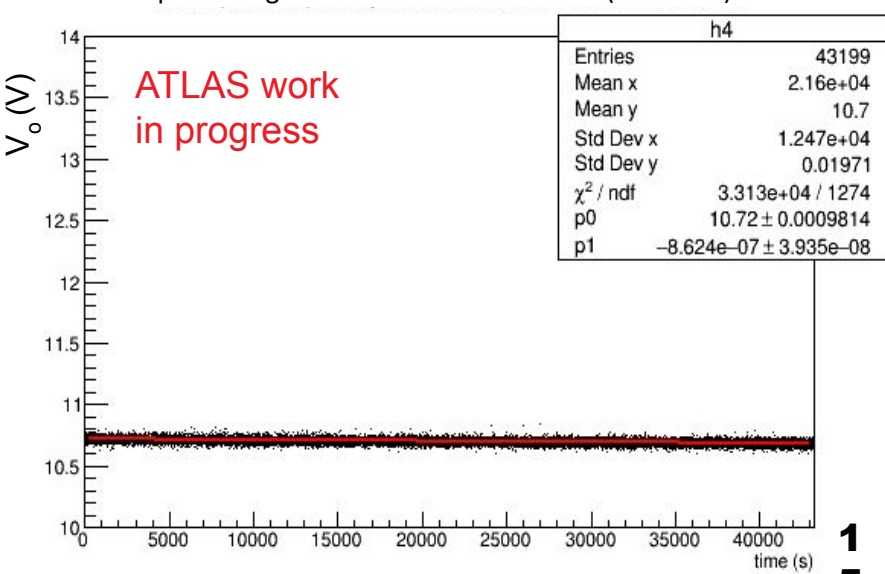
Input Voltage monitoring for LVPS brick (1st 12 hrs))



Output current over time for irradiation (1st 12hrs)

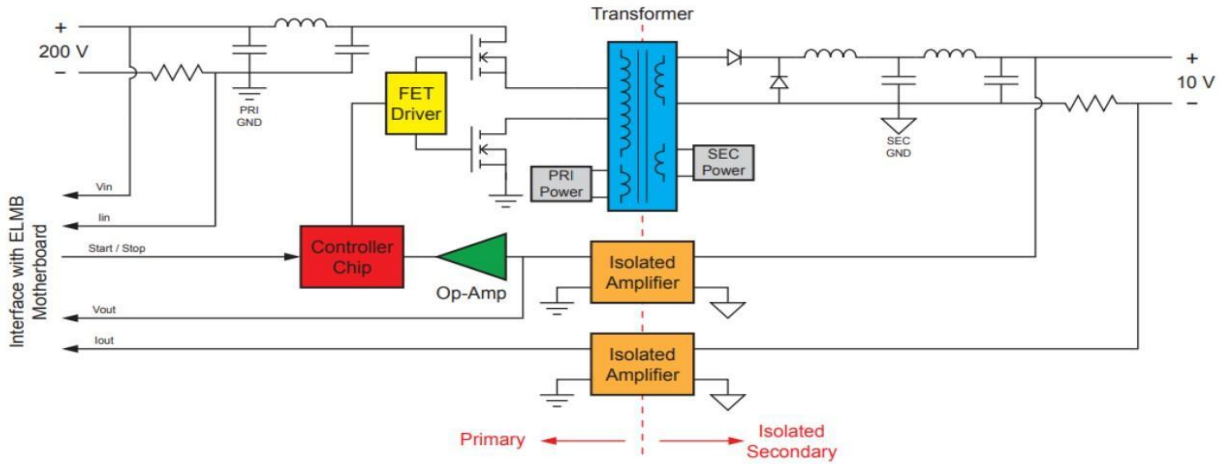


Output Voltage over time for irradiation (1st 12hrs)



Brick principle of operation

- Transformer coupled buck convertor (Forward converter).
- Controller chip **LT1681** (*Heart of design*) is used to provide switching at frequency of ~ 300 kHz



- FET's: When conducting current flows to the primary windings of the transformer which transfers energy to the secondary windings.

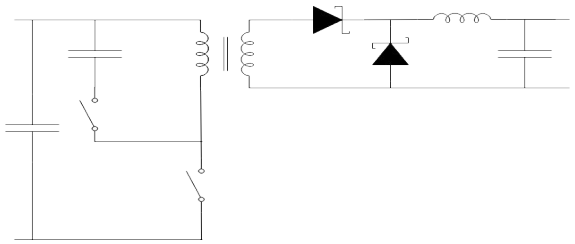
- Opto-Isolators: Provide voltage feedback.
- Shunt Resistor: For measuring the output current.
- Protection circuitry: Overcurrent Protection , Over Voltage Protection, Over Temperature Protection.

Parameter	Value
Threshold for Stable Load	**< 2 A**
Over Voltage Protection	**11.5 – 12.5 V**
Overcurrent Protection	**6.75 – 10.75 A**
Output Voltage Ripple @ NL	**< 0.5 V (p2p)**
Duty Cycle @ NL	**30 – 40 %**
Frequency @ NL	**280 – 320 kHz**
Efficiency @ NL	**> 65%**
Input Power (Current) @ NL	**48 W (0.24 A)**
Output Voltage Change	**< 20 mV/A**
Over Temperature Protection	**70 Degrees C**

Talk to Experts (again); Look at datasheets of similar products

Compile your list of required specifications

From Topology to Components



Power Topology

Simulation

Calculation

Get ALL waveforms (v, i)

Get ALL losses (p)

Radiation Tests

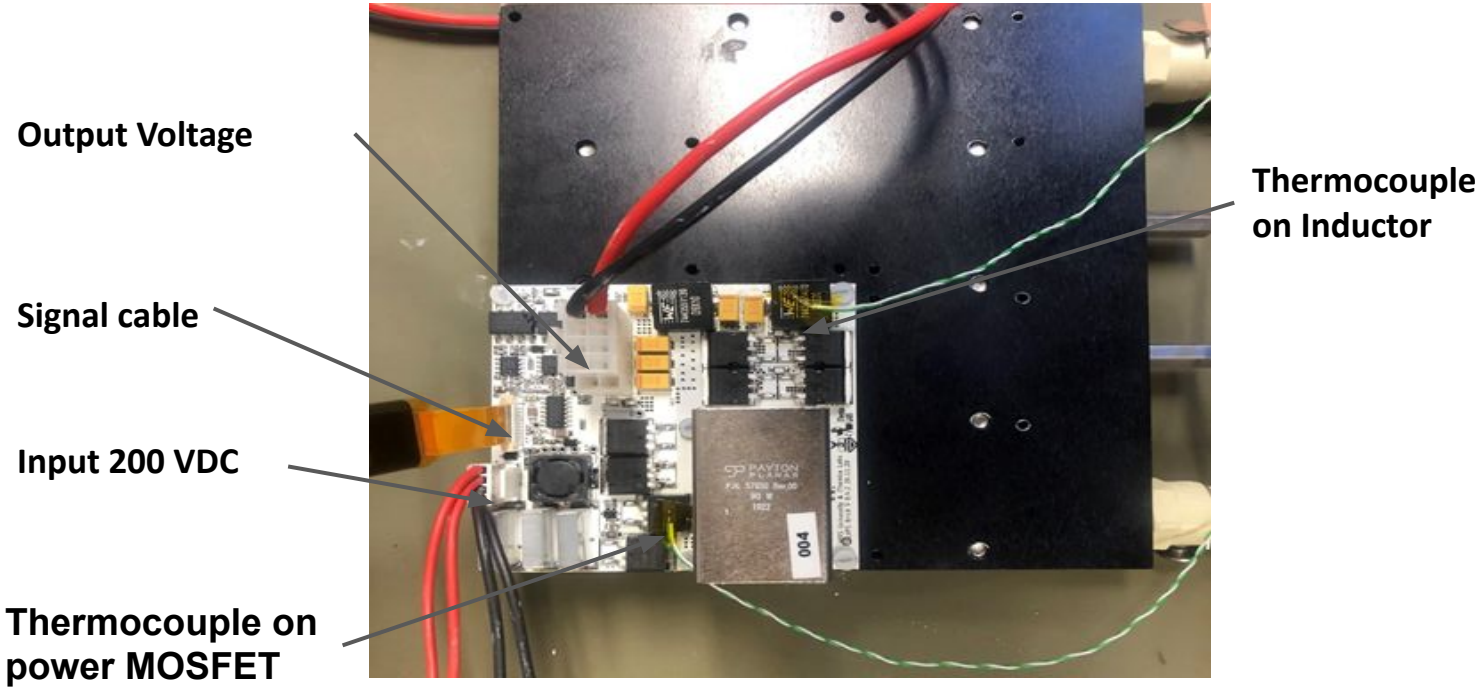
Custom Magnetics

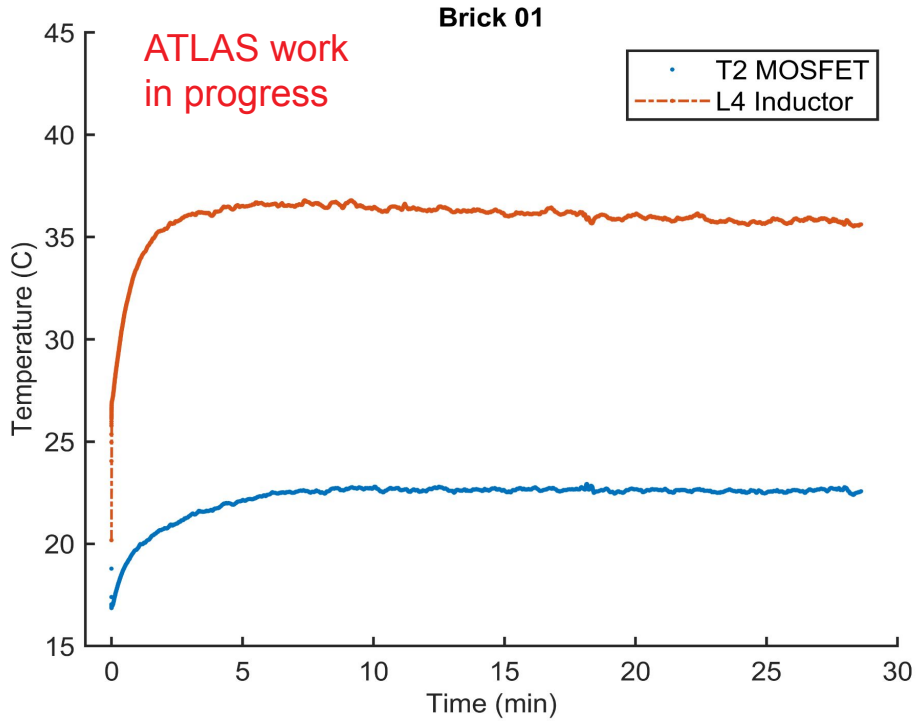
Other Modifications

Choose active and passive components

Monitoring of protection circuitry

- Quality Control test benches developed and operational at Wits High throughput Lab (See talk by Ryan).
- Functions to initiate a trip of the brick if specific operating parameters fall out of a nominal range ensuring isolation of failures.
  - Over Voltage Protection (OVP) trip parameters (11.5 - 12.0 V)
  - Overcurrent Protection (OCP) trip parameters (10.24 - 10.75 A)
  - Over Temperature Protection (OTP) trip parameters (70 ◦C)



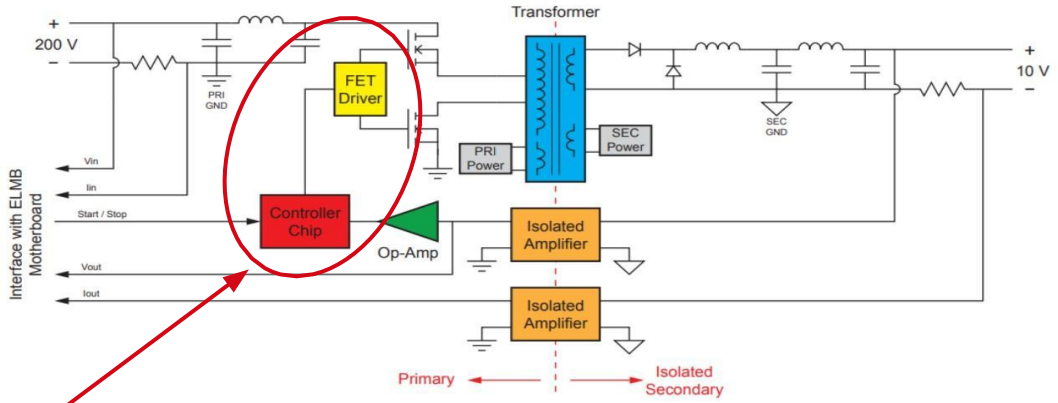


Brick Improvements thus far

Critical Issue: Thermal Management

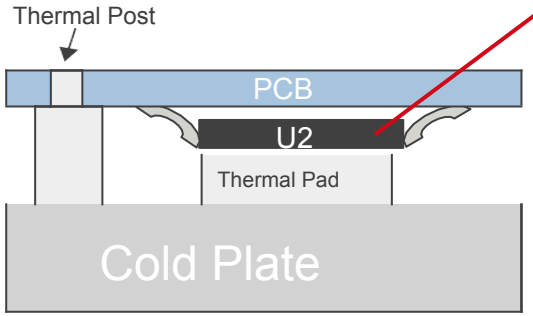
- ***The symptoms:***
  - **Brick experienced high temperatures during operation**
  - ***U1 (controller chip) & U2 (FET driver) had high failure rates***
- ***A possible cause:***
  - ***Insufficient thermal coupling to cold plate***
- ***What we did:***
  - ***New Higher efficiency MOSFET used (To be rad validated). Locally produced Al2O3 (aluminum oxide) ceramic cylinders used***
  - ***Add thermal Bergquist (Gap Pad) to couple chips to cold plate***

Brick Block Diagram

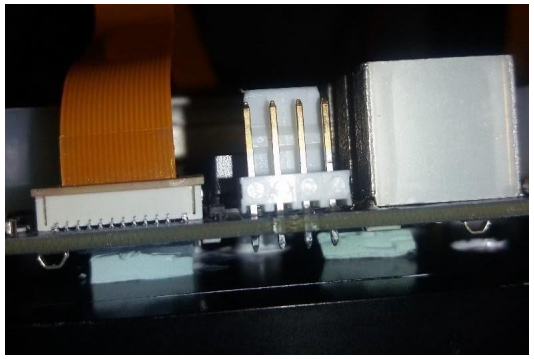


*See Othmane Moune's talk

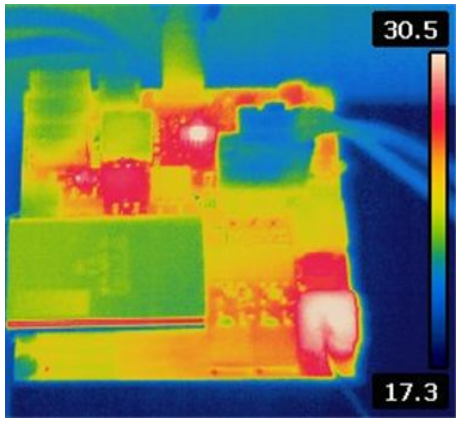
Implementation



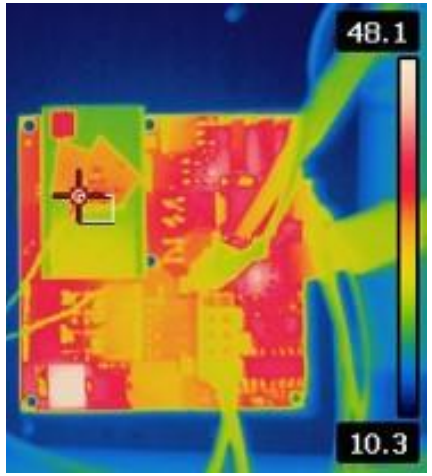
Bergquist Gap Pad 1500S30



New Version 8.4.2 WITS brick



Older v8.1.0 WITS brick



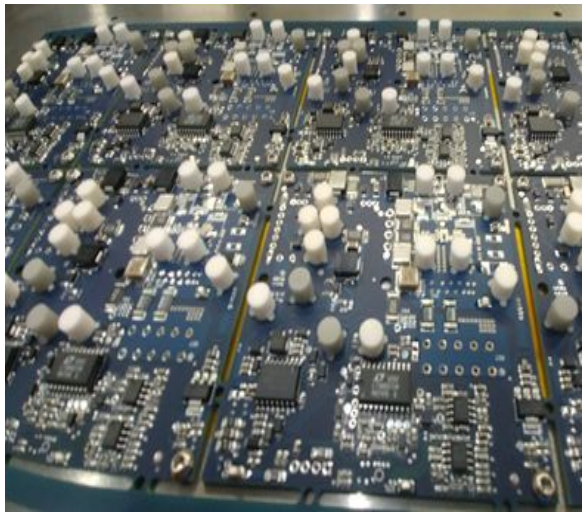
Brick Improvements thus far

Improved Reliability

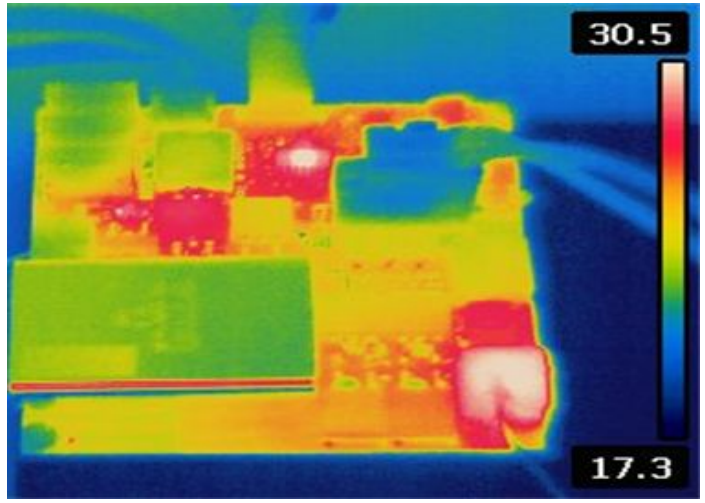
- **Critical Issues**
  - HF Printed circuit boards
  - Reliability studies conducted
  - Better thermal management (Still to be rad validated)
  - Better ESD protection of ICs and Capacitor
- **Medium-Impact Issues**
  - Improved stability
  - Improved trip circuitry
  - Power sequencing
  - Fabrication and soldering quality from supplier
- **Low critical but desirable**
  - Start-up pulse current
  - Improve monitoring circuitry
  - Reduce/improve tuning for final output Voltage

Improved Performance

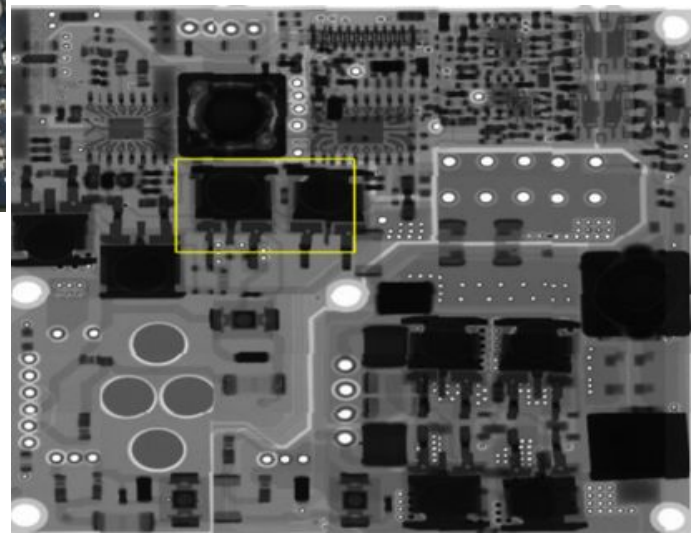
Population of power supplies



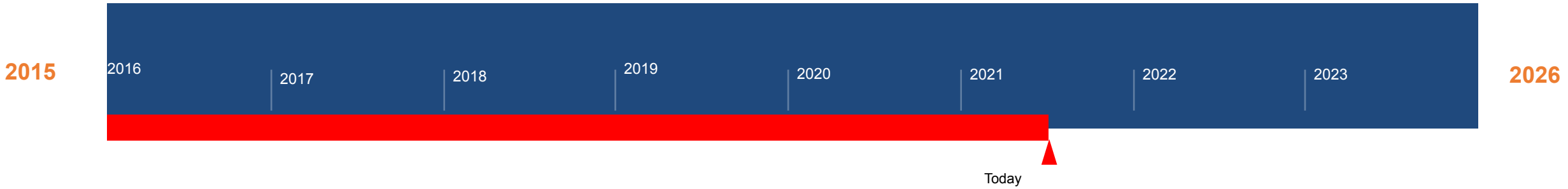
Thermal Image



X-ray Inspection technology



Schedule for LVPS project in SA



SA-Wits LVPS brick design & 1st prototype run	894 days	25 Aug - 28 Jan 2020
Radiation testing, LVPS design and 2nd prototype run. Initial test bench commissioning at Wits	560 days	31 Jul ‘16 - 21 Sep ‘21
Final Design last prototype run and radiation tests	503 days	29 Jan - 31 Dec ‘21
Burn-In Station commissioning	156 days	9 Jan - 13 Jan ‘22
Pre-Production of Bricks	240 days	30 Sept - Dec ‘22
Main Production	175 days	31 Mar - 30 Nov ‘23
Installation	438 days	26 Jan - 30 Sep ‘26

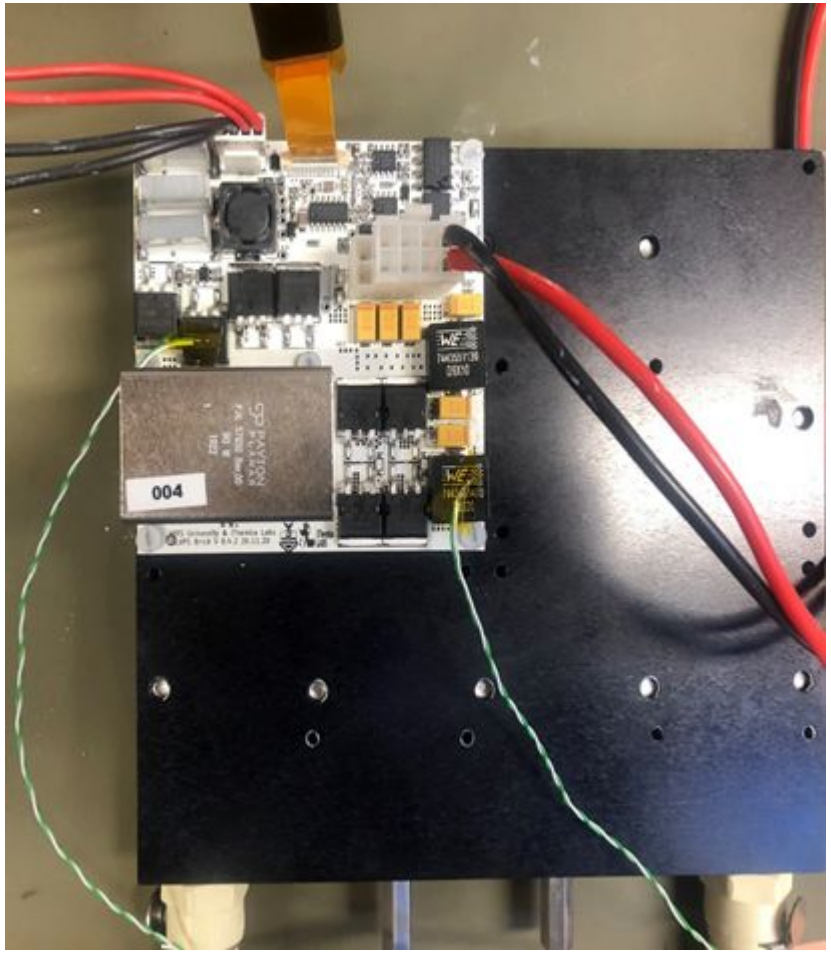
Brick test parameters for thermal testing

Load set = 2.3 A
Cooling station water temperature = 18 °C
Ambient temperature = 24 °C

V(in) = 200.06 V +- 0.01
I(in) = 0.1734 A +- 0.0001
V(out) = 10.9106 V +- 0.001
P(out) = 25.10 W

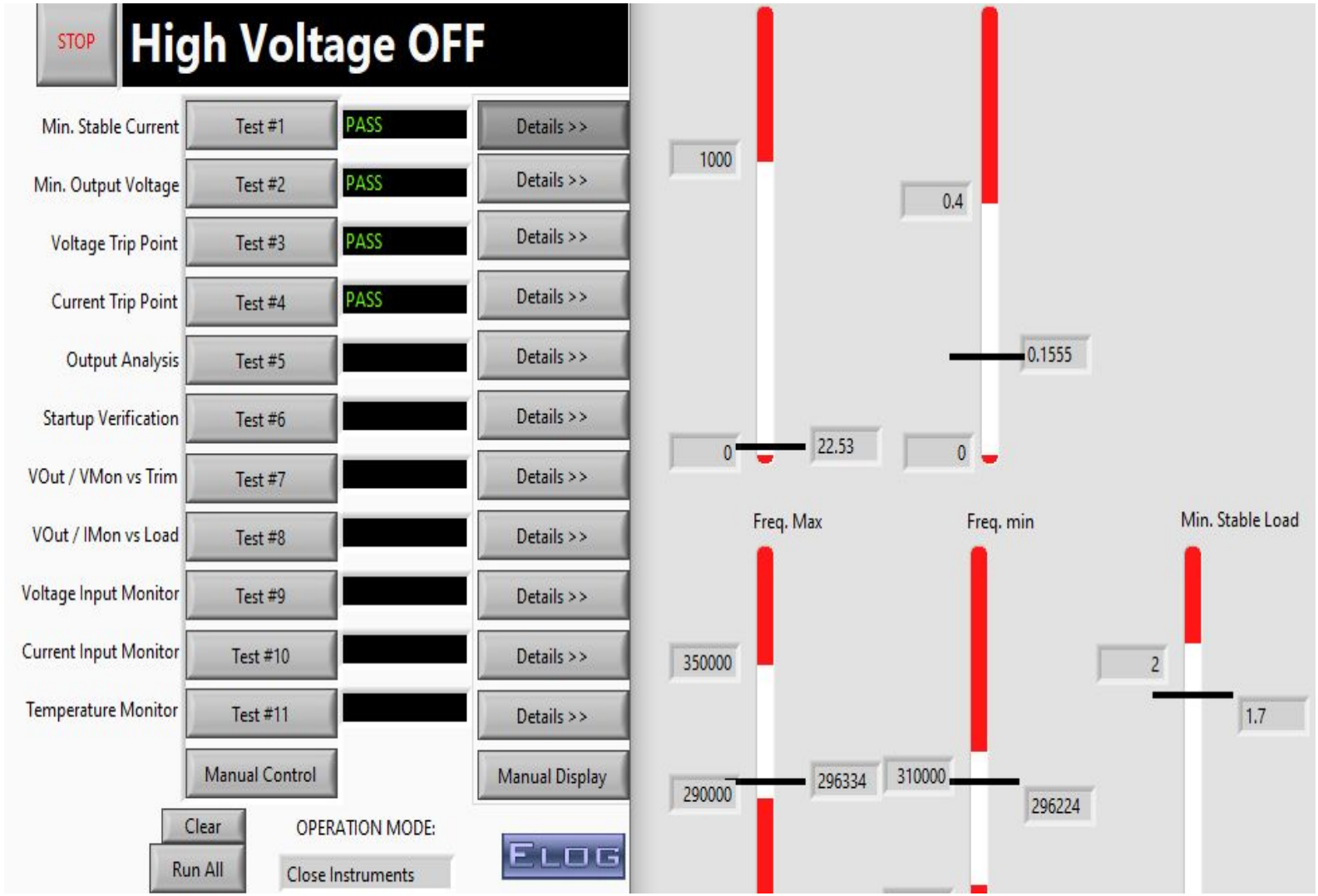
Additions:

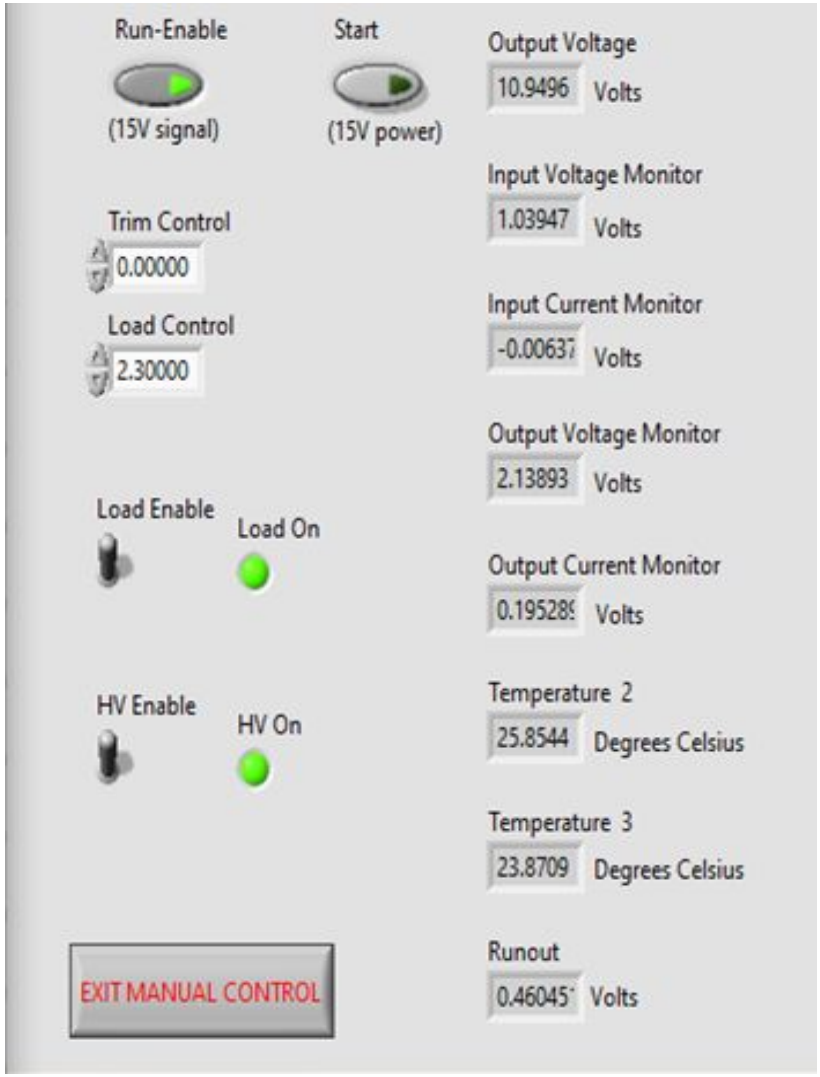
TC1: Attached to T2 MOSFET
TC2: Attached to L4 Inductor
Thermal paste used under Al2O3 posts
Gap Pad® 5000S35 used on LT1681 and IR2110(S)



Testing of prototypes at Wits

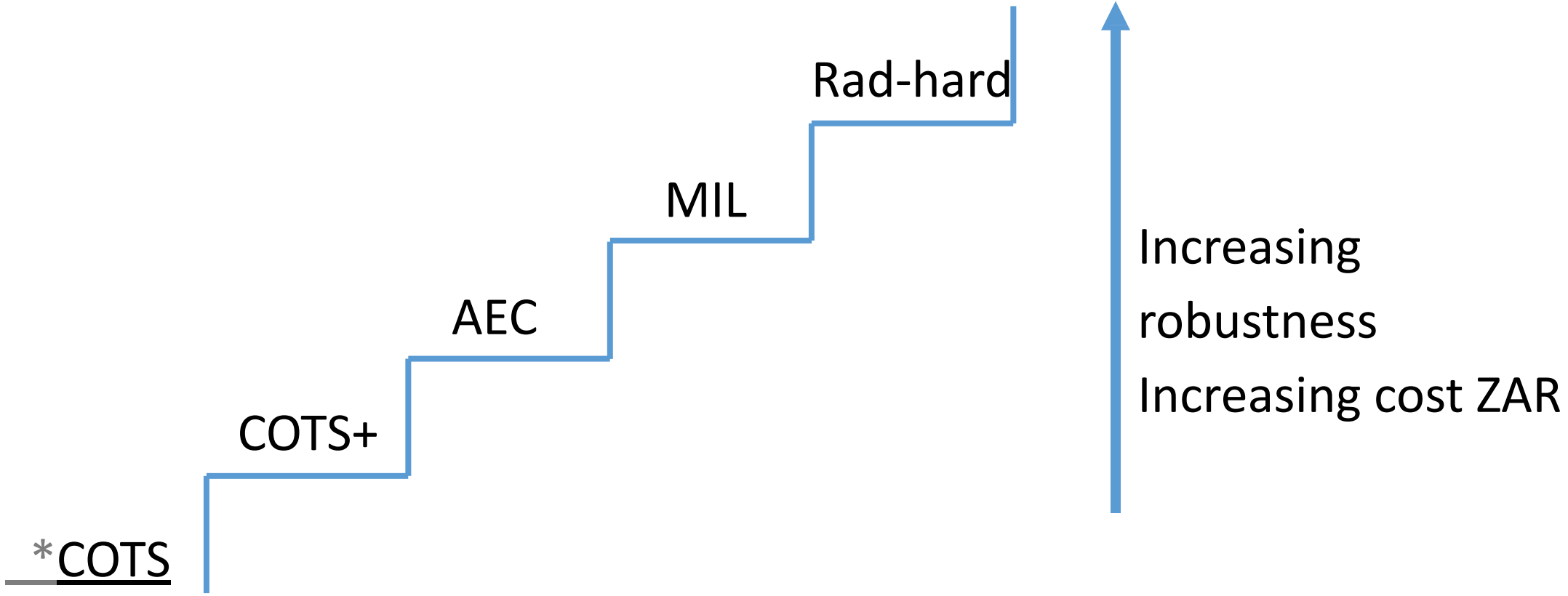
- Bricks were tested and monitored for ~15 minutes on 18/19 May ‘21, and all 8 bricks managed to start without issues.





Premise

COTS = COST Advantage



*Commercial Off-The-Shelf

ICPP LVPS SA team

Front row from left to right: Bruce Mellado, Jacques Klopper, Charles Sandrock, Thabo Lepota, Nkosiphendule Njara, Edward Nkadimeng, Ryan Mckenzie.

Roger Van Rensburg