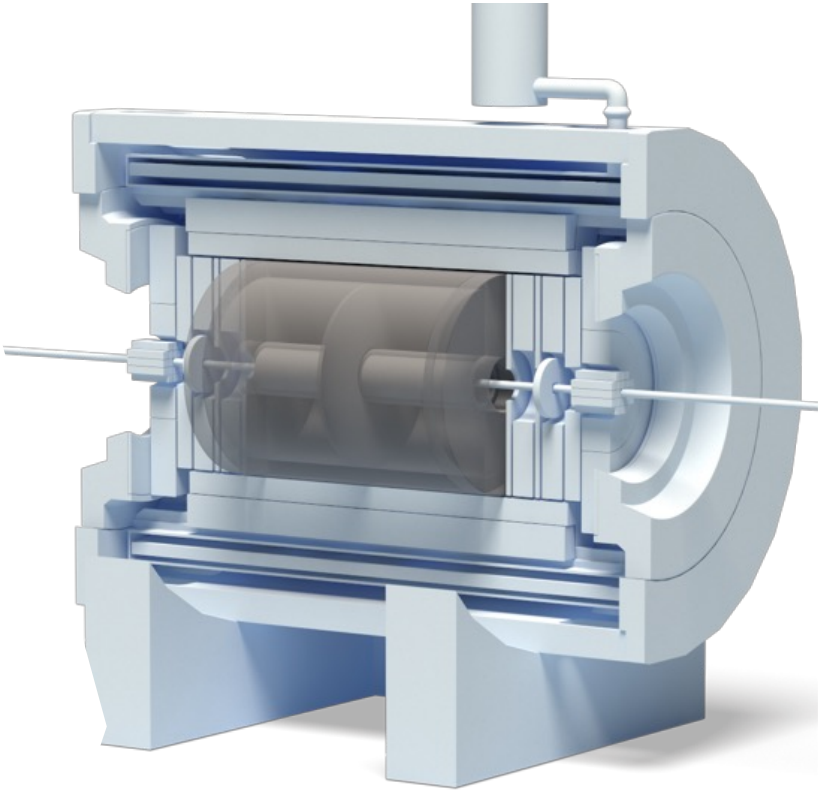
Data acquisition system of the TPC/MPD detector for the NICA project

Stepan Vereschagin, on behalf of the TPC/MPD group, VBLHEP, JINR



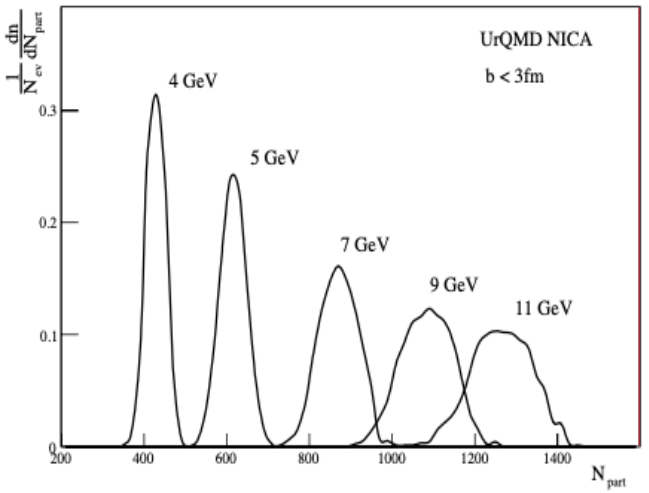
Outline

Nuclotron-based Ion Collider fAcility complex (NICA)

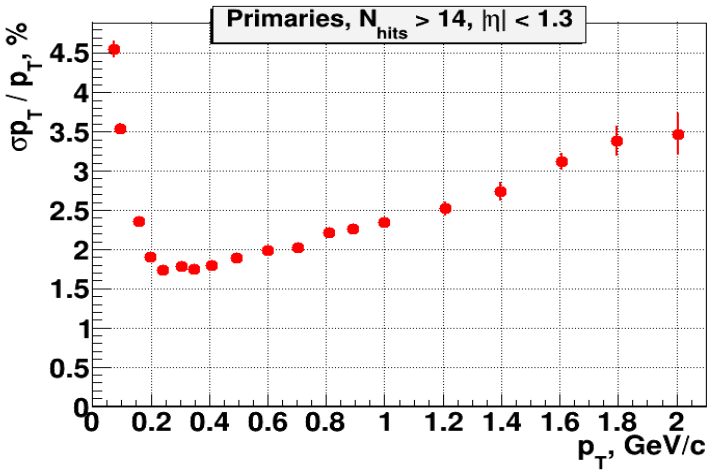
https://nica.jinr.ru/

http://mpd.jinr.ru/

MPD experimental setup

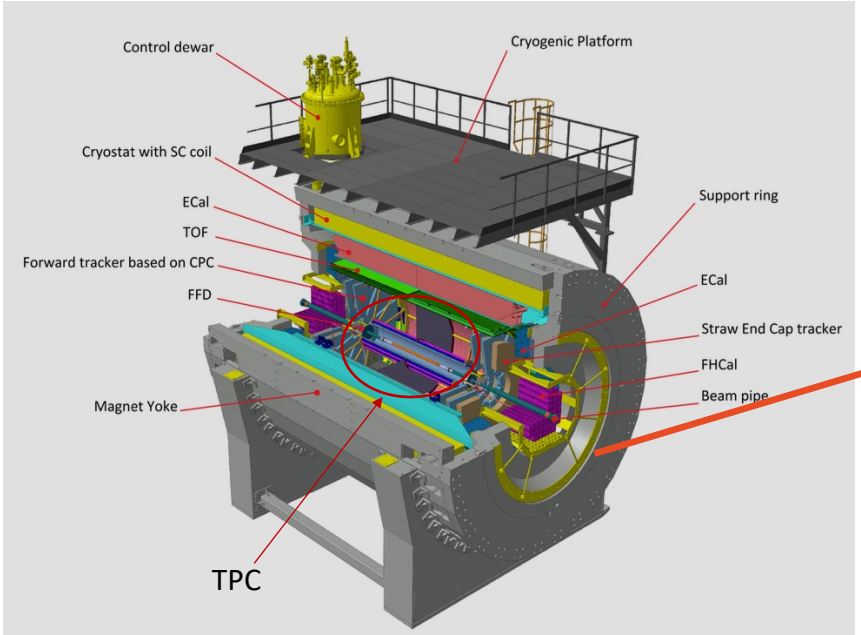


Charged multiplicity distributions in central Au + Au collisions (b < 3 fm) calculated by UrQMD.



Momentum resolution with TPC

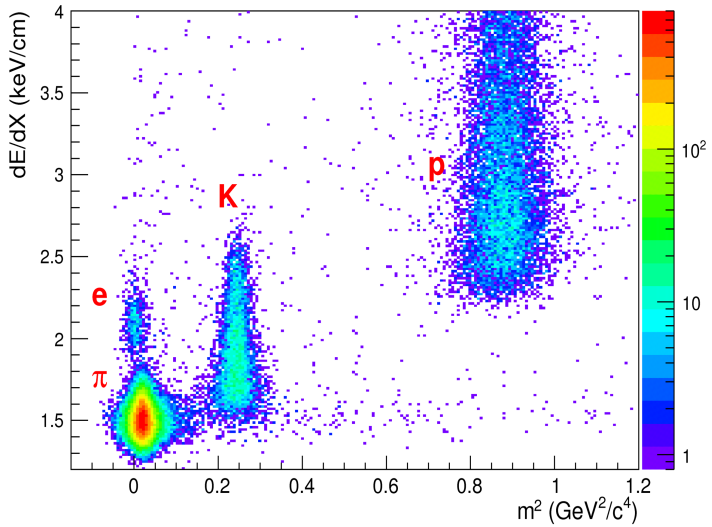
MPD Stage II



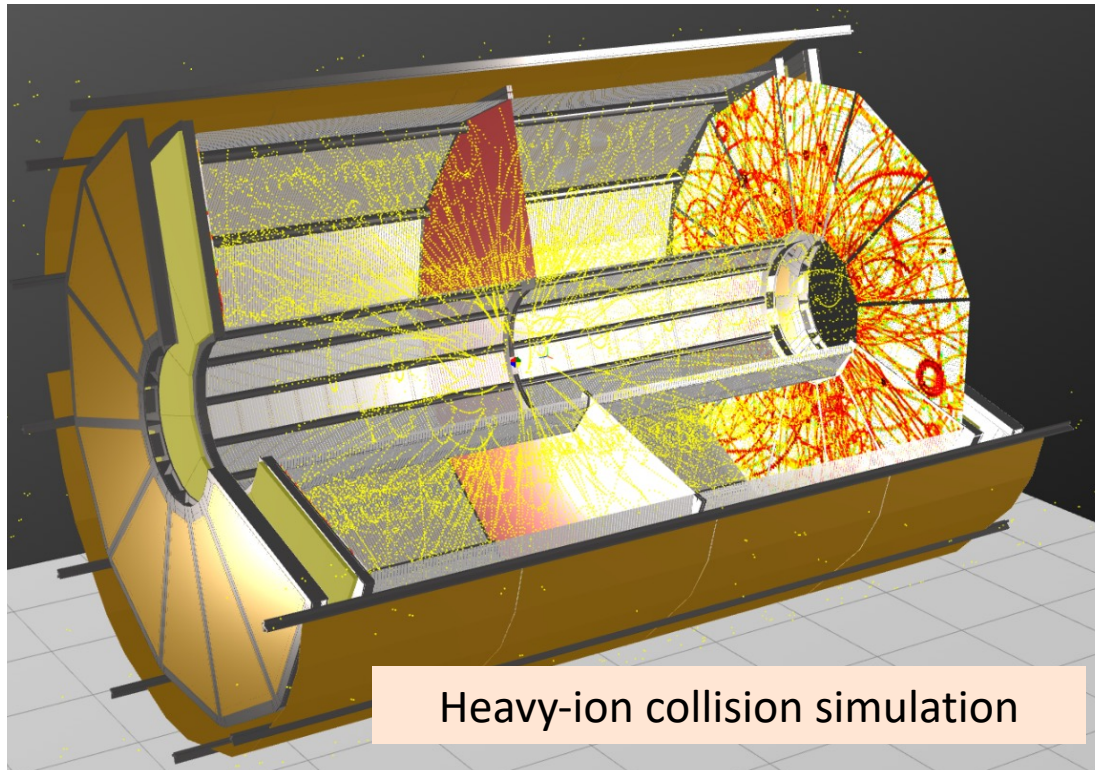
MPD stage I detectors:

- **ECal:** Electromagnetic Calorimeter
- **FFD:** Fast Forward Detector
- **TOF:** Time of Flight system
- **FHCal:** Forward Hadron Calorimeter
- **TPC**: Time Projection Chamber

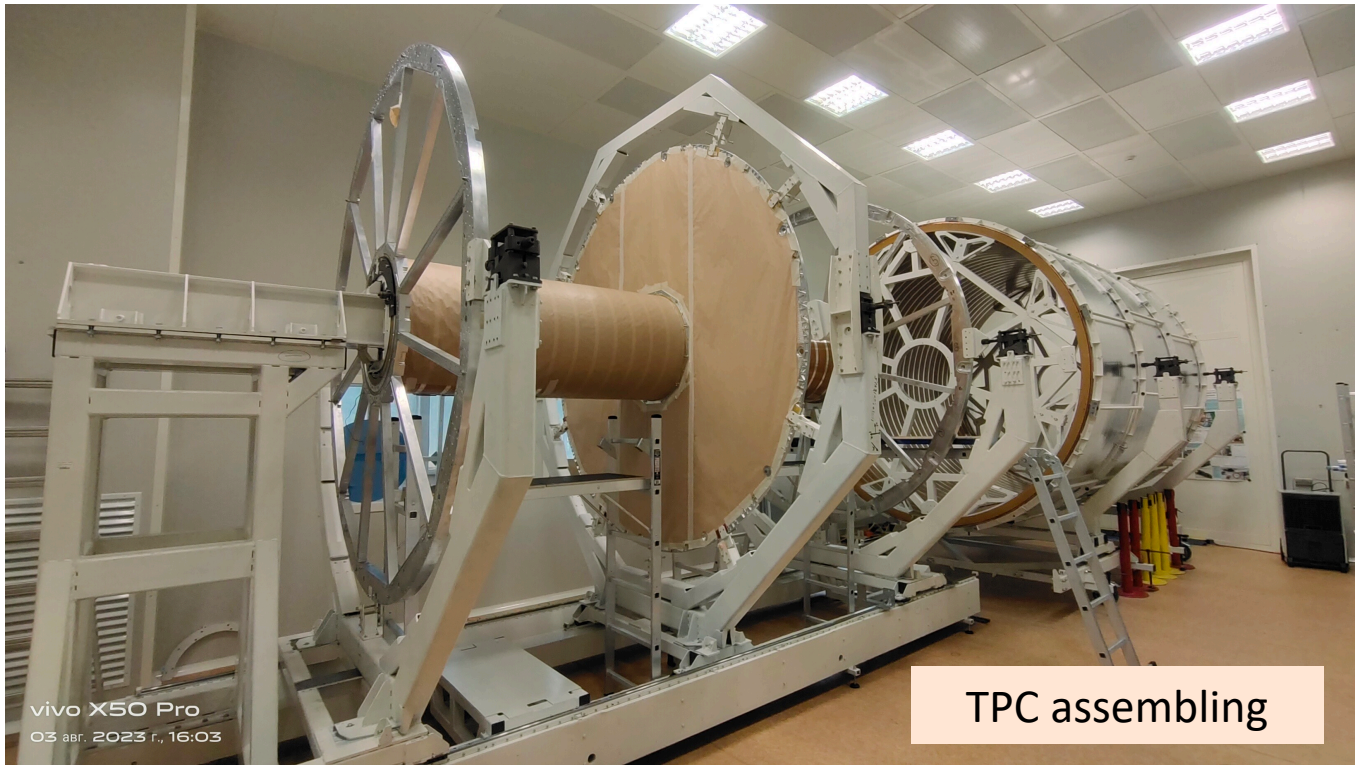
Magnet assembly in the MPD Hall



TPC design requirements



Heavy-ion collision simulation



TPC assembling

The TPC/MPD design requirements:

- The overall acceptance: $\eta < 1.2$
- The momentum resolution for charged particles is under 3% in the transverse momentum range $0.1 < pt < 1$ GeV/c
- Two-track resolution is of about 1 cm
- Hadron and lepton identification by dE/dx measurements: with a resolution better than 8%
- Operation trigger rate: 7 KHz

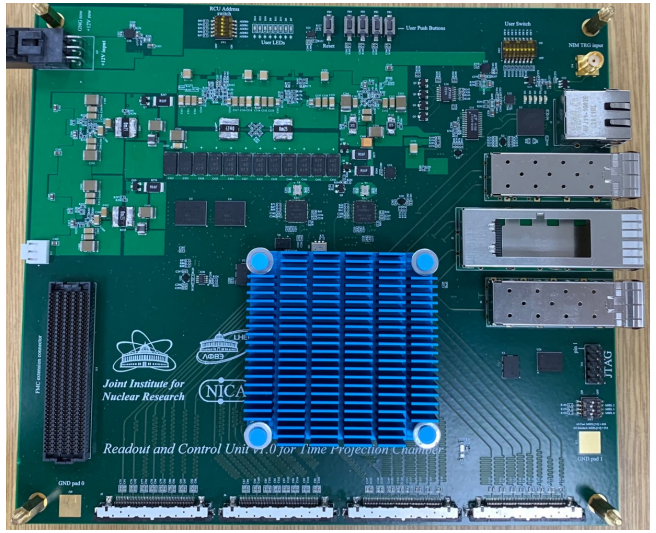
TPC/MPD data acquisition system main parts

Front-End-Cards (**FEC**): 1488 pc., 95 232 10-bit ADCs in total

1488 ×

Readout and Control Units (**RCU**): 24 pc. in total

24 ×



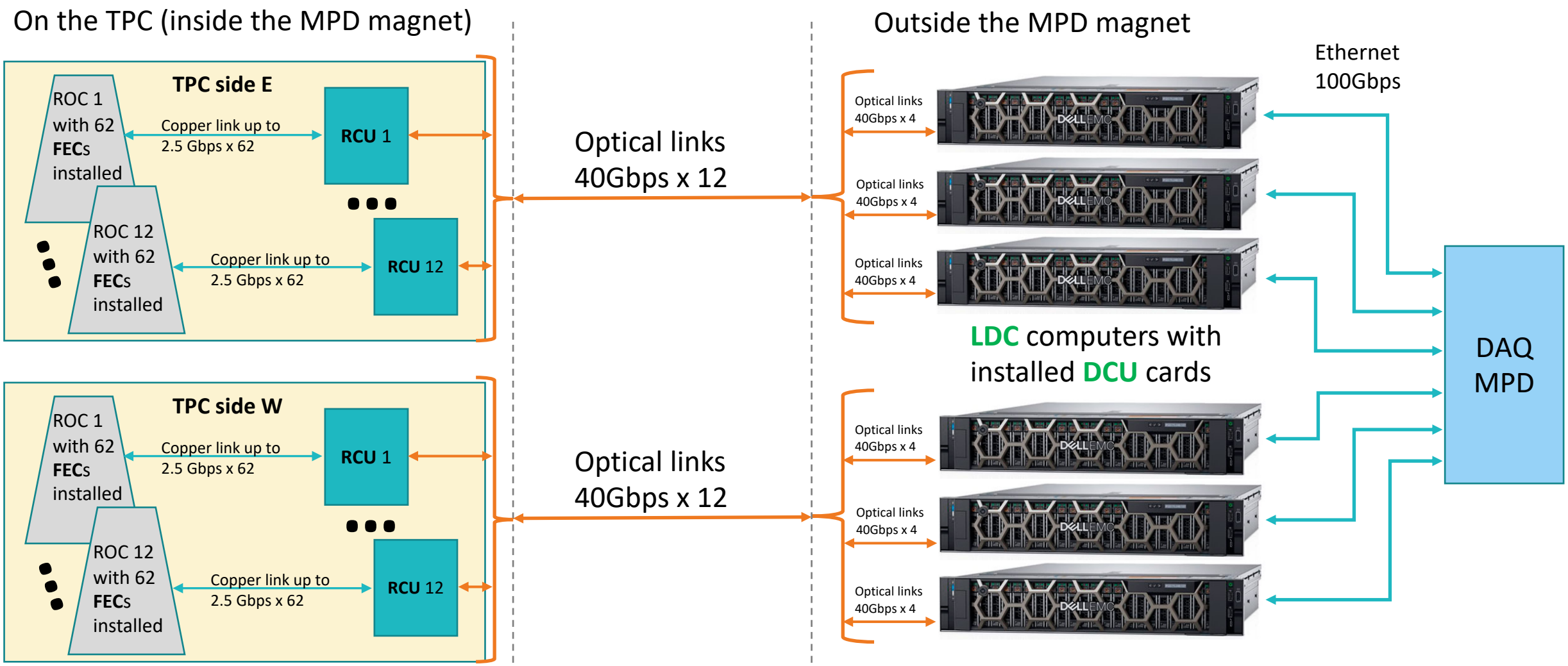
Data Concentrator Units (**DCU**): 6 pc. in total

6 ×

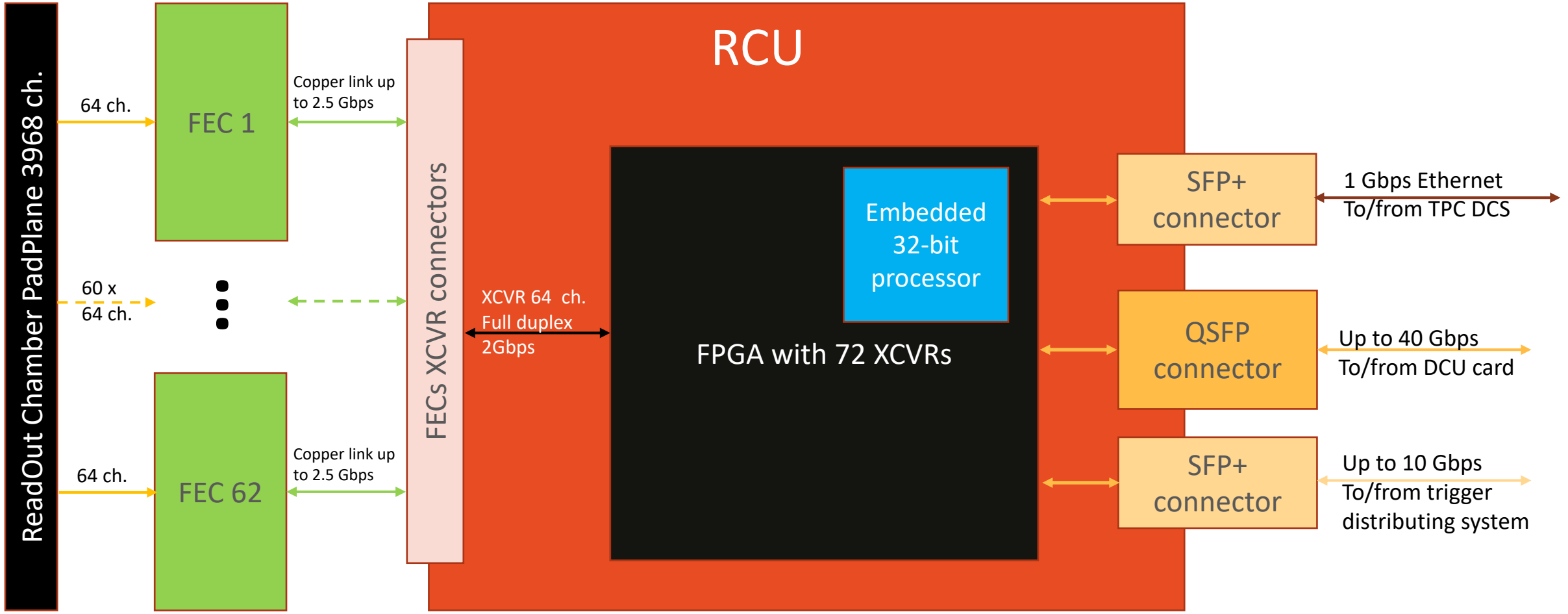
Local Data Concentrator (**LDC**) servers: 6 pc. in total

6 ×

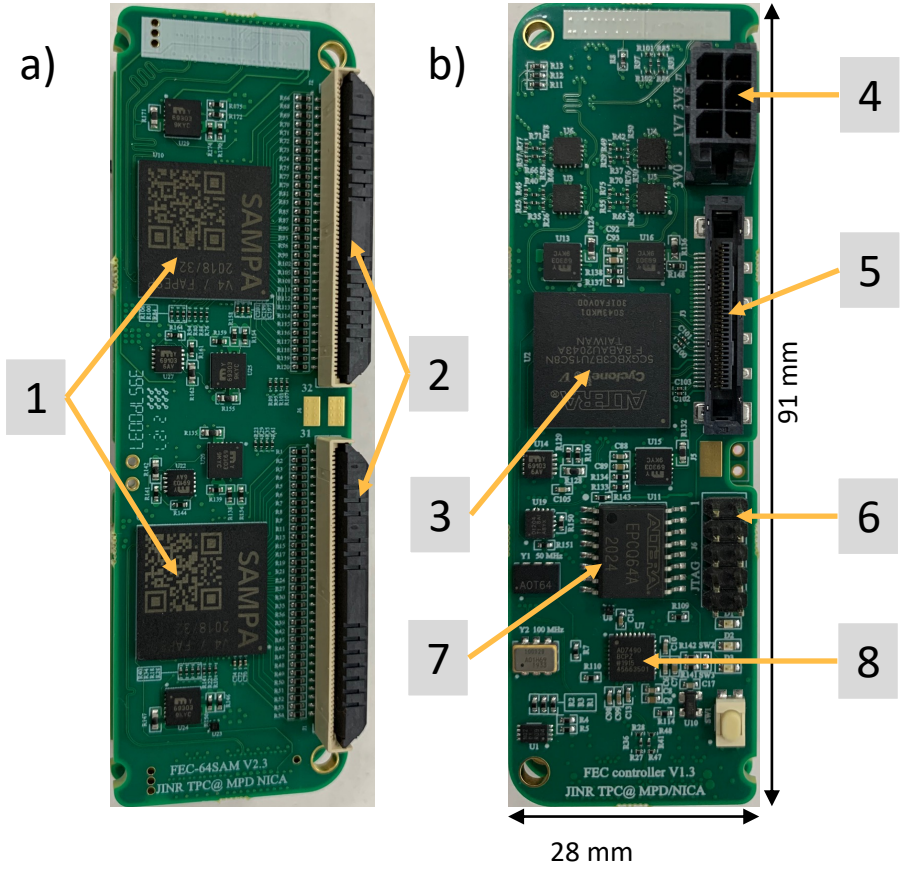
TPC/MPD DAQ network



One chamber readout scheme (1/24 of full TPC readout stream)



Front-End Card characteristics, components and production status



FEC: a) Bottom view (ROC side); b) Top view (service side). 1 – SAMPA ASICs; 2 – input connectors; 3 – FPGA; 4 – PS connector; 5 – HSSI connector; 6 – JTAG connector; 7 – EPCQ64 flash memory; 8 –control 16 ch. ADC.

- The total number of registration channels: 64
- Maximum input charge within the linear range: 100 fC
- ADC resolution: 10 bit
- ENC: les than 1000 e^-
- Readout serial interface: up to 2.5 Gbps
- The total number of monitored values for current, voltage, and temperature: 16

➢Management of SAMPA chips via FPGA high-speed interface.

➢*Double-PCB FEC provides opportunities for potential card readout upgrades.*

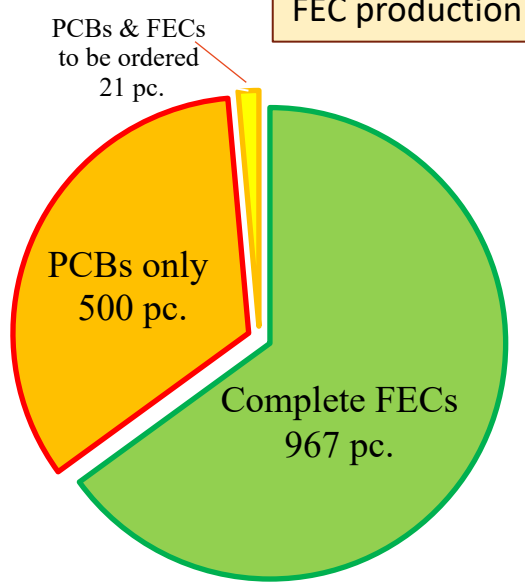
➢*Data and trigger signal transfer were achieved using the same high-speed serial interface.*

➢*Onboard circuitry and embedded protection functionality against SEU are provided.*

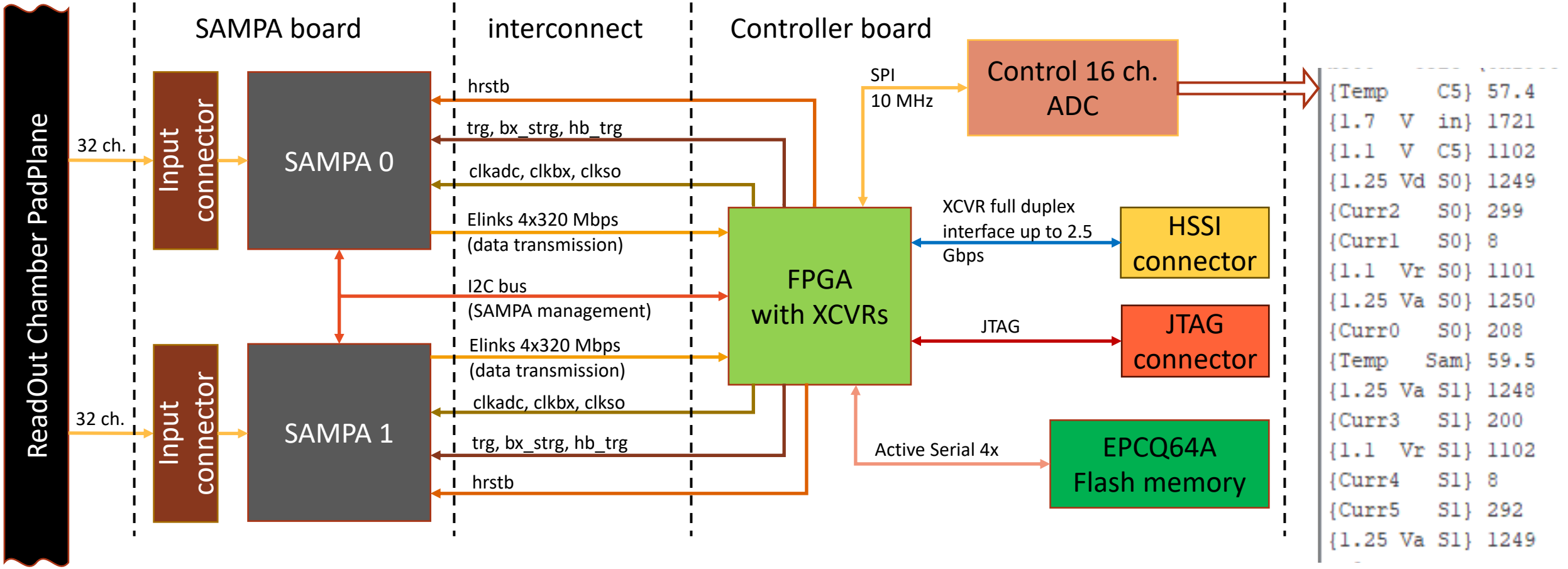
➢*Remote system updates for FEC firmware are available.*

Double-desk FEC formfactor:
a) SAMPA board;
b) Controller board;

FEC production status:

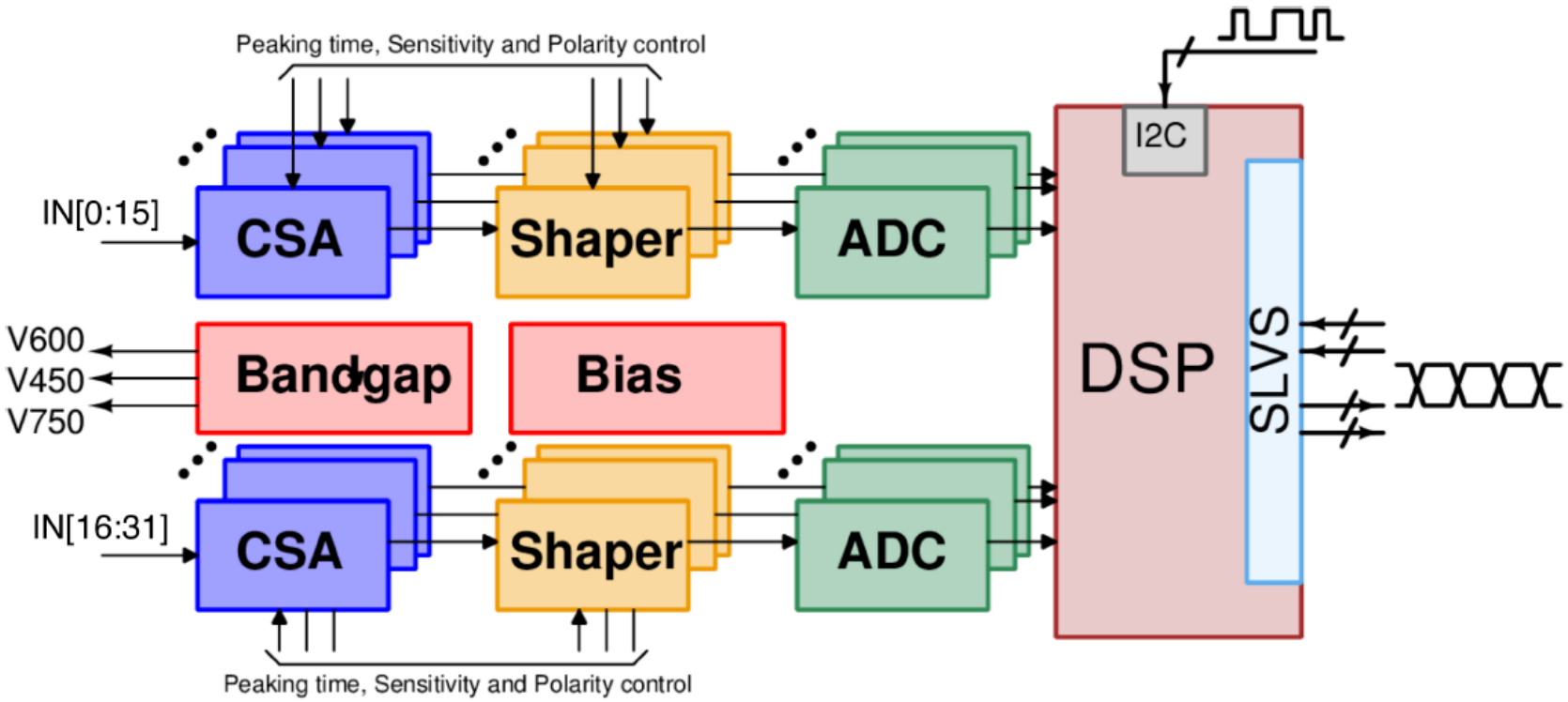


FEC structural scheme



The FEC includes SAMPA ASICs, FPGA and serial interfaces.

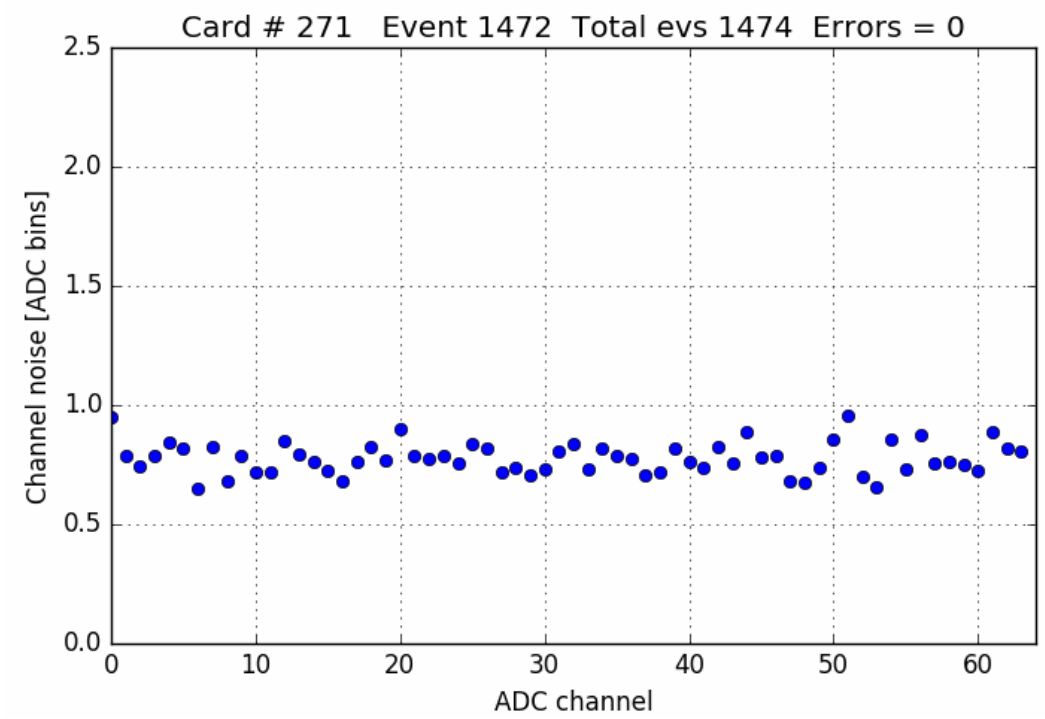
SAMPA ASIC: the core of FEC



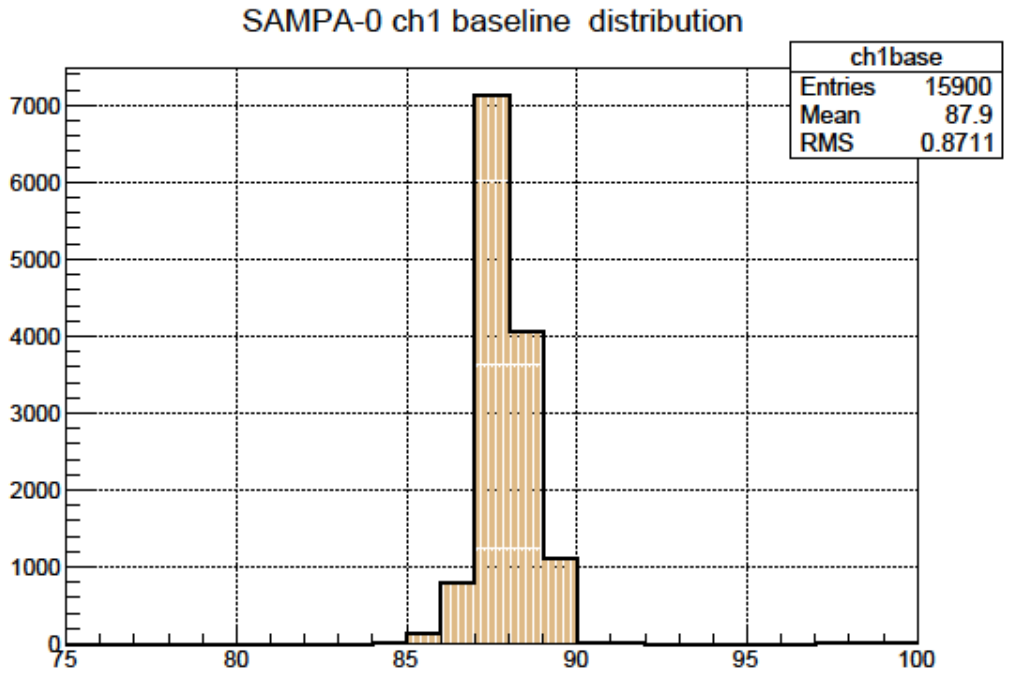
The SAMPA ASIC includes 32 blocks comprising charge-sensitive amplification, signal shaping, digitization, digital signal processing, data memory, and a serial data interface.

[1] J. Adolfsson, et al., SAMPA chip: the new 32 channels ASIC for the ALICE TPC and MCH upgrades, JINST 12 (04) (2017) C04008.

FEC noise measurement



Noise distribution over FEC channels

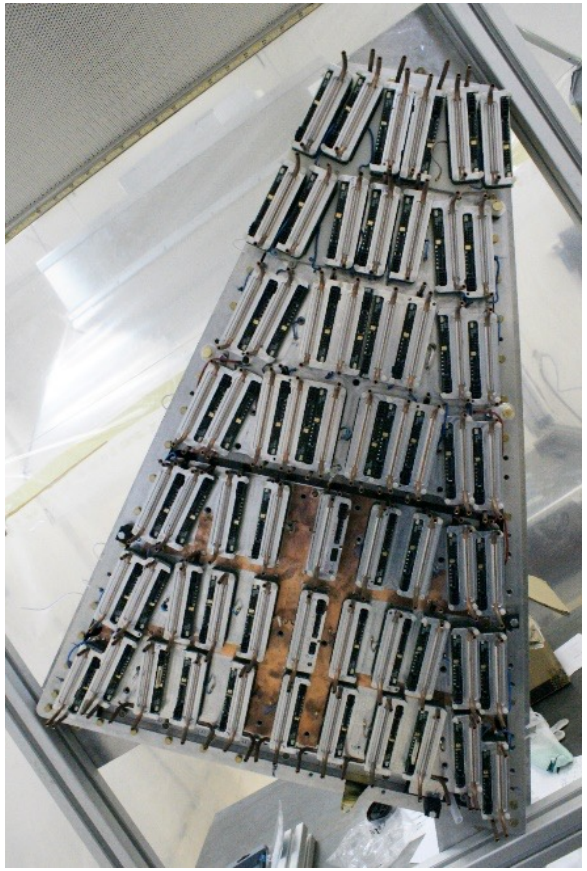


Typical noise distribution of a SAMPA channel

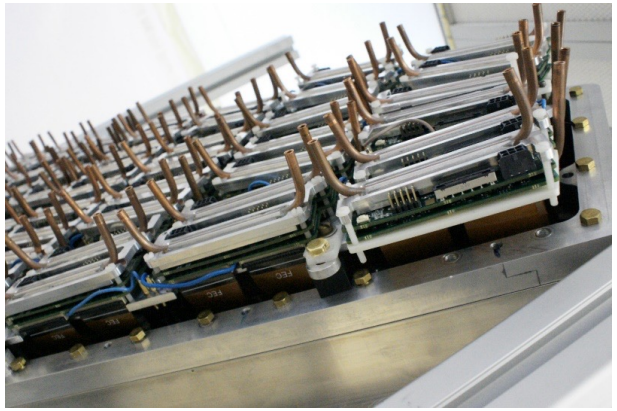
Measurements were conducted without a FEC connection to the ROC. The measurements correspond to the SAMPA ASIC specifications.

1 ADC LSB = 670 e^-

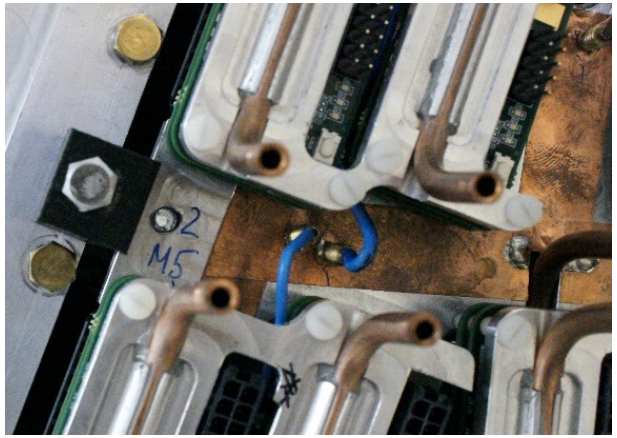
FECs position on the ROC



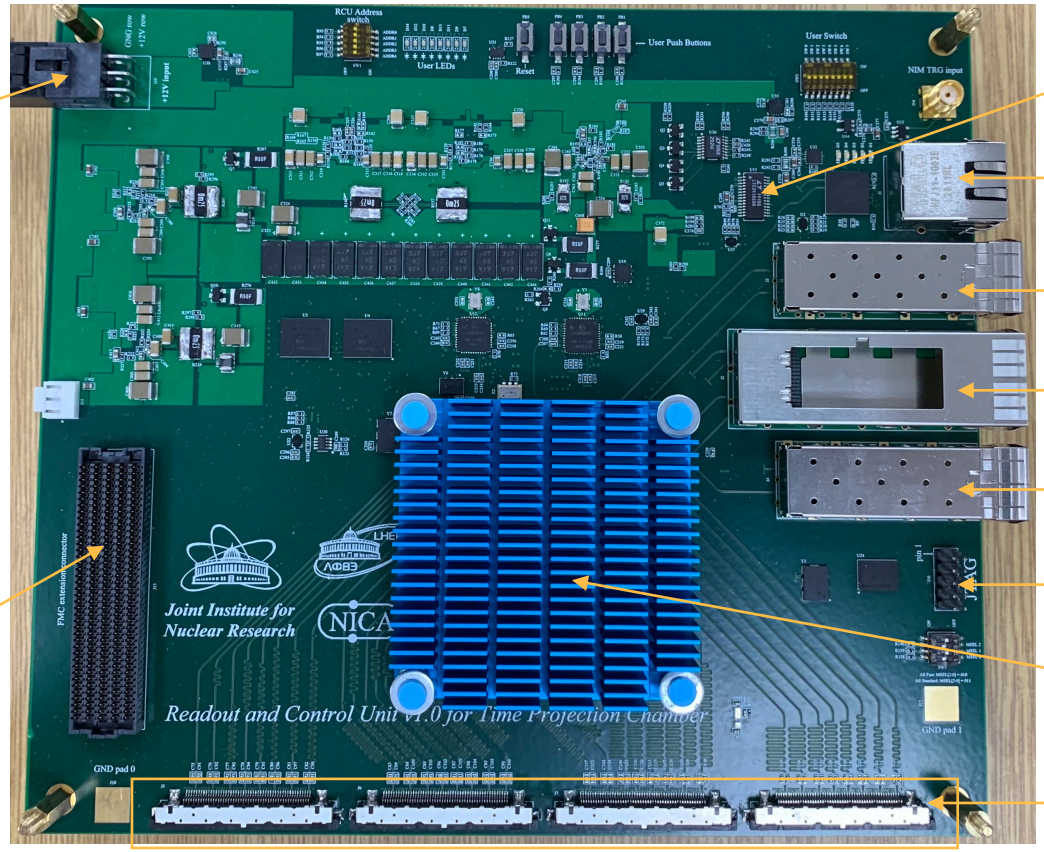
The double-desk FEC form factor enables us to reduce the amount of material at the TPC endcaps and distribute it evenly.
All FECs were placed on one level, covered from both sides by cooling plates.



The possibility for additional grounding of the FECs was provided.



Readout and Control Unit components and functionality

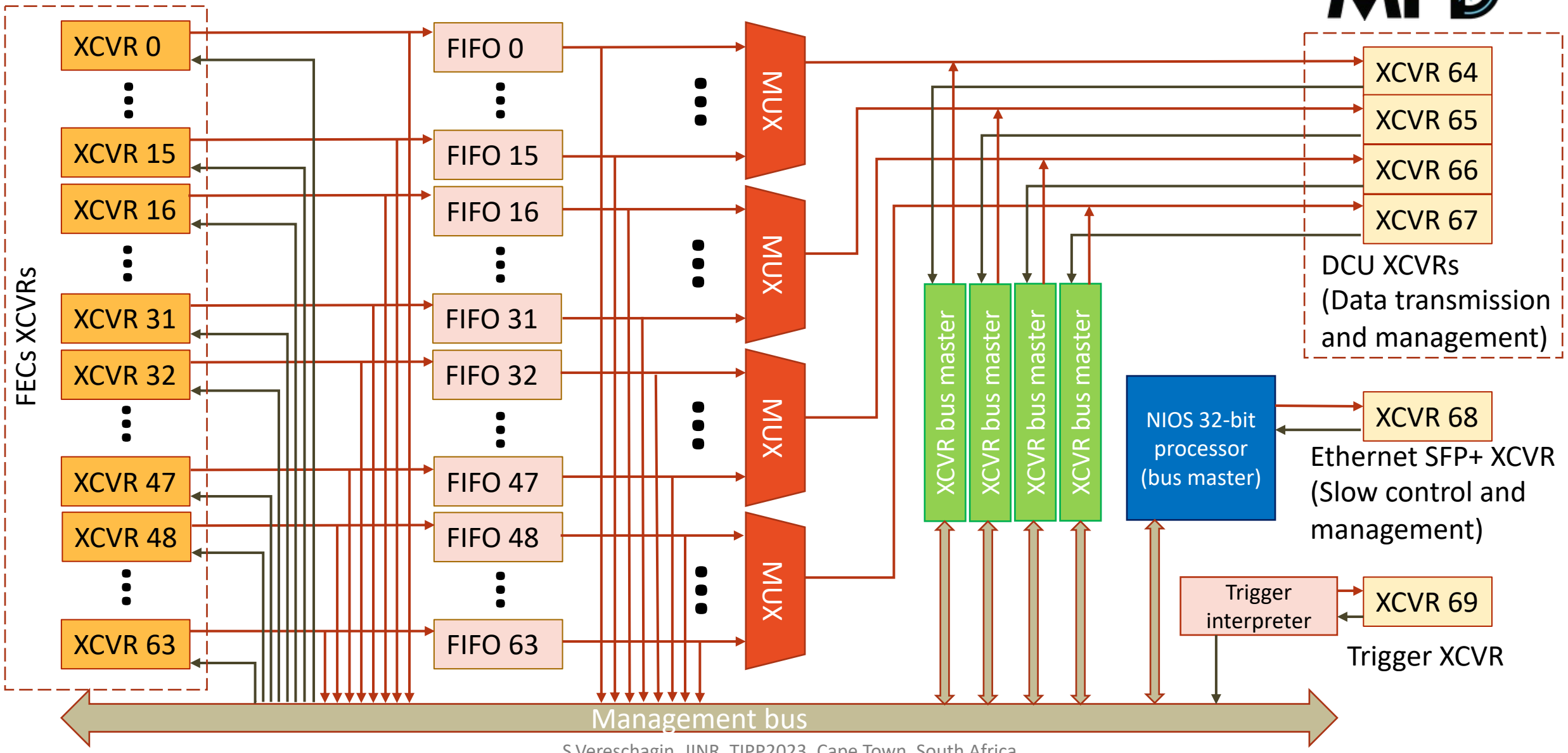


1. PS connector (+12 V)
2. 16-ch. ADC (health monitoring)
3. RJ45 connector (NIOS Ethernet 1Gbps)
4. SFP+ connector (optical trigger up to 10 Gbps)
5. QSFP connector (data transfer interface up to 40 Gbps)
6. SFP+ connector (spare optical channel up to 10 Gbps)
7. JTAG connector (FPGA programming end debugging + spare management channel)
8. Arria 10 GX FPGA
9. FECs XCVR connectors 64 full duplex channels
10. Multifunctional connector with GPIO pins and 2 spare XCVR

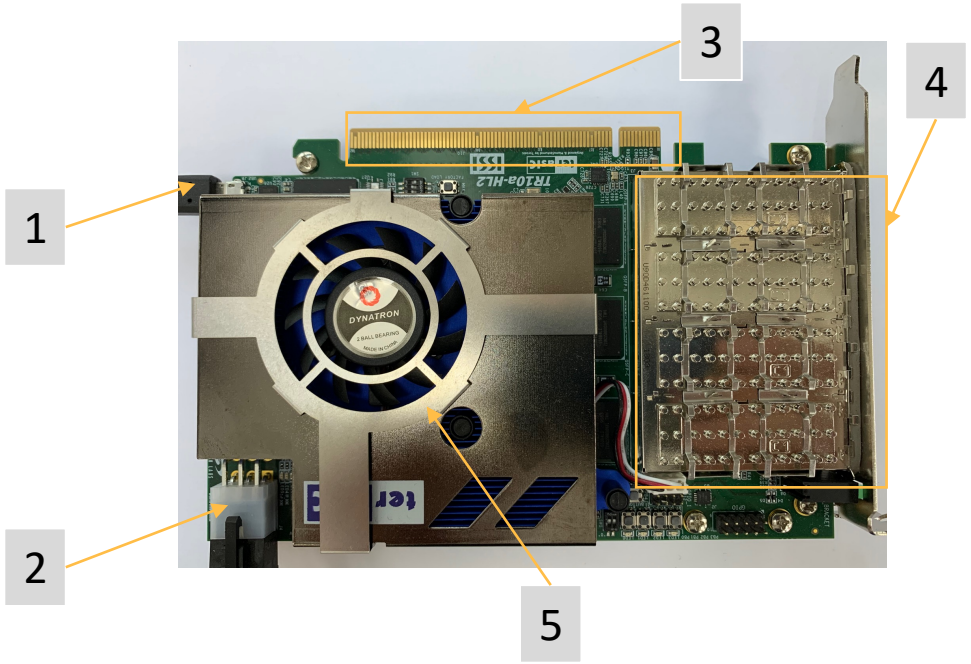
Main RCU functionalities include:

- Receiving data packets from 62 FECs.
- Buffering data with subsequent transmission to the DCU via an optical channel.
- Organizing a high-speed management channel to the FECs.
- Organizing FECs synchronization.

Core of RCU firmware structural scheme



Local Data Concentrator and Data Concentrator Unit



LDC based on DELL R740XD rack unit

Receiving data via PCIe of the DCU card and after transmitting it to the MPD DAQ via 100G Ethernet

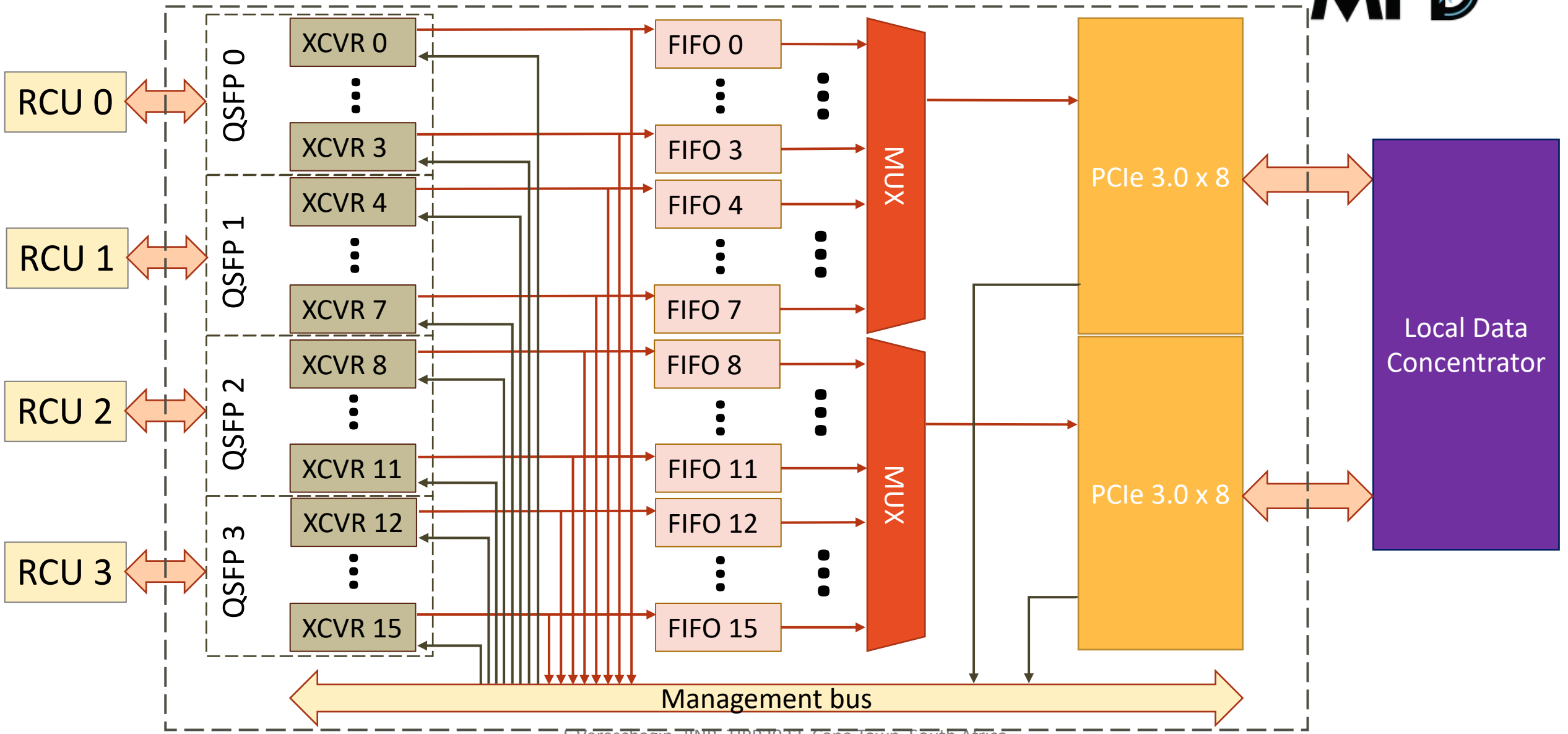
DCU card based on commercial development board

1) USB connector for onboard usb-blaster;
2) PS connector +12 V;
3) PCIe gen 3 x16 connector (double x8);
4) 4 QSFP connectors for data taking and management;
5) Arria 10 GX FPGA;

DCU functionality includes:

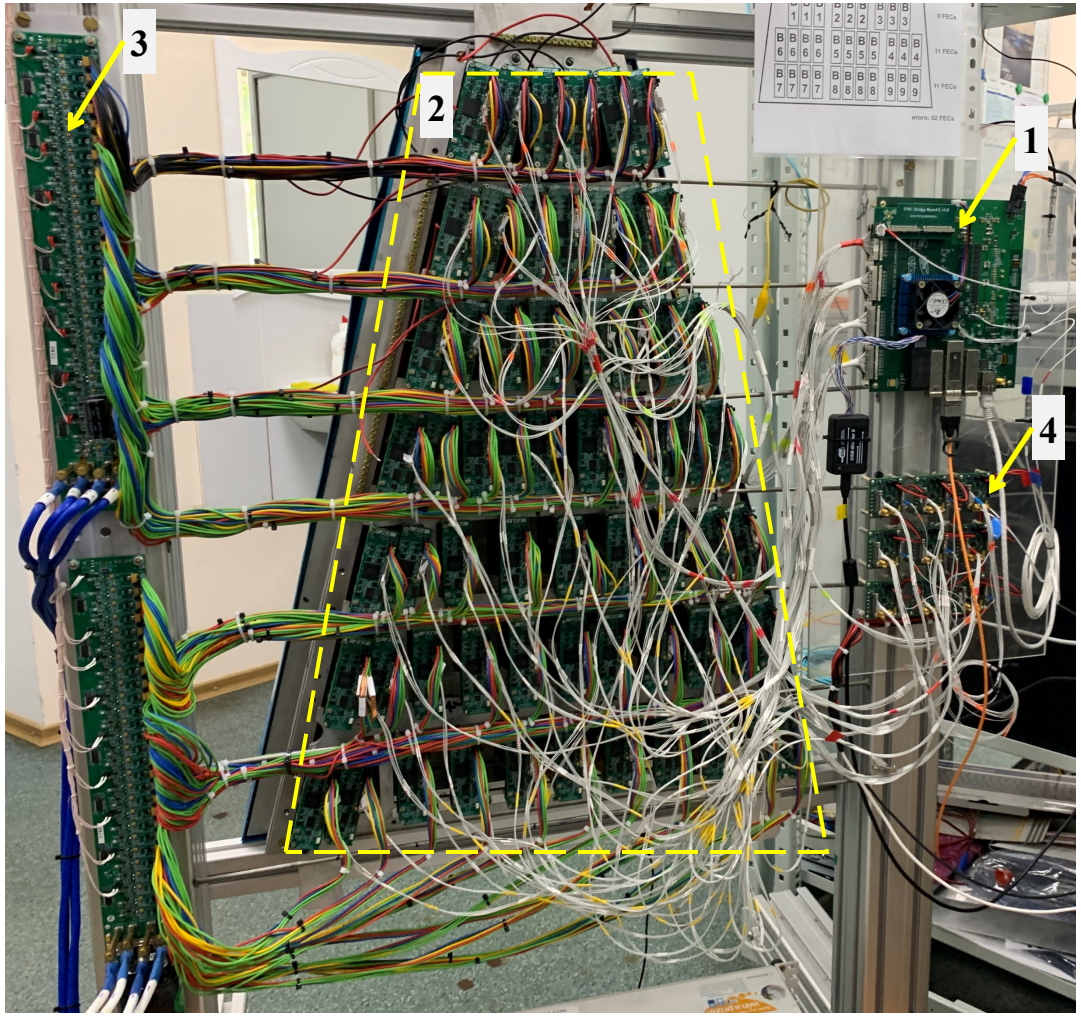
- Receiving data packets from four RCUs.
- Organizing a high-speed management channel via PCIe.
- Managing all downstream devices (RCUs, FECs).
- Buffering data with subsequent transmission to the server memory via PCIe.

Core of DCU firmware structural scheme

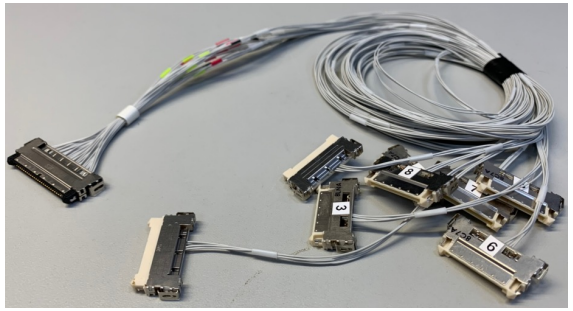


ReadOut Chamber DAQ test setups

Setup in electronics test room

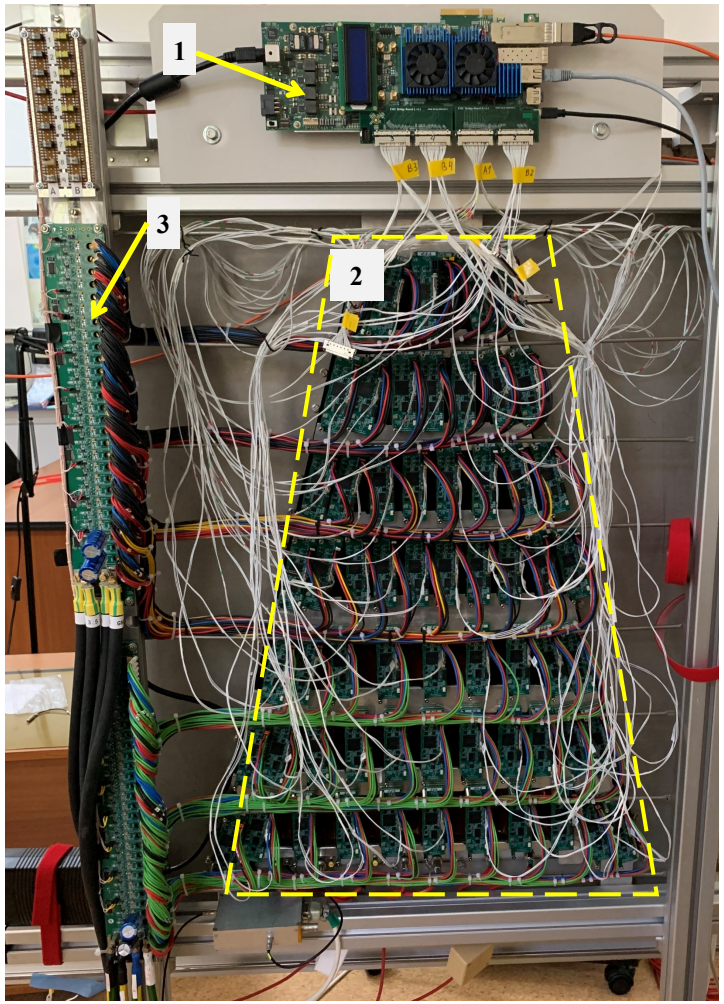


1. RCU64 (left) and RCU32 (right)
2. FECs on the ROC (62 pc)
3. LVDB modules
4. Clock fanout



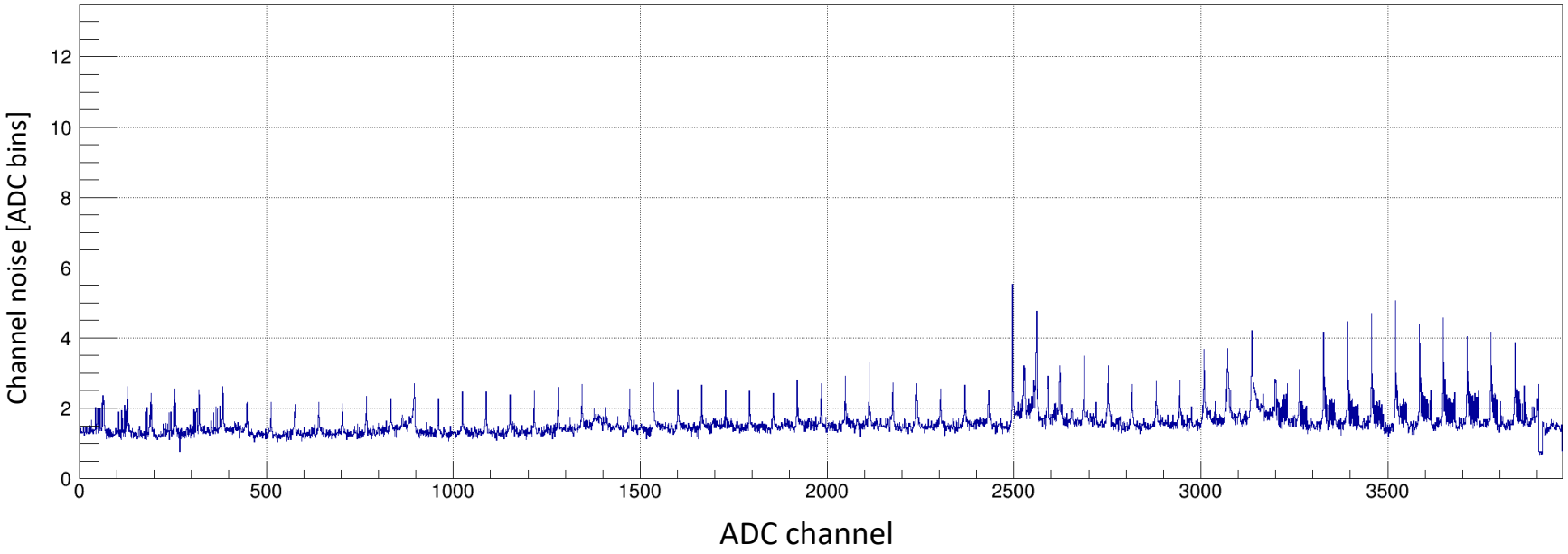
A vital element of the ROC data acquisition system is the microcoaxial cable assembly, based on µcoax 36 AWG cables and Hirose FX15 and FX16 series connectors.

Setup in MWPC workshop building

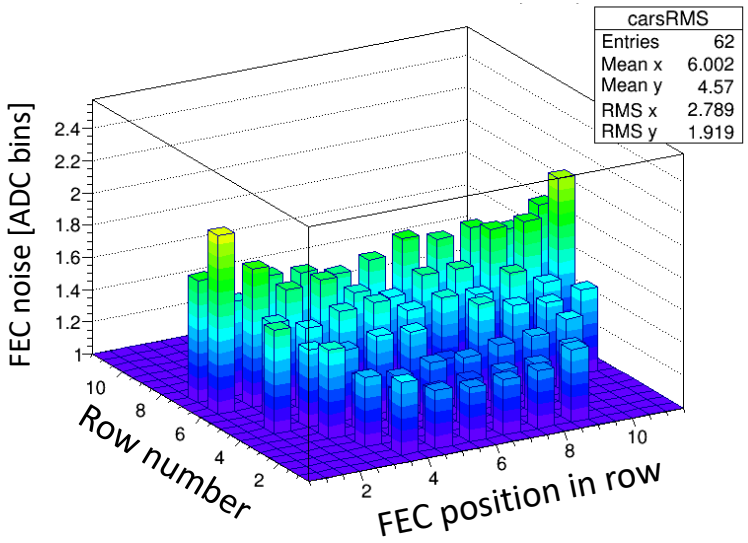


DAQ setup testing

Noise distribution of 3 968 channels of MWPC



FECs mean noise RMS over MWPC



The testing program includes FECs noise study, connectivity testing with probe signals, and readout stability assessment.

Data throughput estimate

Size of one event packet from FEC is 208896 bits

Size of one event packet from RCU is about 13Mb

Size of one event packet from 4 RCU is about 52Mb

At trigger rate 7 kHz FEC data stream is about 1.5 Gbps

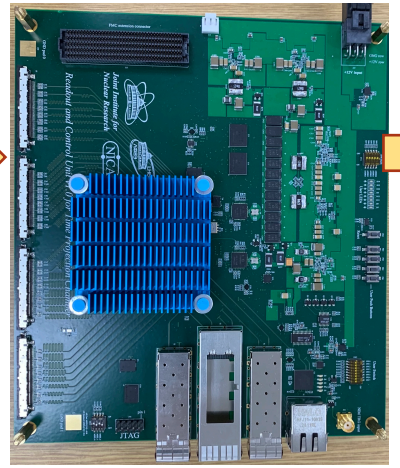
Max trigger rate for raw events is about 2.4 kHz

Max trigger rate for raw events is about 2.4 kHz

FEC to RCU

2 Gbps x 64

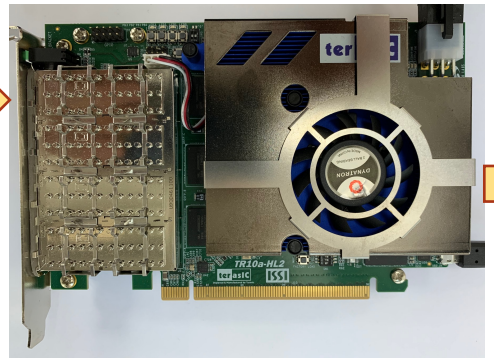
Copper microcoaxial cable assembly



RCU to DCU

32 Gbps x4

Optical fiber



DCU to LDC

126 Gbps

FEC XCVR max data rate is 2.5 Gbps (2 Gbps using 8/10 bit encoding)

Optical transceiver max data rate is 40 Gbps (32 Gbps using 8/10 bit encoding)

PCIe 3.0 x16 max data rate is 128 Gbps (126 Gbps without 128/130 bit encoding)

The system design satisfies the requirement for operation at a trigger rate of 7 kHz using a zero suppression factor of approximately 10.

Summary

- The data acquisition system of the TPC is based on ASICs, FPGAs, high-speed copper, and fiber serial transmission lines.
- The use of FPGAs provides opportunities for future tuning and upgrading of the DAQ firmware.
- Currently, two DAQ-equipped ROCs are undergoing testing at VBLHEP JINR.
- The high parallelization design of the DAQ system aligns with the target requirements, enabling operation at a trigger rate of 7 kHz in a zero suppression mode.