TEMPUS: a Timepix4-based detector system for Photon Science

DESY Photon Science Detector Group

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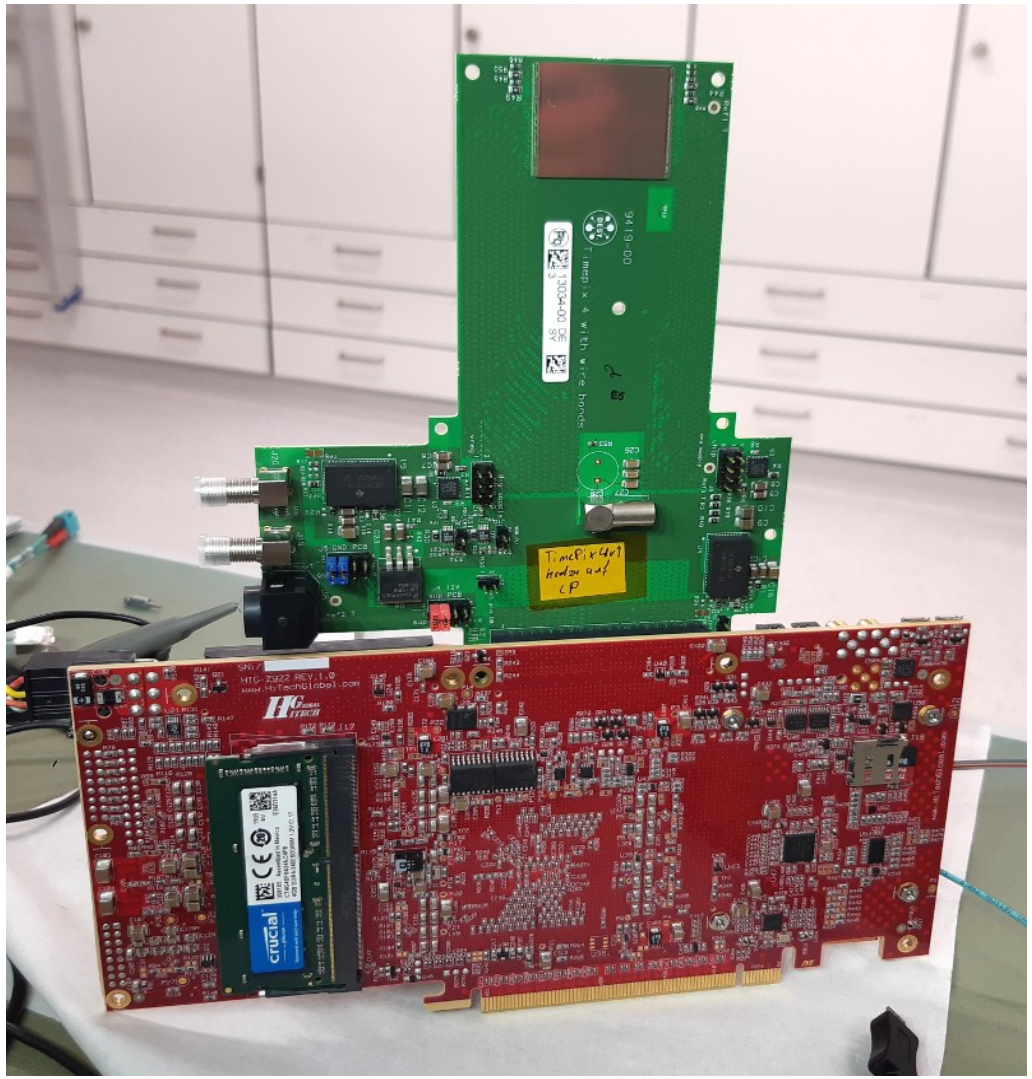
S. Smoljanin, J. Lange, J. Schmehr, H. Klink, A. Beckmann – **X-Spectrum GmbH**



HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

CFEL SCIENCE

DESY

DESY Photon Science

Detector Group

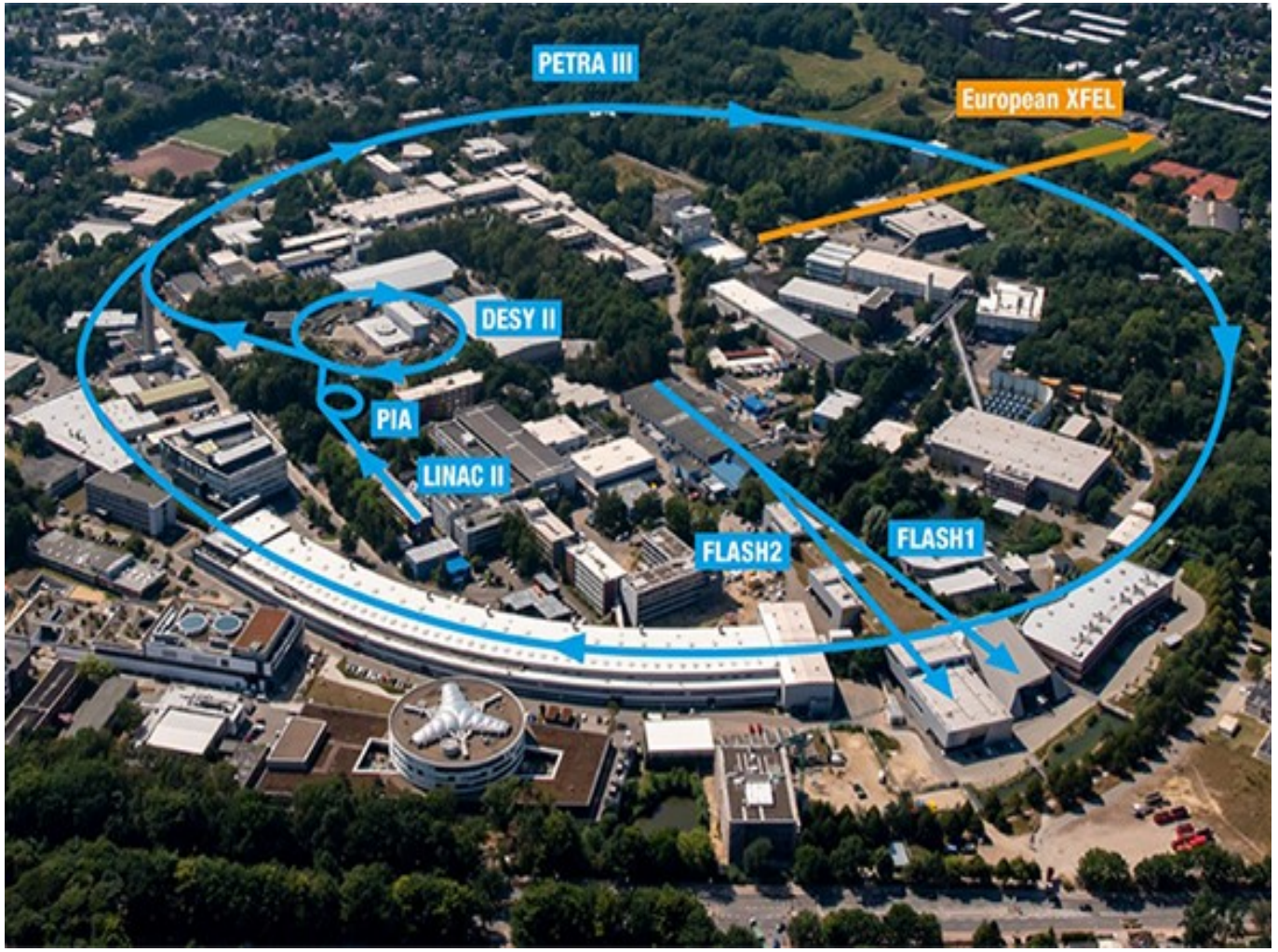
> Storage rings (SR):

- PETRA III
- PETRA IV

> Free Electron Lasers (FELs):

- FLASH
- Eu.XFEL

> Electron and ion detection for experiments in and around our campus



Timepix4 readout chip – key features

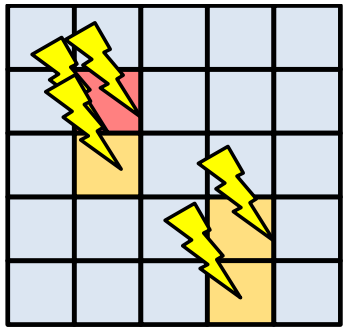
Operation Modes

> Developed by CERN, Nikhef and IFAE on behalf of Medipix4 collaboration – TSMC 65nm

- Timepix4v2 received from foundry in Sept 2021

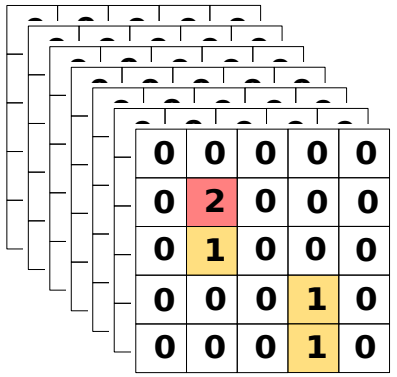
Photon counting and frame readout (like Medipix3)

Detector



55 µm pixels

Frame readout



- 40 kHz frame rate CRW (8 bit depth)
- ~ $4x10^6$ counts/pixel/s

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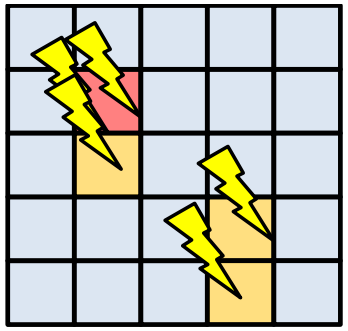

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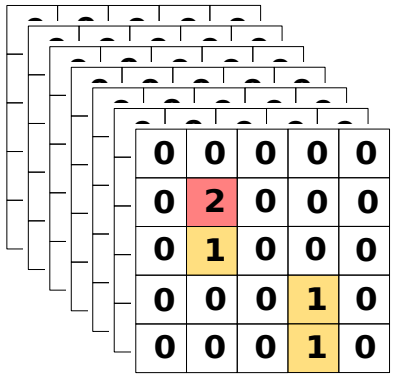

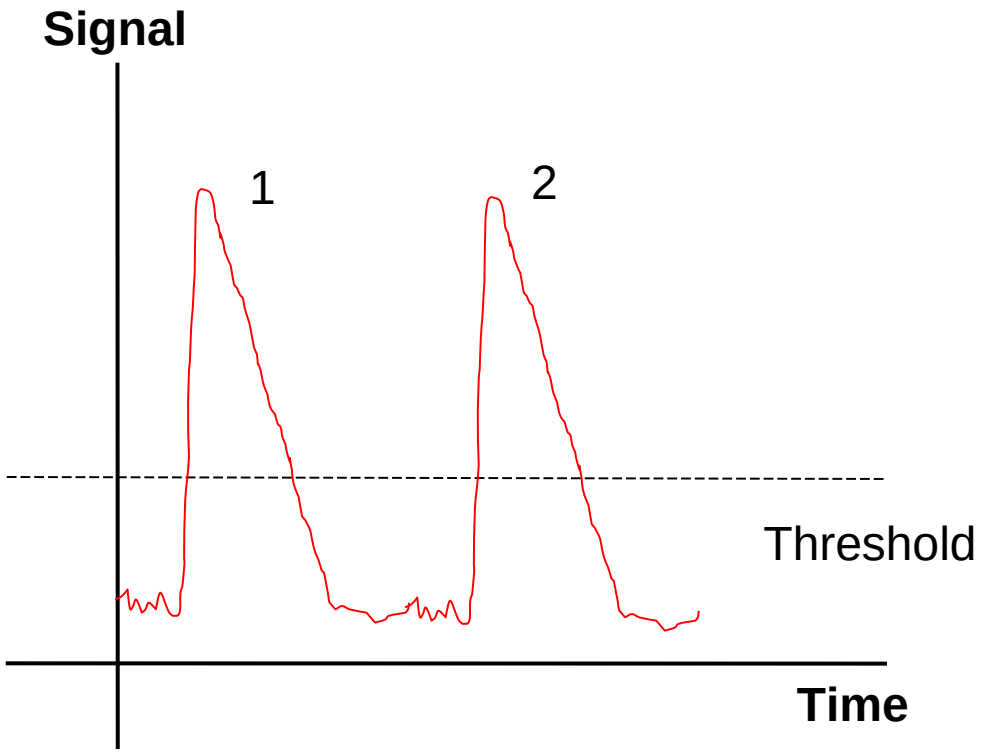

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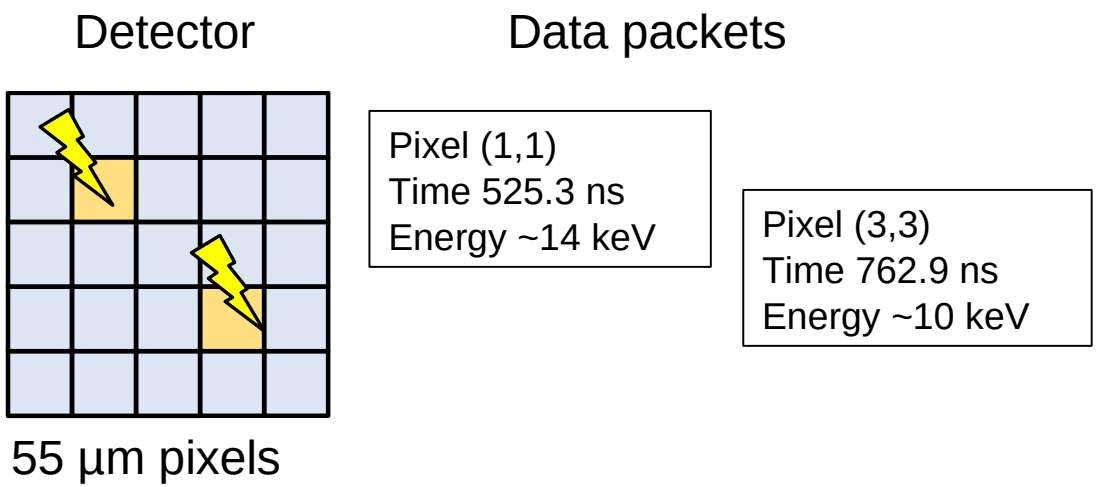

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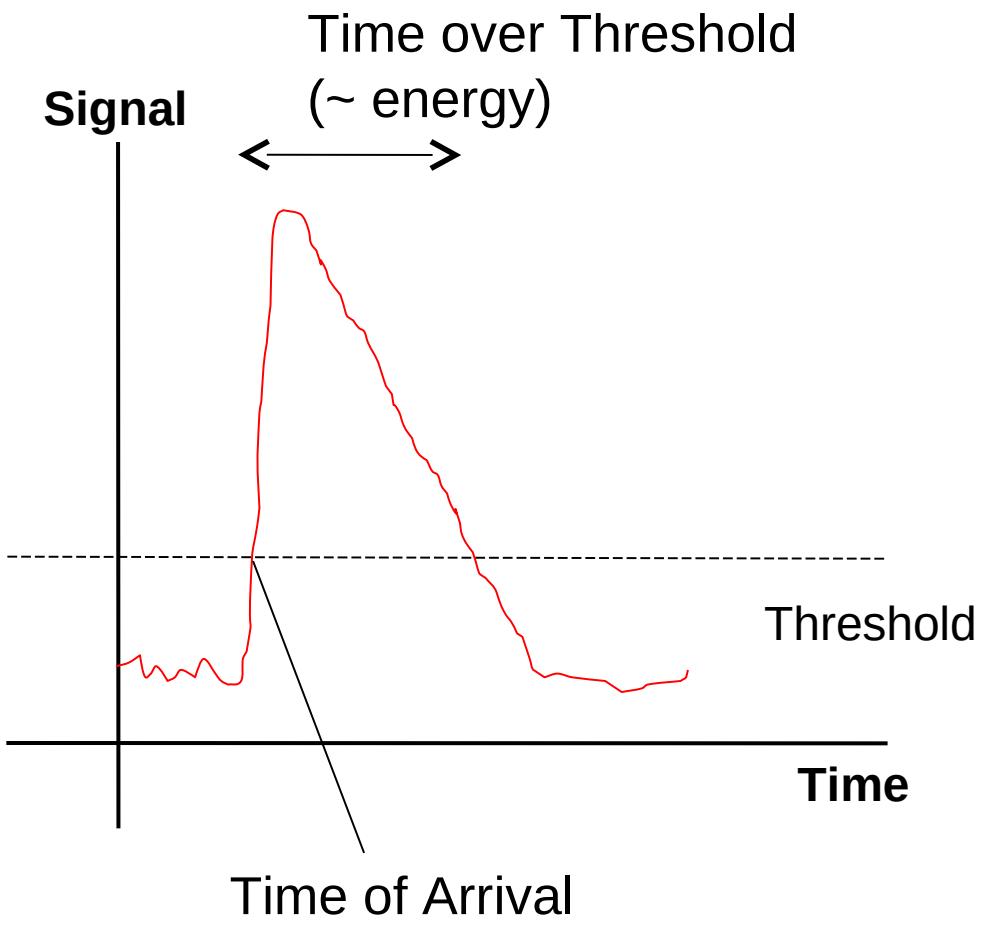

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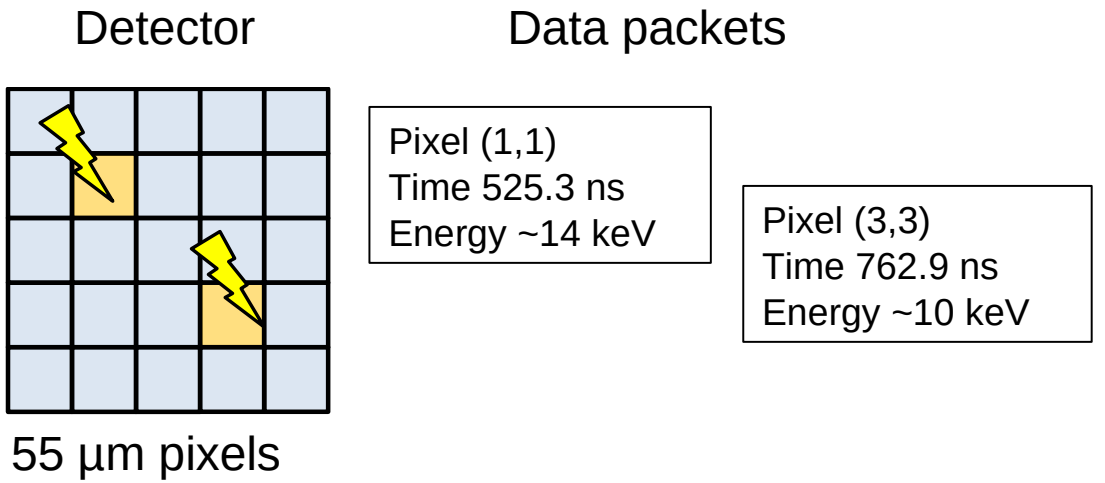

Timepix4 readout chip

Generation comparison

			Timepix3 (2013)	Timepix4 (2019/20)
Technology			IBM 130 nm – 8 metal	TSMC 65 nm – 10 metal
Pixel size			55 x 55 µm	55 x 55 µm
Pixel arrangement			3-side buttable 256 x 256	4-side buttable (TSV) 512 x 448
Sensitive area			1.98 cm^2	6.94 cm^2
Readout modes	**Data driven (tracking)**	**Mode**	ToT and TOA	
		Event packet	48-bit	64-bit
		Max rate	< 43 Mhits/cm^2/s	357.6 Mhits/cm^2/s
		Pix rate equiv.	1.3 kHz/pix average	10.8 kHz/pix average
	Frame Based (imaging)	**Mode**	Count: 10 bit + iToT	Count: 8 or 16 bit CRW
		Frame	Zero suppressed (with pix addr)	Full frame (no pix addr)
		Max count rate	82 Ghits/cm^2/s	~ 800 Ghits/cm^2/s
		Max frame rate	N/A (worst case: 0.8ms readout)	80 kHz CRW
TOT energy resolution			< 2 keV	< 1 keV
Time resolution			1.56 ns	~ 200 ps
Readout bandwidth			≤ 5.12 Gbps (8 x 640 Mbps)	≤163.8 Gbps (16 x 10.2 Gbps)
Target minimum threshold			< 500 e^-	< 500 e^-

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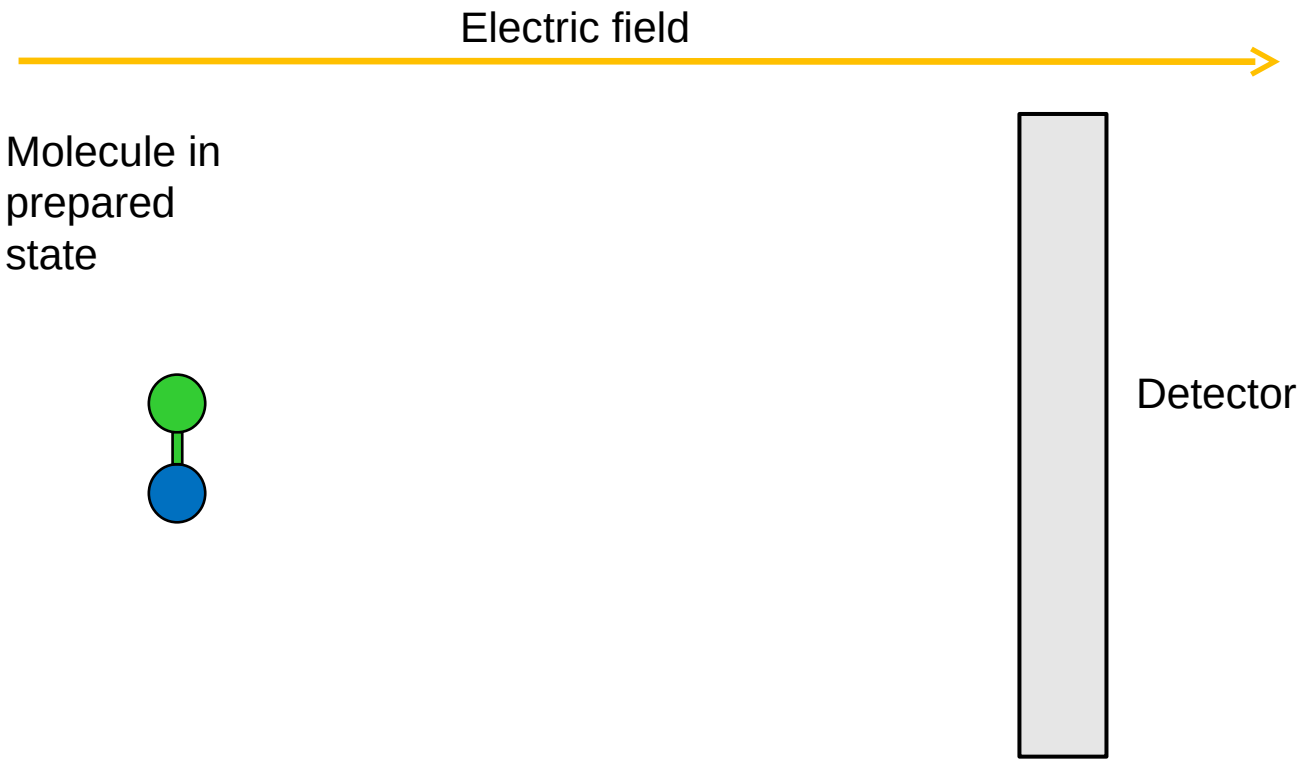
		Max frame rate	N/A (worst case: 0.8ms readout)	80 kHz CRW	
TOT energy resolution			< 2 keV	< 1 keV	2 x
Time resolution			1.56 ns	~ 200 ps	8 x
Readout bandwidth			≤ 5.12 Gbps (8 x 640 Mbps)	≤163.8 Gbps (16 x 10.2 Gbps)	32 x
Target minimum threshold			< 500 e^-	< 500 e^-	

TEMPUS – applications: molecular imaging

Ion detection



Acknowledgment to Melby Johny, Sebastian Trippel, Hubertus Bromberger, Jochen Küpper @ CMI-DESY

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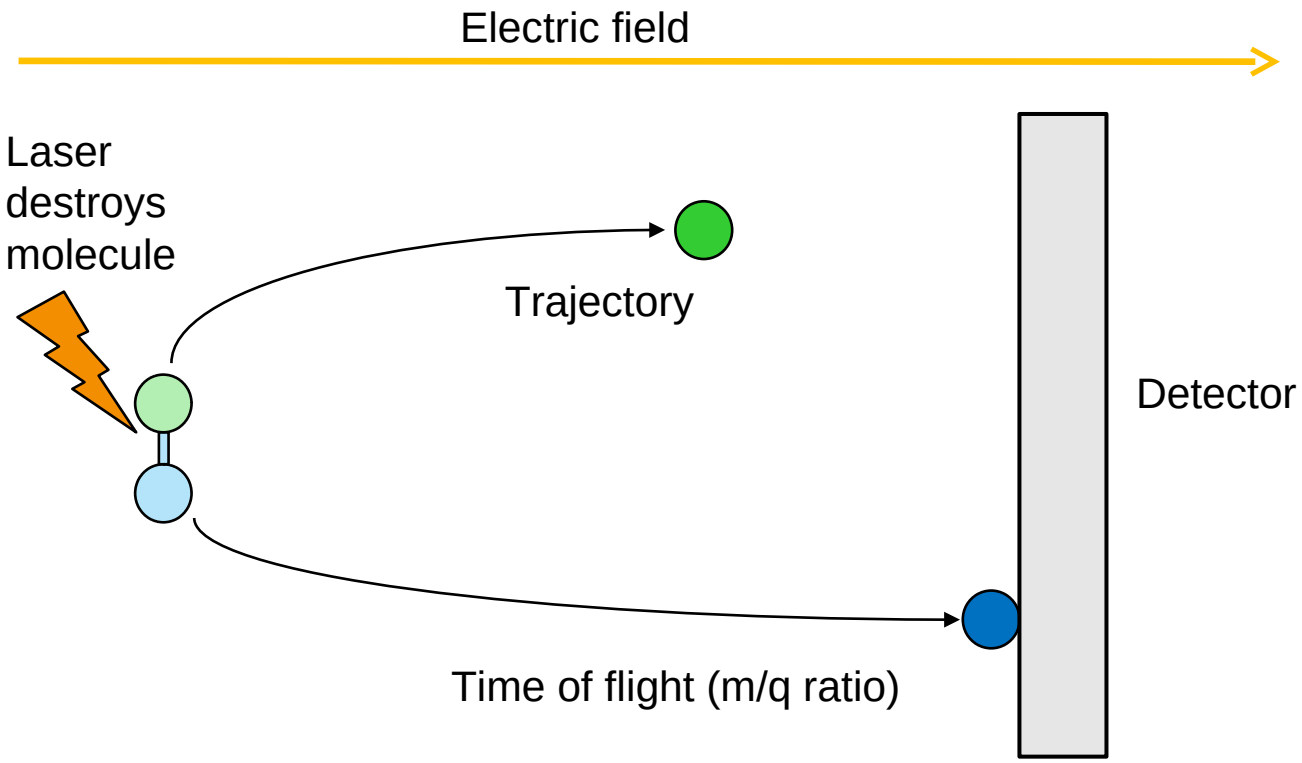

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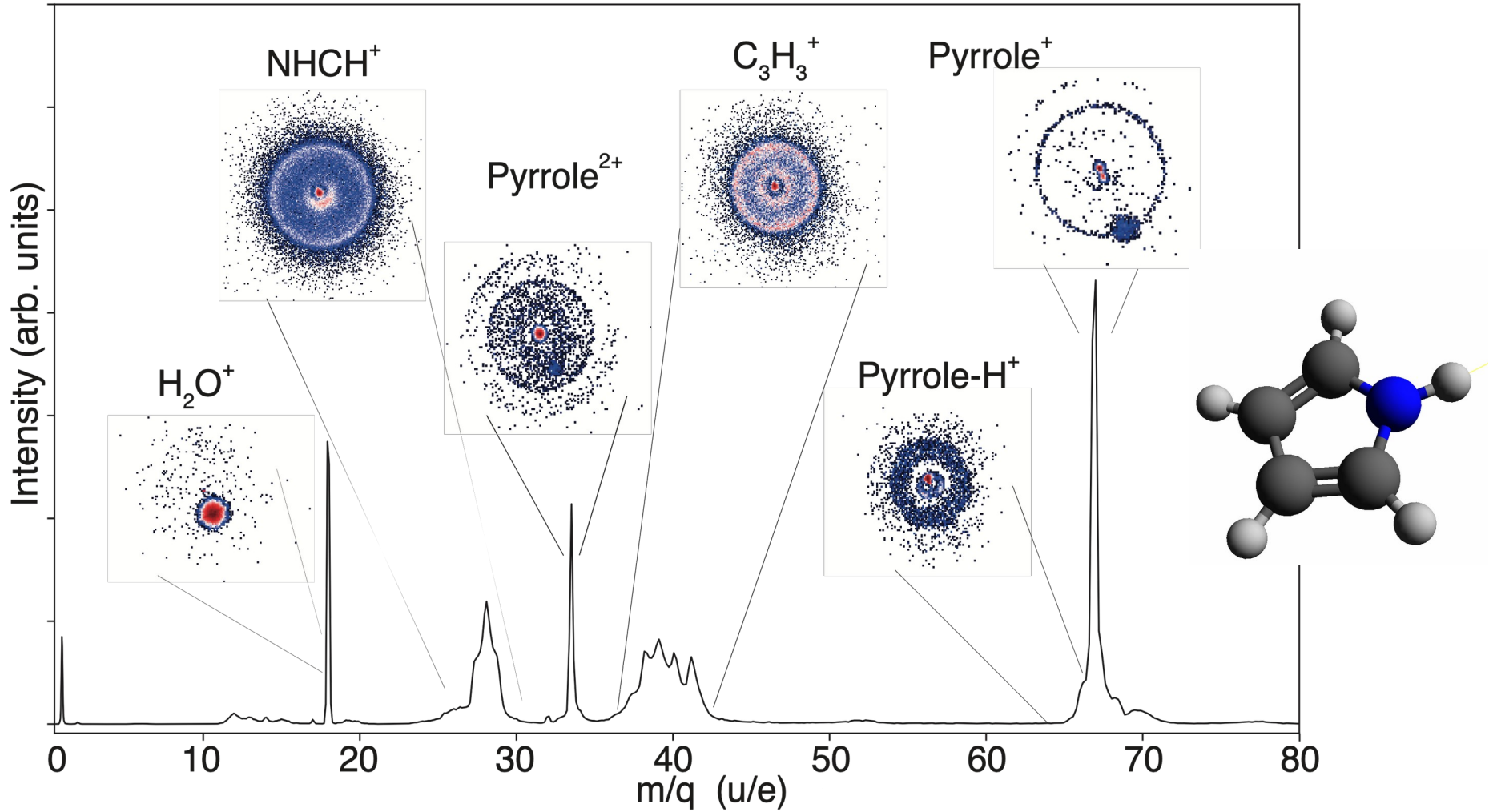
TEMPUS – applications: molecular imaging

Ion detection

~2 ns (std dev) time resolution



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TEMPUS – applications: XPCS @ PETRAIII-P10

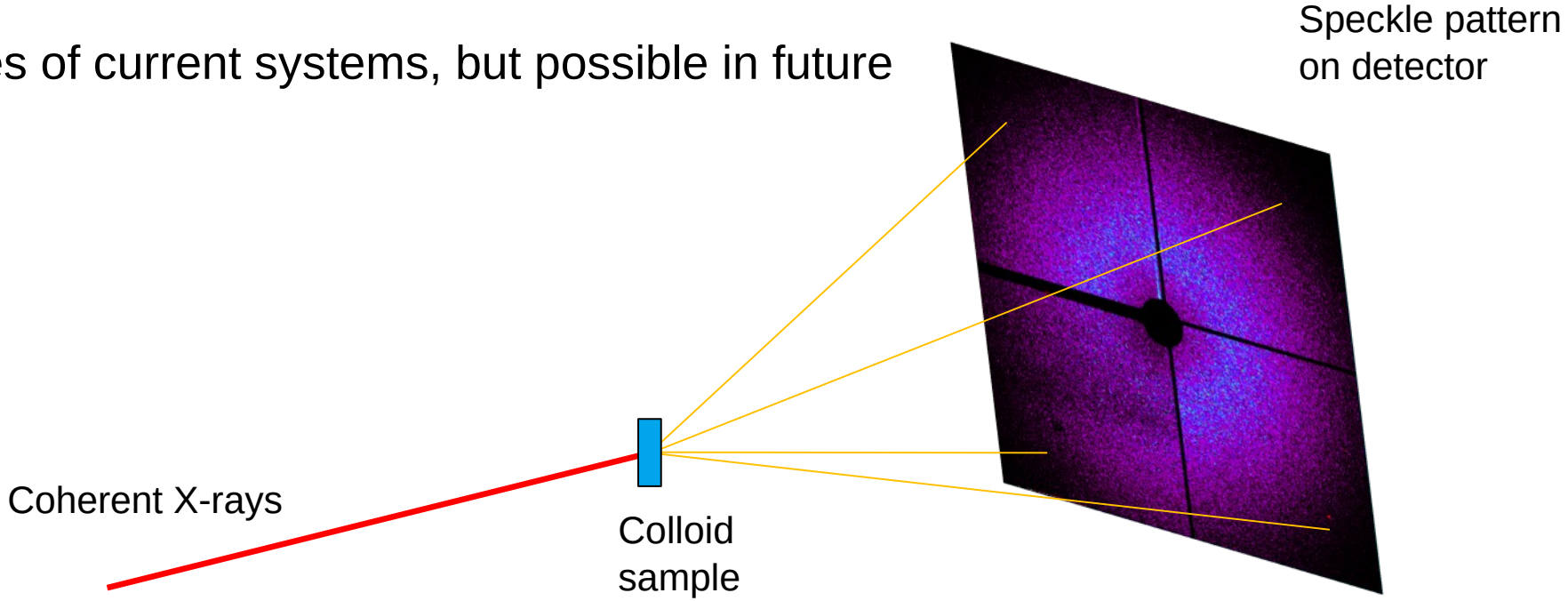
X-ray Photon Correlation Spectroscopy

> Fluctuation of speckle pattern over time reveals dynamics of sample

- At PETRA-IV, XPCS could reach 100 ns time resolution!

> Typical experiment has ~2x10^7 hits/s in detector

- Beyond capabilities of current systems, but possible in future

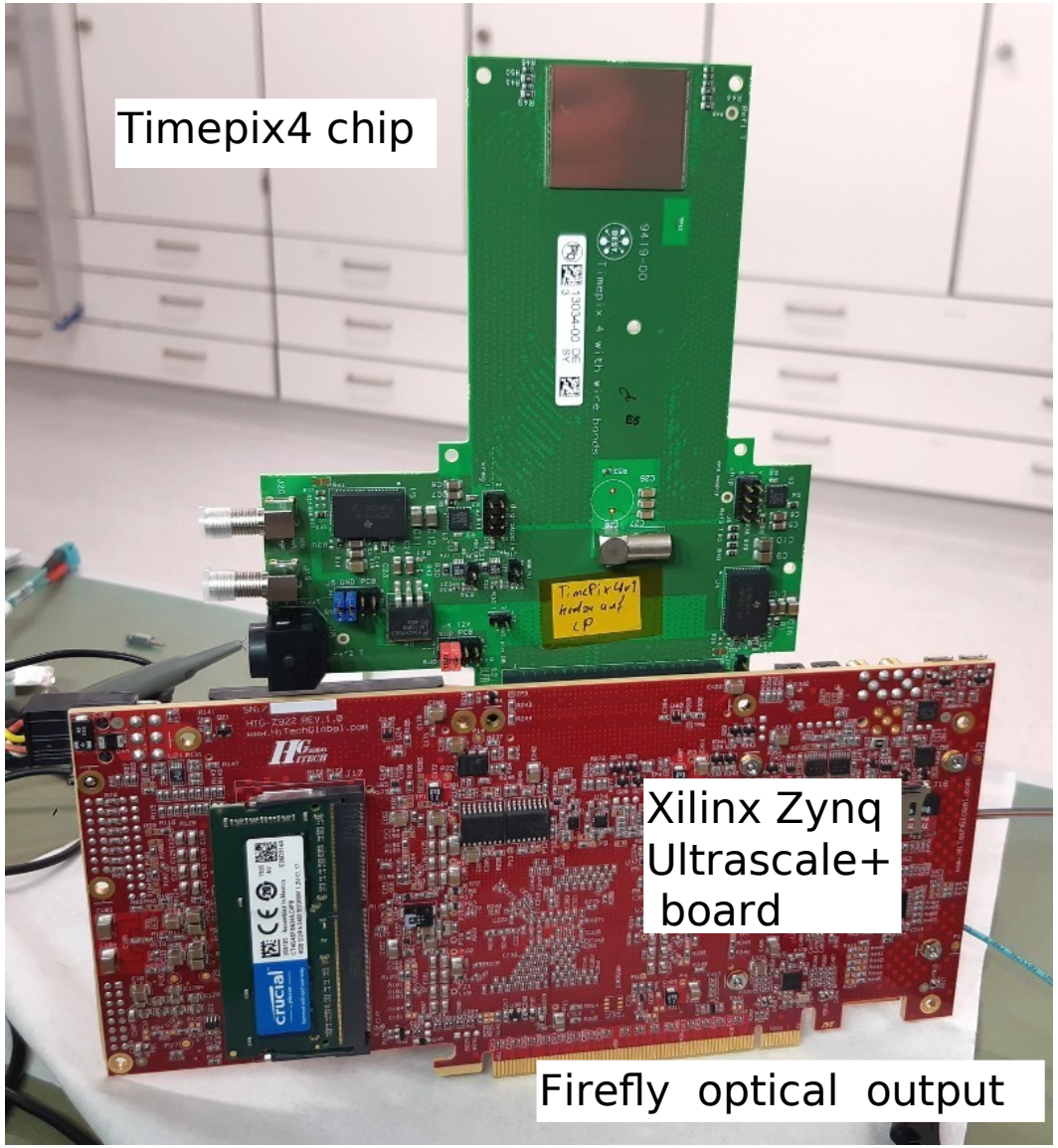


Acknowledgment to Fabian Westermeier, Ruth Livingstone and Michael Sprung @ PETRAIII - P10

TEMPUS readout system

Key features

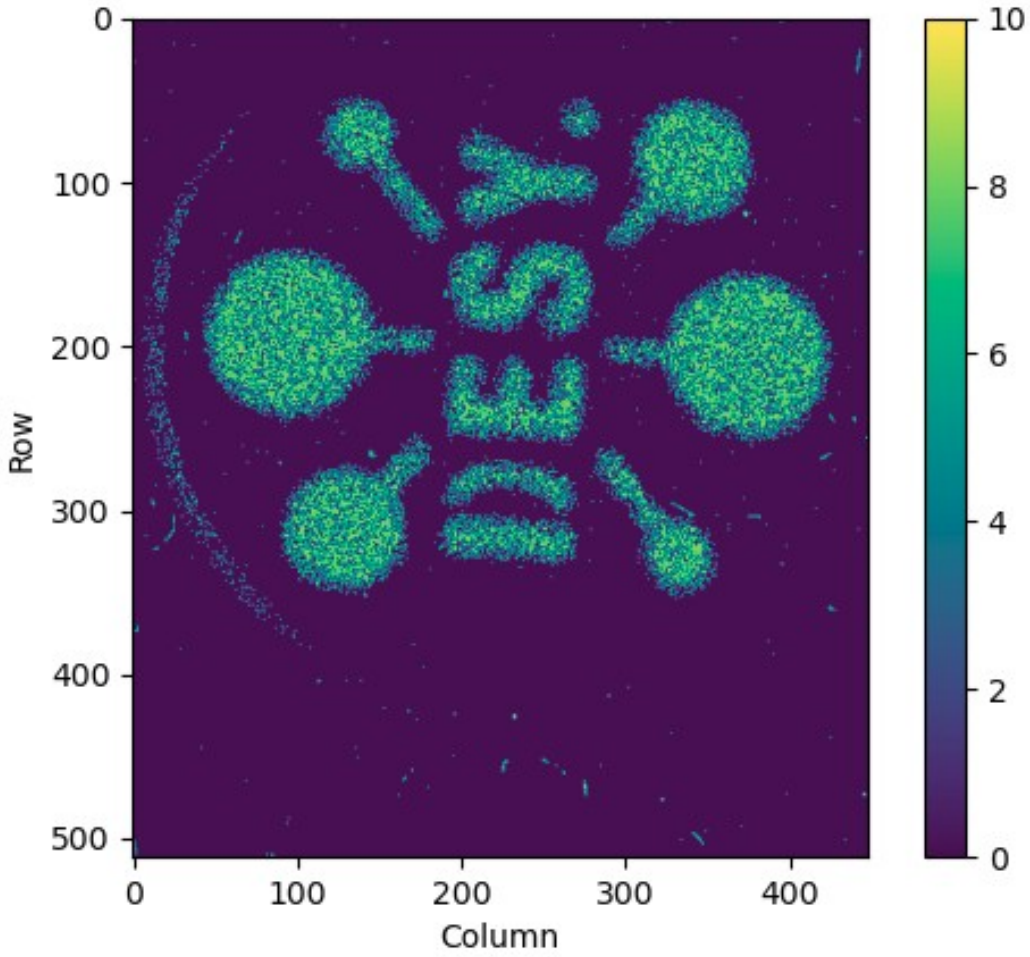
- Single-chip Timepix4 board connected to off-the-shelf Xilinx board:
  - Zynq Ultrascale+ with FPGA fabric and 4-core CPU
- Parallel readout of 16 high-speed links from chip, each up to 5 (or 10) Gbit/s
  - Specialised transceivers on Zynq
- Daughter-board offering 2 x 100 GbE links over “Firefly” optical cable
  - Challenge of dealing with ~ 160Gbits/s



TEMPUS readout system

Development status

- Data read out over the control link
  - First image using a ^{55}Fe source and a DESY-logo target
  - Limited to ~ 5000 hits/second
- High speed data links being debugged
- Basic software for taking data
  - Detector-PC communication protocol: gRPC
  - Implementation of Pymepix library (used in Timepix3) is ready for data processing
- External triggering is operational
  - Different triggering schemes are being implemented
- Digital pixel (provides time reference) operational



TEMPUS – data reception and processing in PC

Hardware and software approaches

> Xilinx FPGA accelerator cards:

- Data reception with 2 x 100 Gigabit Ethernet
- Buffering in high-bandwidth memory
- Data correction in FPGA fabric
  - Programming in C++ (Xilinx High Level Synthesis)
- PCIe4.0 transfer to server PC

> Data reduction algorithms through machine learning:

Rahmani, V. et al. "Data reduction for X-ray serial crystallography using machine learning" J. Appl. Crystallogr. 2023 (56) 1

https://doi.org/10.1107/S1600576722011748

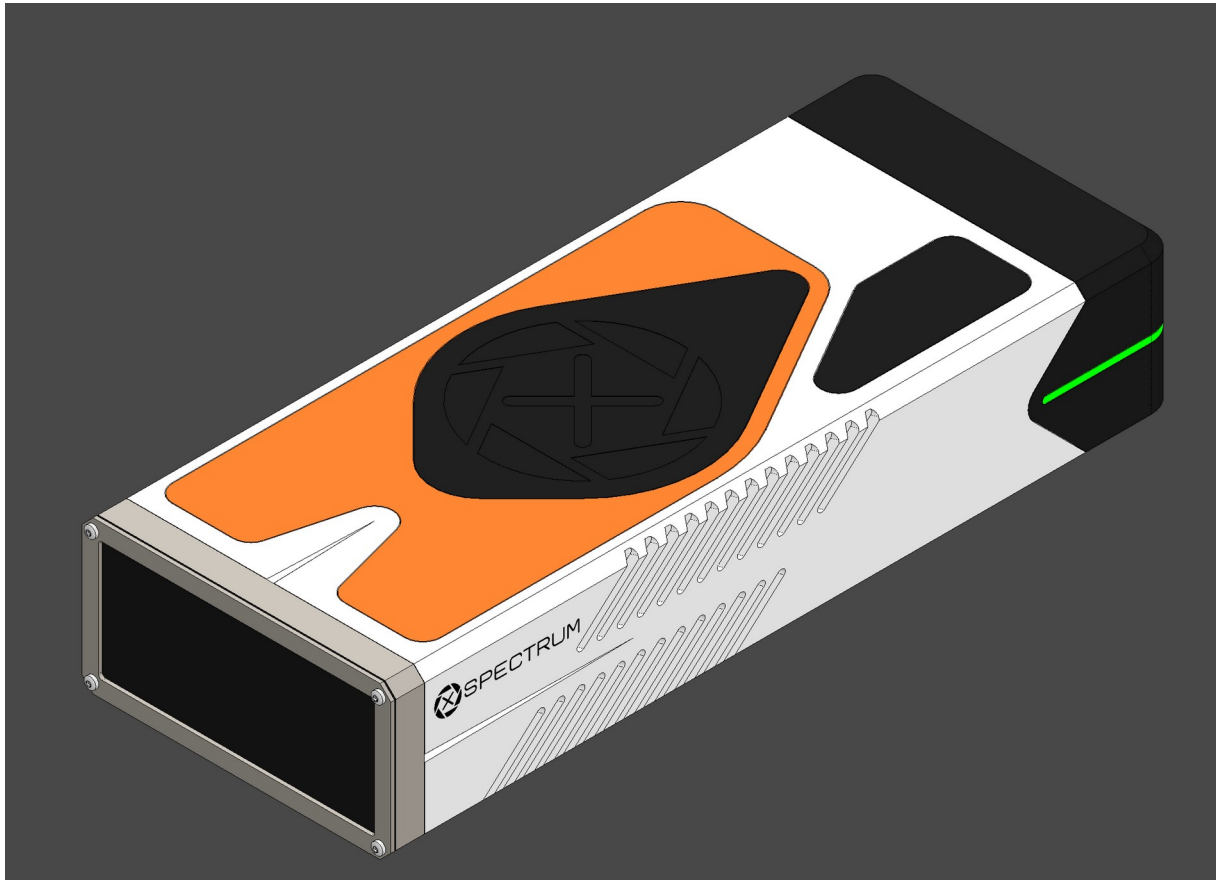
TEMPUS – outlook and perspectives

A multi-chip system

> Goal: large, continuous detector area

> Tileable building block: 3-chip module

> Readout board with Zynq Ultrascale+ SoC



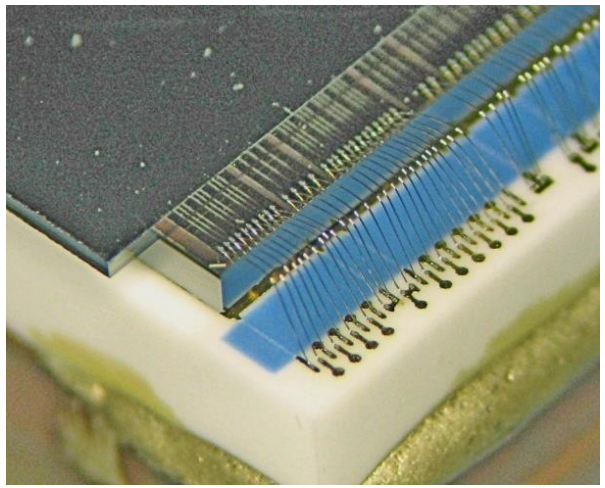
3-chip detector head
1344 x 512 pixels

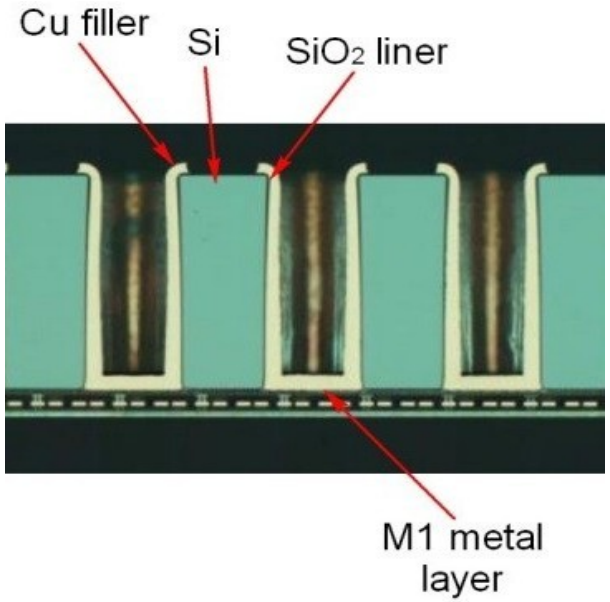
TEMPUS – outlook and perspectives

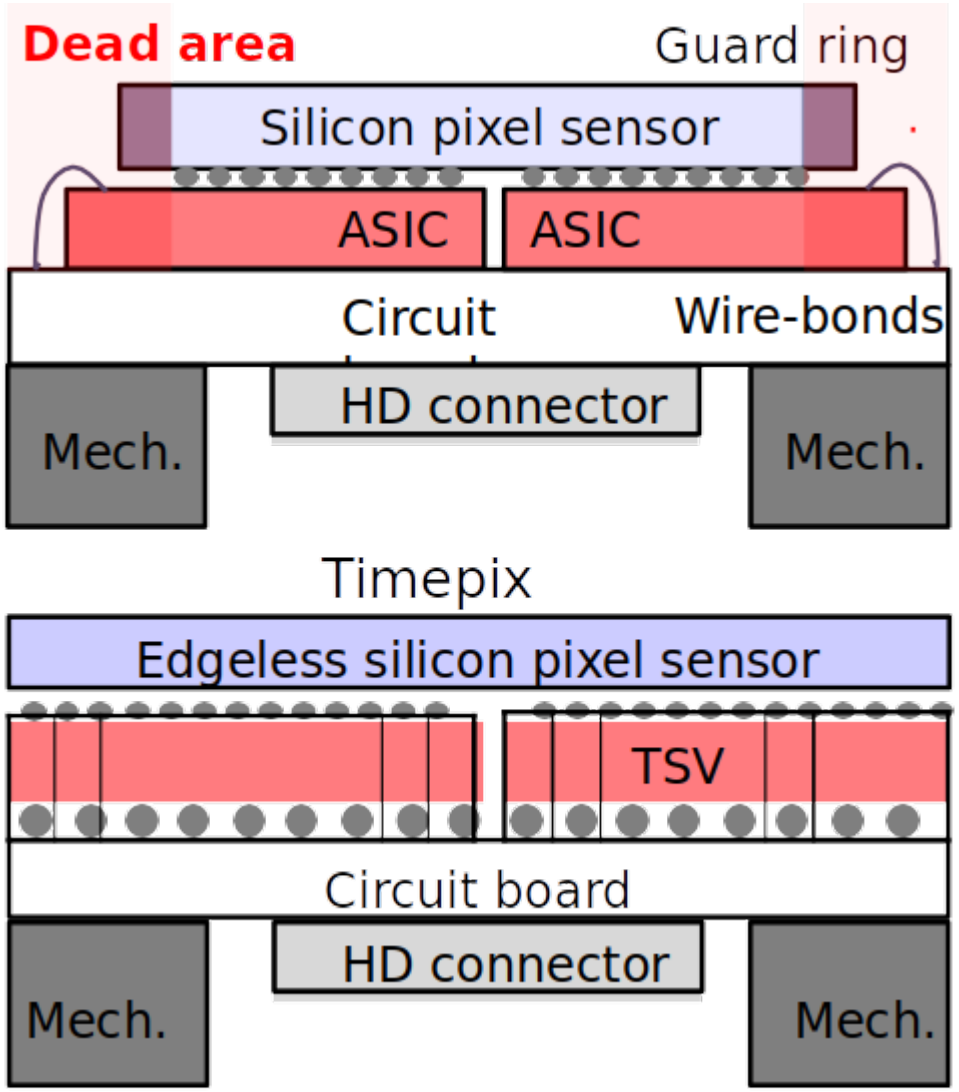
TSV technology

> Improved 4-side butting with Through Silicon Vias (TSVs)

- Full chip surface is covered with pixels
- Rerouting in metal layers creates space for periphery
- Improved TSV landing pads, redundant inputs, extra power TSV connections in center of chip







TEMPUS readout system

Conclusions

- Current LAMBDA systems ~ 2 kHz frame rates and large areas
- Current Timepix3 systems ~ 5ns time resolution with limited hit rate

TEMPUS readout system

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- We are developing TEMPUS using Timepix4
  - Improved photon counting and time stamping modes:
    - Higher frame rate ~ 40kHz
    - Hit rate compatible with more PETRA experiments
    - Much higher time resolution possible

TEMPUS readout system

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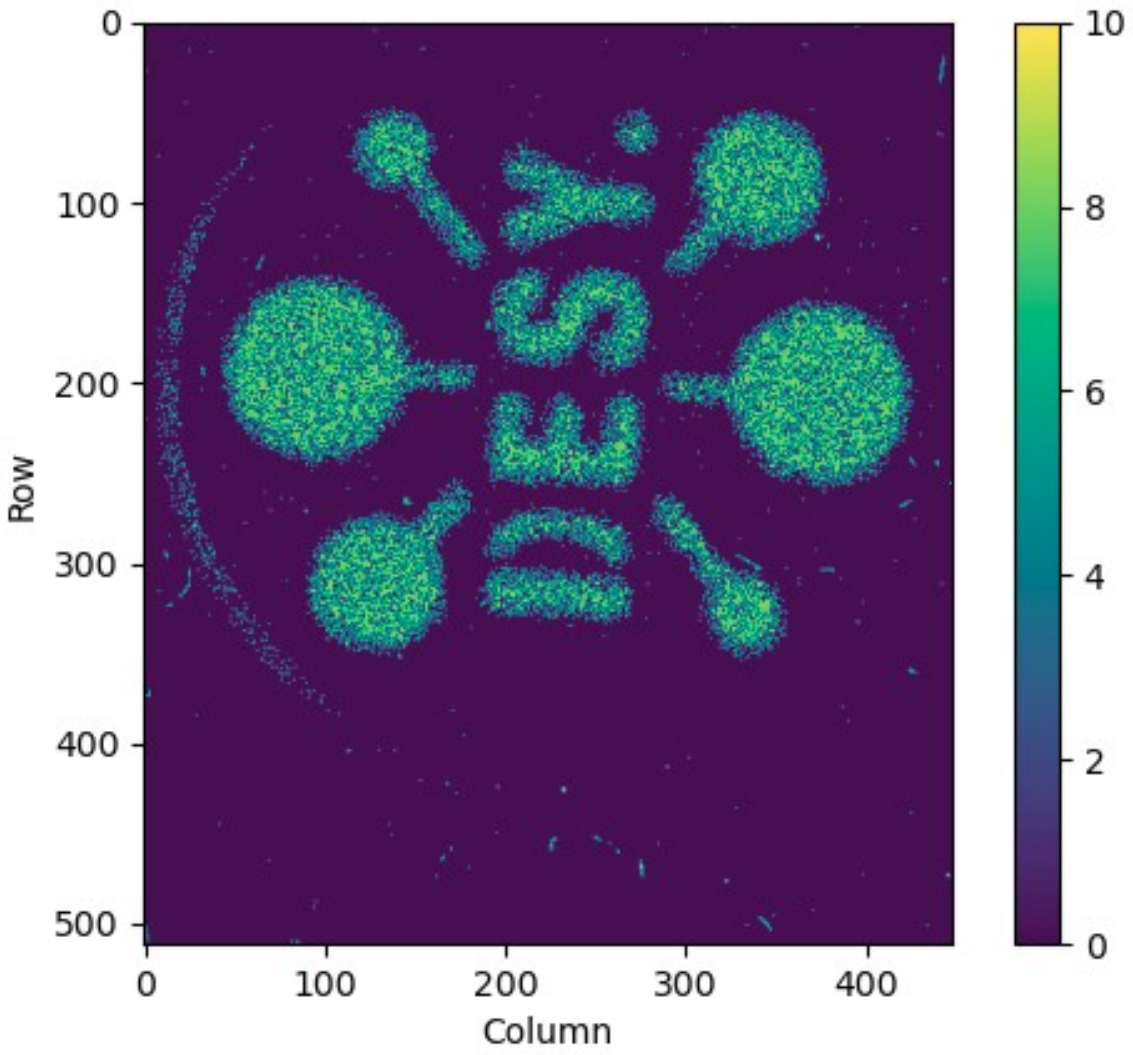
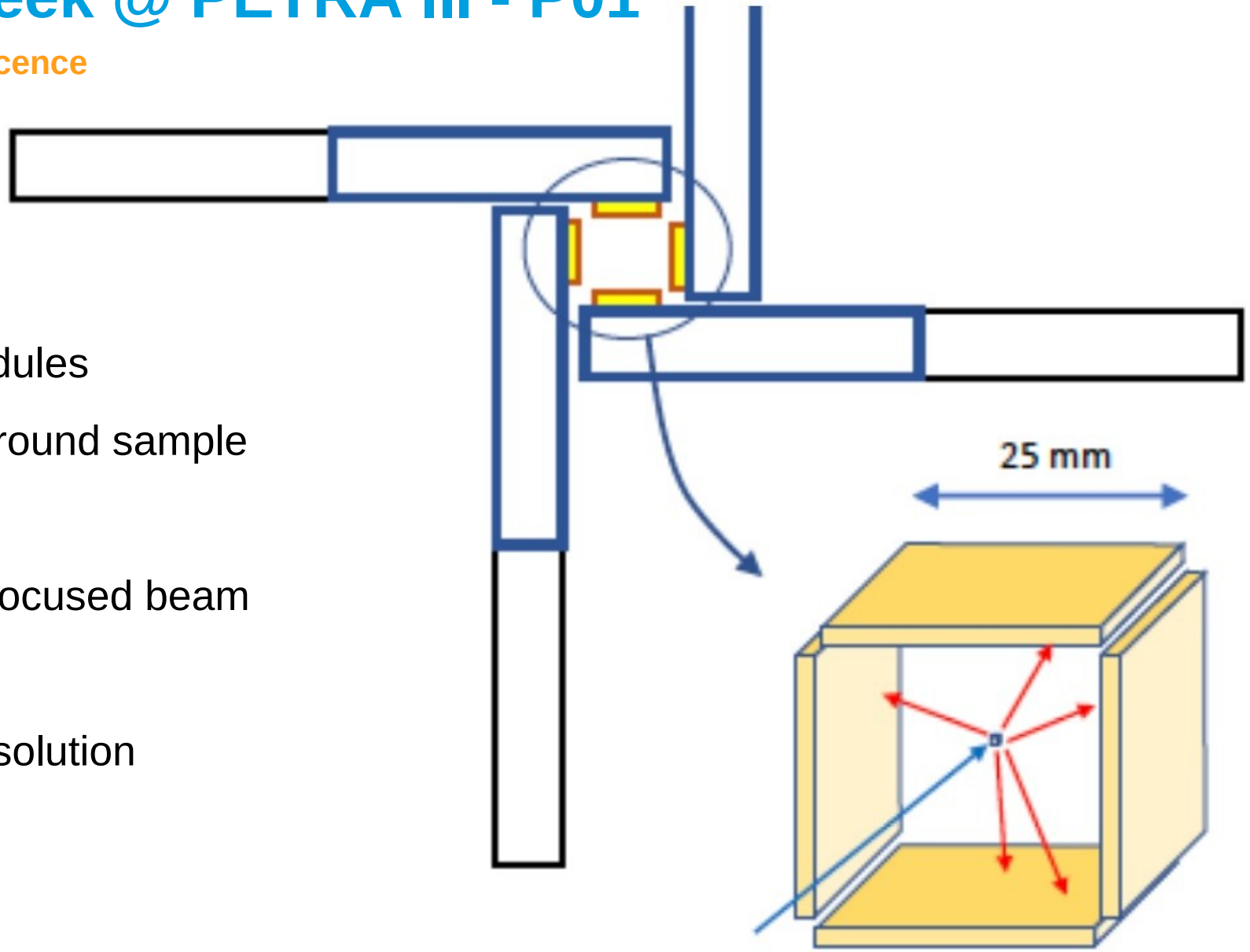


1st experiment next week @ PETRA III - P01

Quantum Imaging: X-ray nuclear fluorescence

- Arrangement of 4 single-chip modules
  - Covering 2/3 of solid angle around sample
- Sample illuminated with sub-um focused beam
- Event-based detection with ns resolution



TEMPUS readout system

Acknowledgments

> DESY / FS-DS – Photon Science Detector Group

> DESY / CFEL-CMI – Controlled Molecule Imaging

> The Medipix4 collaboration

> University of Jena

> X-Spectrum GmbH