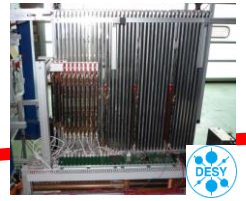
future ASICs for calorimetry at OMEGA

Ch. de LA TAILLE TIPP 2023

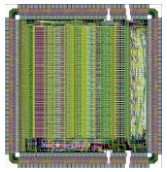
Organization for Micro-Electronics desiGn and Applications

ASICs produced and installed on detectors

Omega

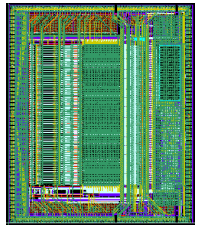


MAROC3

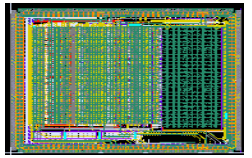


2006

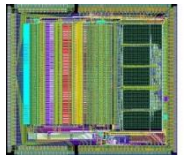
SKIROC



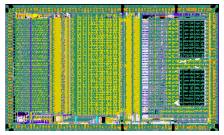
SPIROC



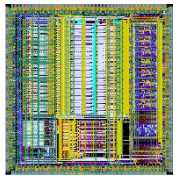
MICROROC



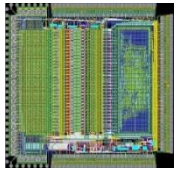
HARDROC



SPACIROC



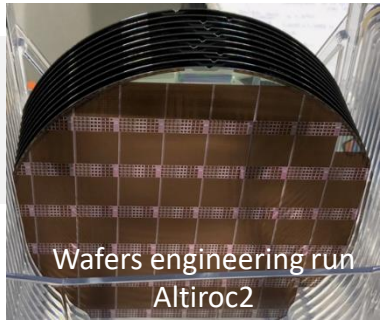
PETIROC



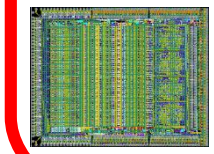
9 engineering runs in 9 years :

AMS SiGe 0,35um 2014, 2016, 2018

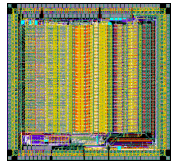
TSMC 130nm: 2019, 2020, 2021, 2022 and 2023 (x2)



TRIROC

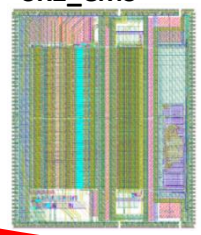


CITIROC

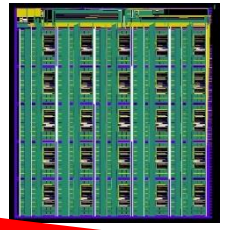


CATIROC

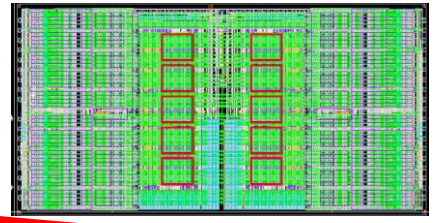
SK2_CMS



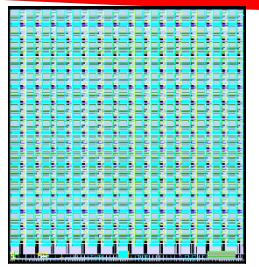
ALTIROC1



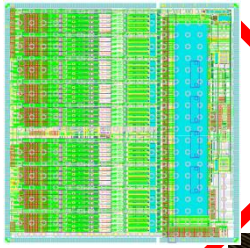
HGCROC



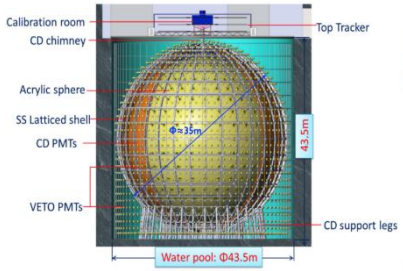
ALTIROC2



HKROC



2023



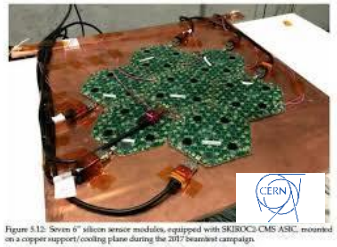
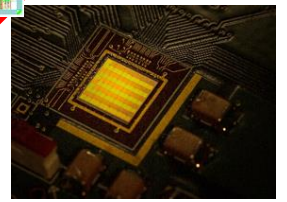


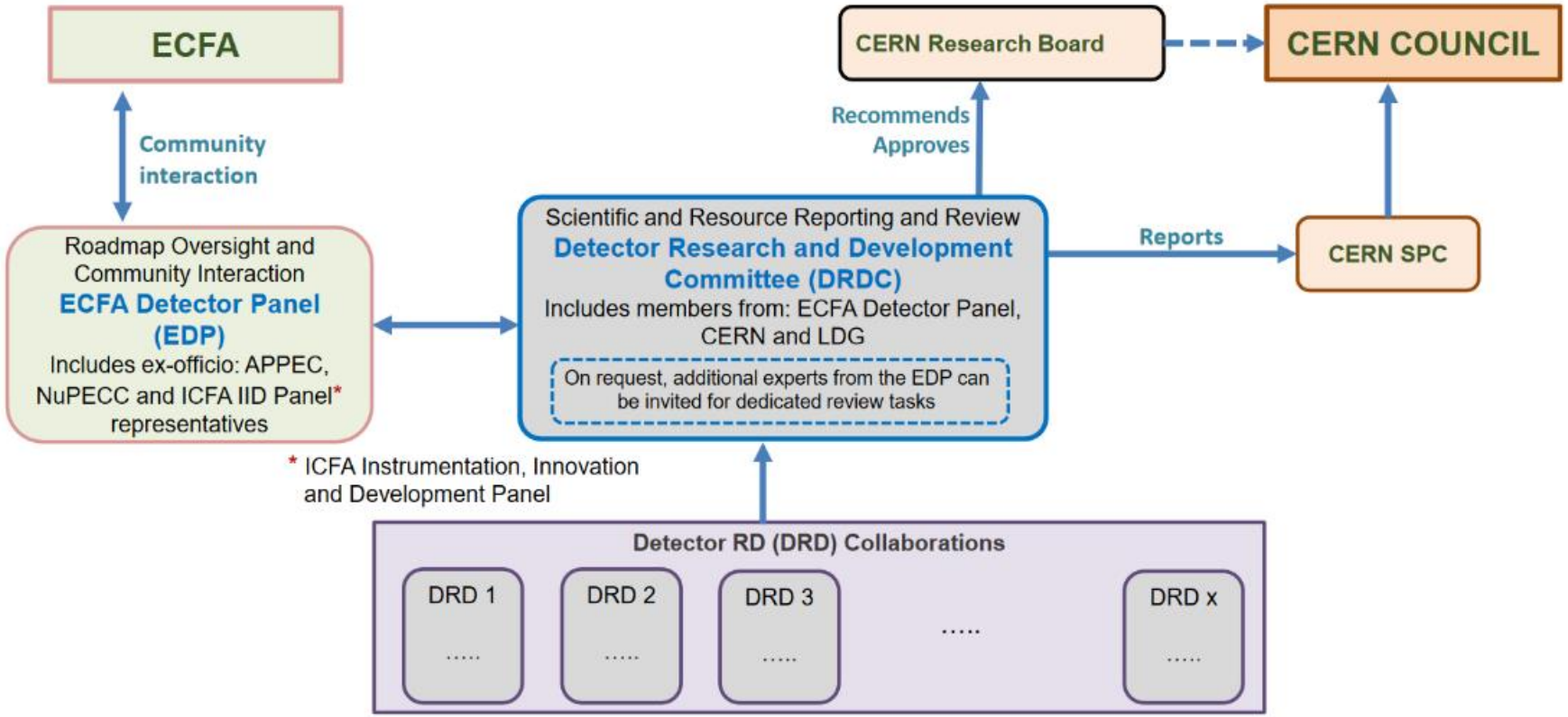
Figure 5.12: Seven 6" silicon sensor modules, equipped with SKIROC2-CMS ASIC, mounted on a copper support/cooling plane during the 2017 beamtest campaign.

ips for calorim



ECFA detector R&D roadmap [see talk by Th. Bergauer]

- DRD1 : gas detectors
- DRD2 : liquid detectors
- DRD3 : semiconductors
- DRD4 : photon detectors
- DRD5 : quantum
- DRD6 : calorimetry
- DRD7 : electronics



DRD6 (calorimetry) readout schemes

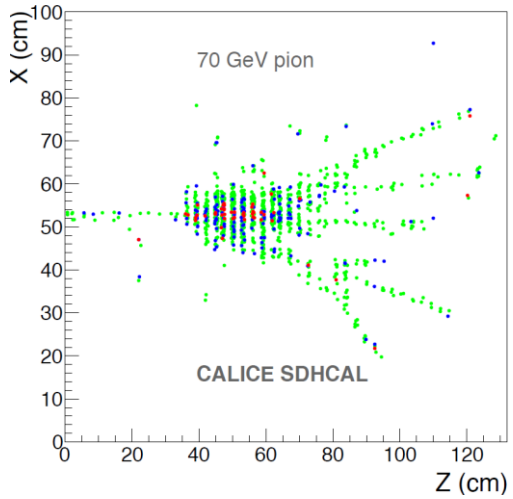
Name	Track	Active media	readout
LAr	2	LAr	cold/warm elx"HGCROC/CALICElike ASICs"
ScintCal	3	several	SiPM
Cryogenic DBD	3	several	TES/KID/NTL
HGCC	3	Crystal	SiPM
MaxInfo	3	Crystals	SIPM
Crilin	3	PbF2	UV-SiPM
DSC	3	PBbGlass+PbW04	SiPM
ADRIANO3	3	Heavy Glass, Plastic Scint, RPC	SIPM
FiberDR	3	Scint+Cher Fibres	PMT/SiPM,timing via CAENFERS, AARDVARC-v3,DRS
SpaCal	3	scint fibres	PMT/SiPMSPIDER ASIC for timing
Radical	3	Lyso:CE, WLS	SiPM
Grainita	3	BGO, ZnWO4	SiPM
TileHCal	3	organic scnt. tiles	SiPM
GlassScintTile	1	SciGlass	SiPM
Scint-Strip	1	Scint.Strips	SiPM
T-SDHCAL	1	GRPC	pad boards
MPGD-Calo	1	muRWELL,MMegas	pad boards(FATIC ASIC/MOSAIC)
Si-W ECAL	1	Silicon sensors	direct withdedicated ASICS (SKIROCN)
Si/GaAS-W ECAL	1	Silicon/GaAS	direct withdedicated ASICS (FLAME, FLAXE)
DECAL	1	CMOS/MAPS	Sensor=ASIC
AHCAL	1	Scint. Tiles	SiPM
MODE	4	-	-
Common RO ASIC	4	-	common R/O ASIC Si/SiPM/Lar

Trends for calorimeter readout

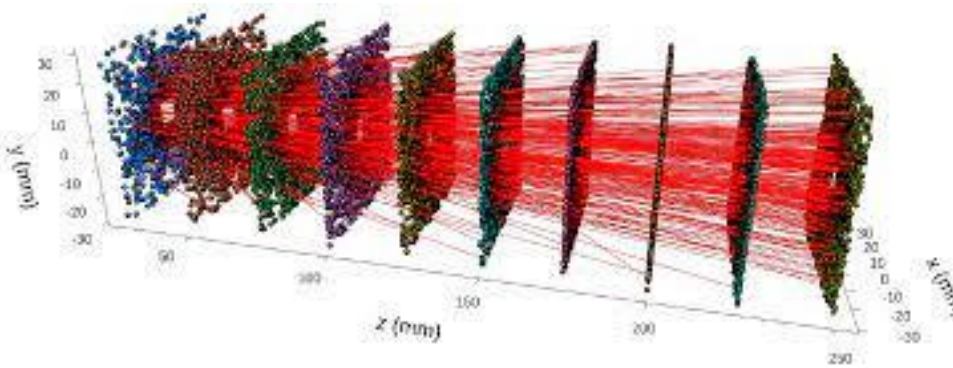
- On-detector embedded electronics, low-power multi-channel ASICs
  - CALICE SKI/SPI/HARDROC, FLAME, CMS HGCROC, FCC LAr, FATIC…
  - Challenges : #channels, low power, digital noise, data reduction
- Off-detector electronics : fiber/crystal readout
  - Wavefrom samplers : DRS, Nalu AARD, LHCb spider…
  - Challenges : low power, data reduction
- Digital calorimetry : MAPs, RPCs…
  - DECAL, ALICE FOCAL, CALICE SDHCAL
  - MAPS for em CAL : eg ALPIDE ASIC for FOCAL, DECAL…
  - Challenges : #channels, low power, data reduction

Digital calorimetry

- Hadronic : e.g. CALICE RPCs or µmegas
  - ~1 cm² pixels, low occupancy, ~1 mW/cm² (unpulsed)
  - Performance improvement with semi-digital architecture
  - Timing capability can be added



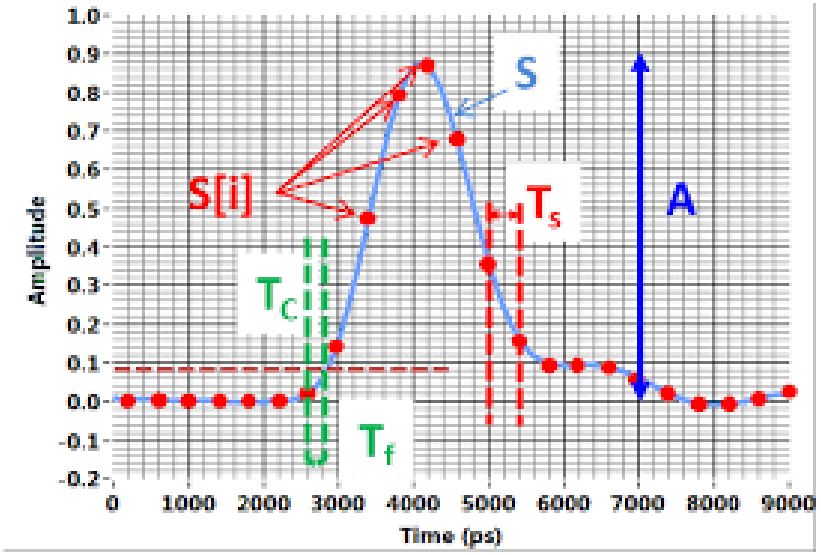
- Electromagnetic : e.g. DECAL, ALICE FOCAL…
  - Based on ALPIDE : (30µm)² pixels, high occupancy, ~ few 100 mW/cm², slow
  - To be compared with embedded electronics ~10 mW/cm²
  - Most power in digital processing => would benefit a lot from ≤ 28 nm node
  - Semi-digital and/or larger pixels couldl be an interesting study

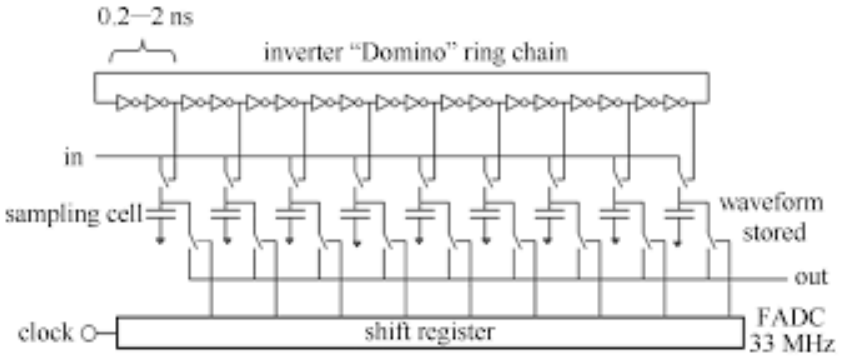


Waveform sampling

- Switched capacitor arrays (DRS4, Nalu, SAMPIC…)
  - Pulse shape analysis
  - High accurcay timing, digital CFD
  - Sizeable power to provide GHz BW on large capacitance
  - large data volume

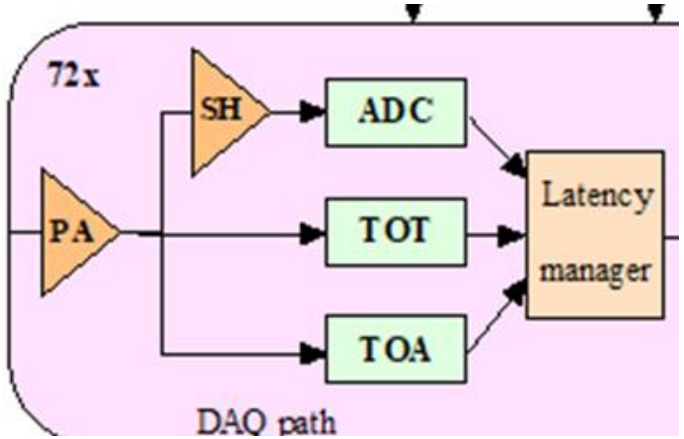
- Often used in off-detector electronics
  - Space and cooling available
  - Small/medium size detector readout and/or characterization
  - See LHCb calorimeter upgrade



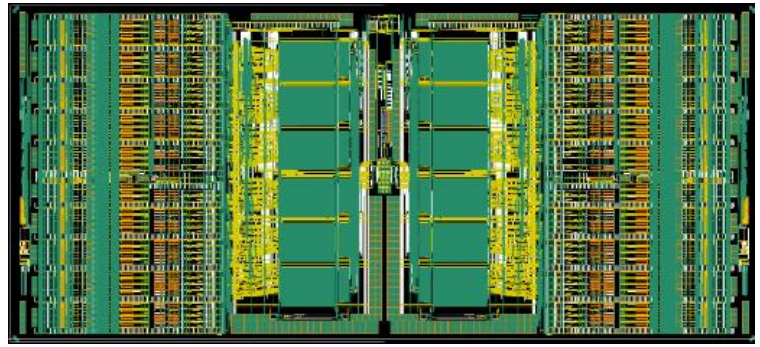


Embedded ASICs

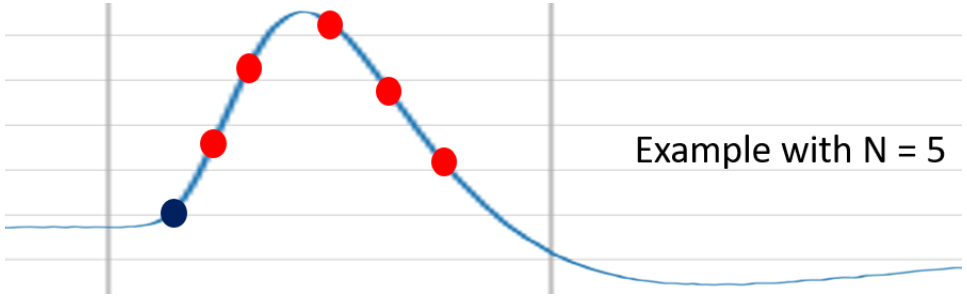
- Pioneered with CALICE R&D (SKIROC, SPIROC..)



- Multi-channel charge/time readout
  - Fast preamp
    - Full dynamic range. Possible extension with ToT
  - Fast path for time measurement (ToA)
    - High speed discriminator and TDC
    - Time walk correction with ADC (or ToT)
  - Slow path for charge measurement
    - ~10 bit ADC ~40 MHz
  - Low power for on-detector implementation (~10 mW/ch)



- Difficulties
  - Analog/digital couplings



Example : HGCROC (CMS HGCAL)

Overall chip divided in two symmetrical parts

- Each half is made of:
  - 39 channels: 36 channels, 2 common-mode, 1 calibration
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

Measurements

- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.16 fC binning. TOT: 2.5 fC binning
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

Two data flows

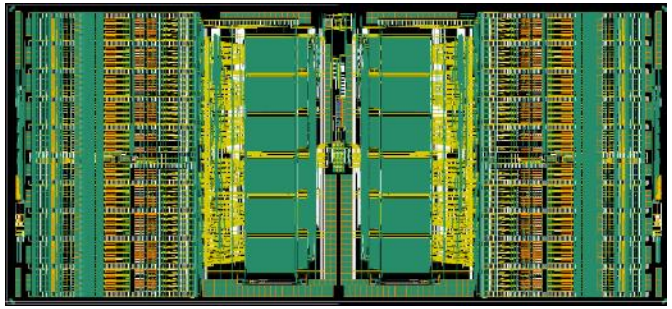
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links (CLPS)
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links (CLPS)

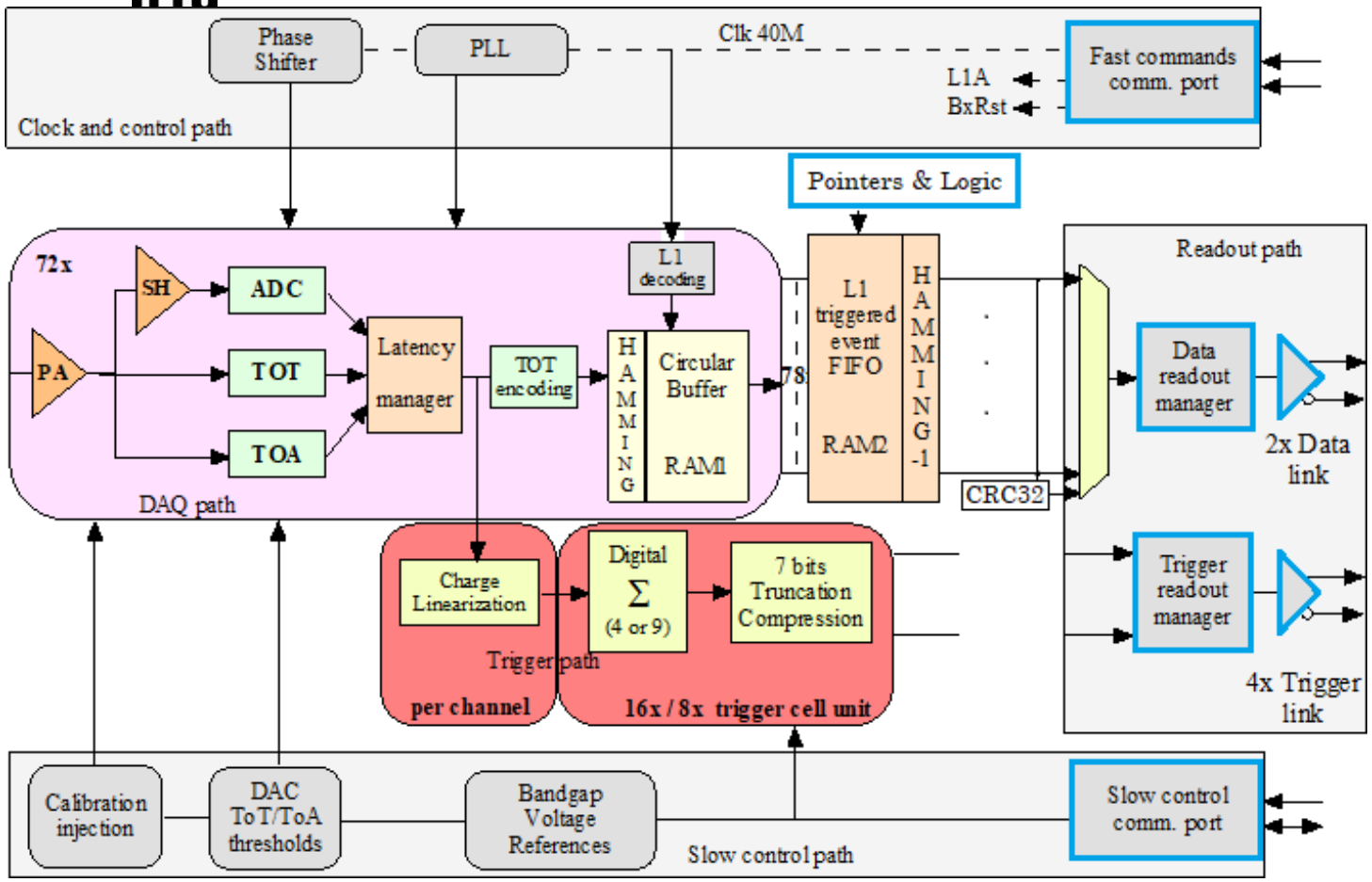
Control

- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

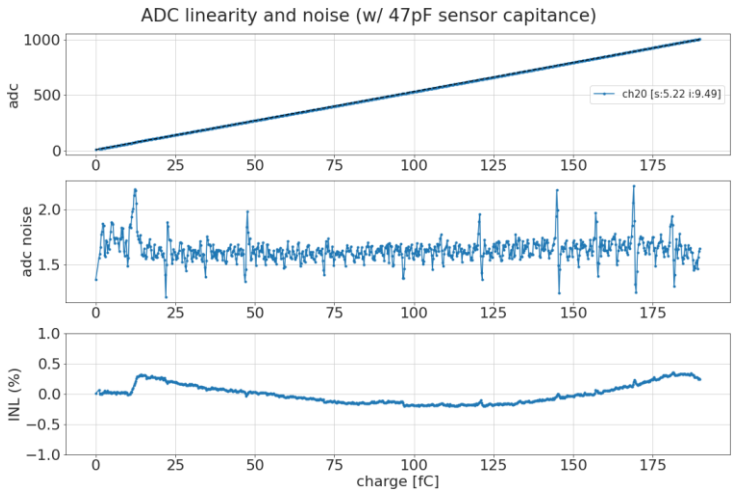
Ancillary blocks

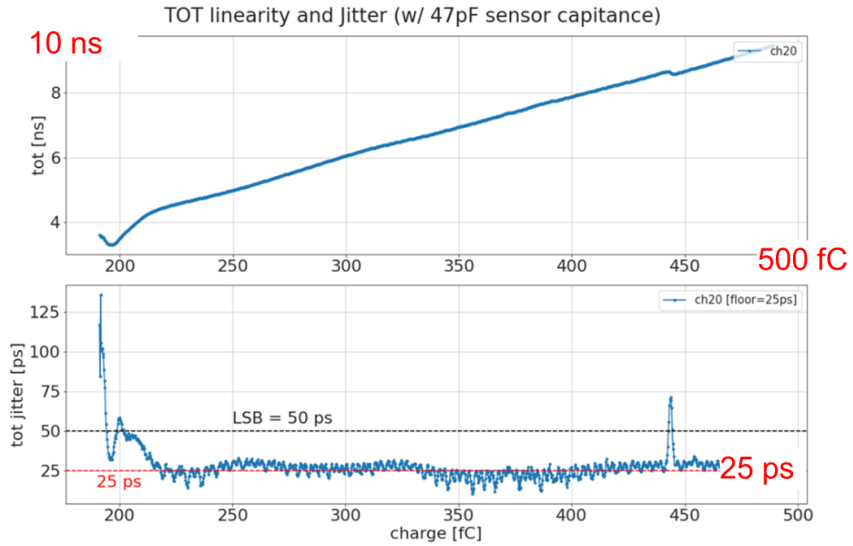
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

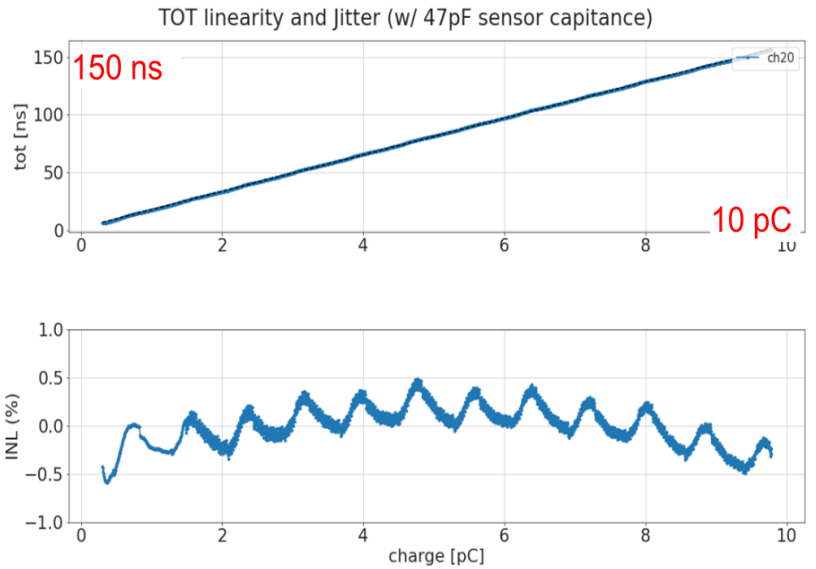


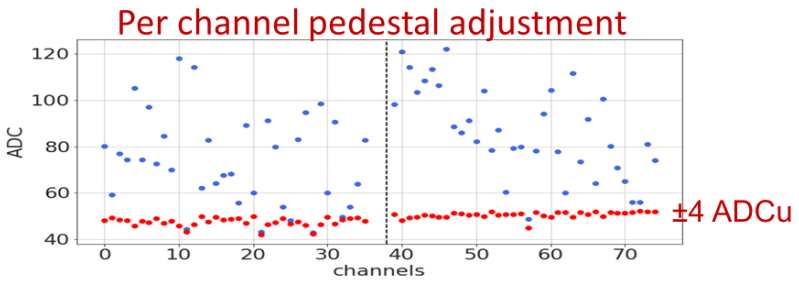


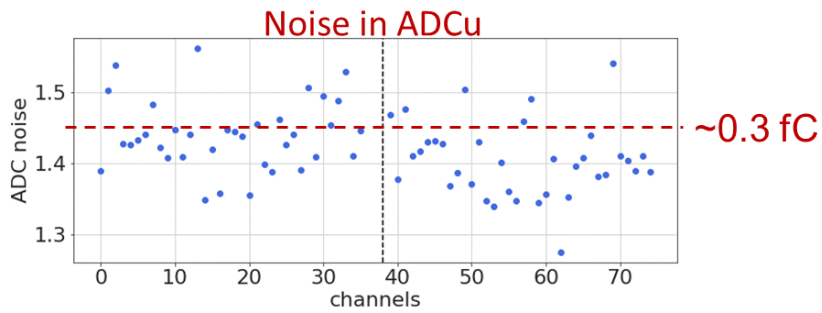
Performance

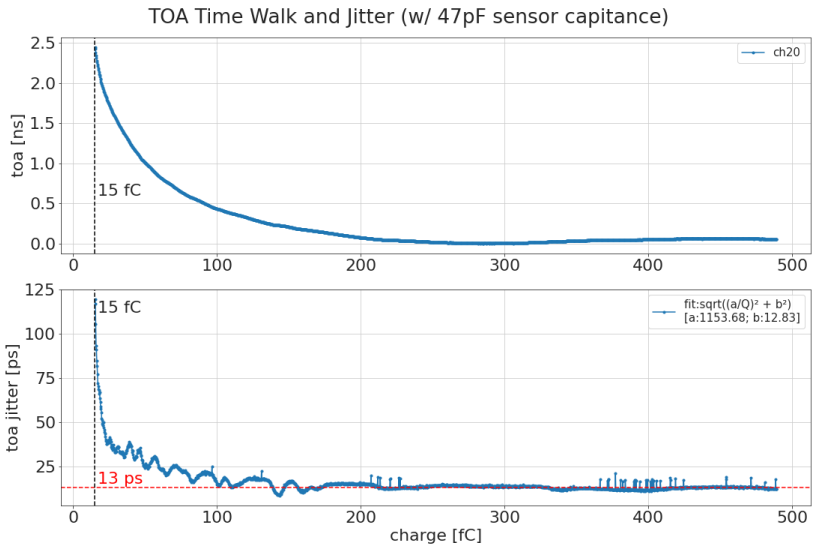






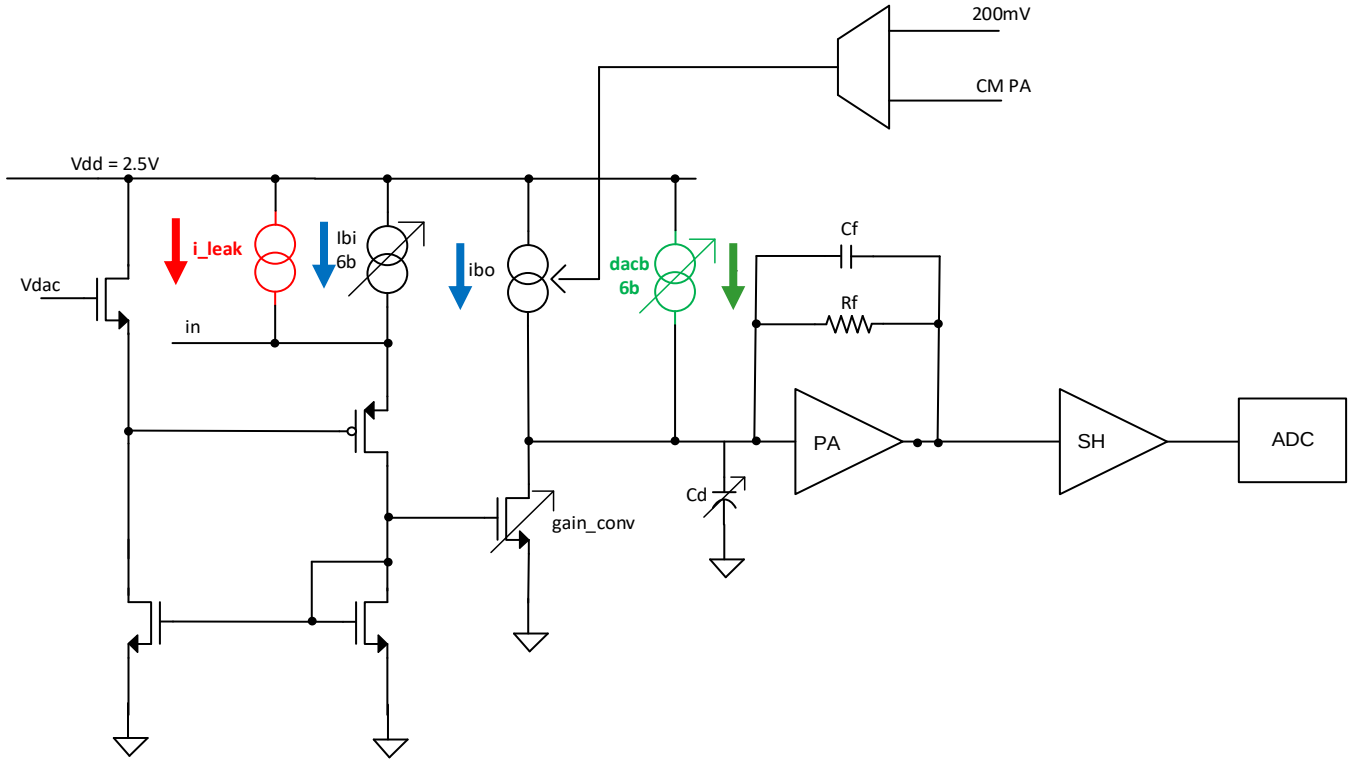


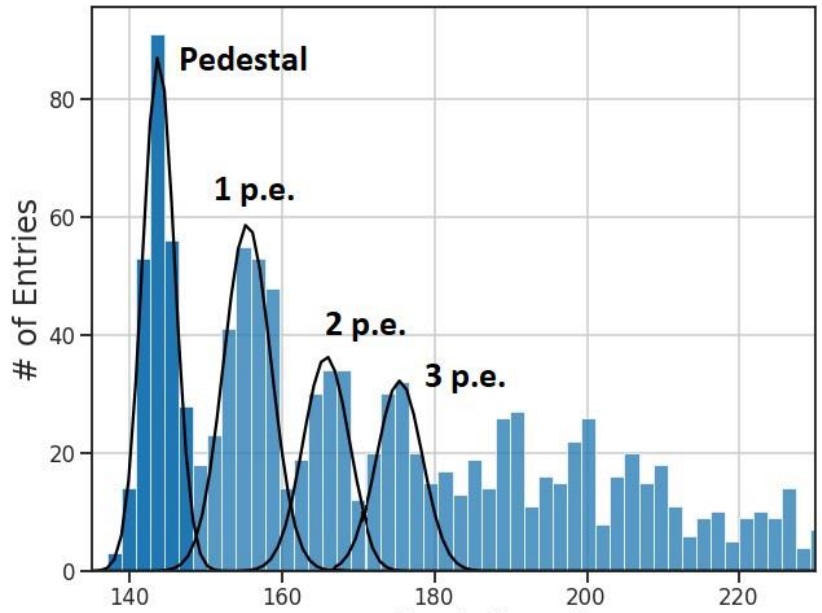


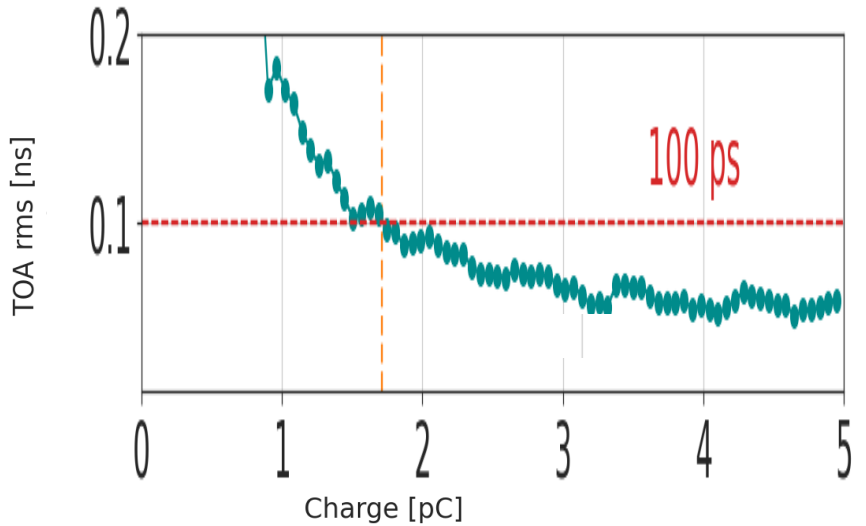


H2GCROC: SiPM version current conveyor

- **Current conveyor (Heidelberg design) to adapt to Si version**
- **Dynamic range : 50 fC – 300 pC**
- **2 typical gains**
  - Low gain (Physics mode): **44 fC/ADC gain, 50 fC noise (1.25 ADCu)**
  - High gain (Calibration mode): **10 fC/ADC gain, 20 fC noise (2 ADCu)**





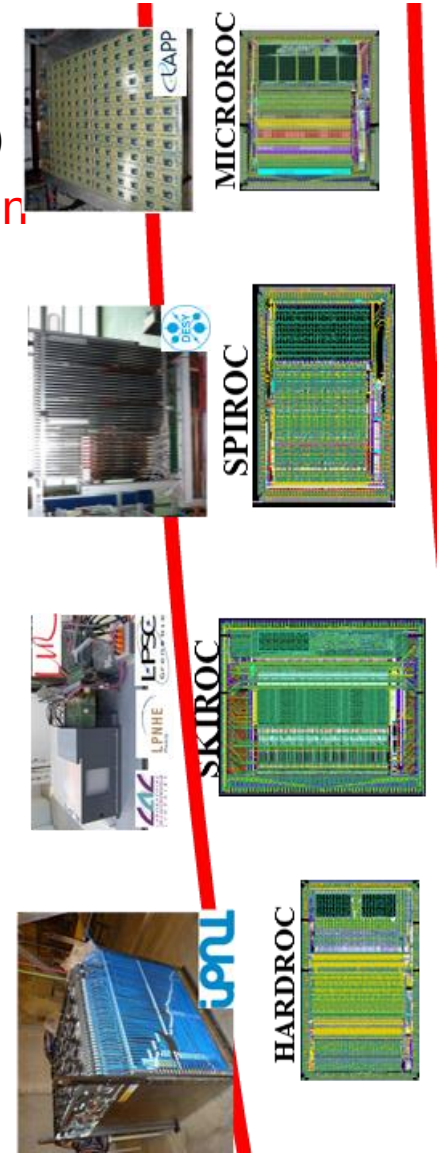


DRD6 Common readout ASICs proposal [AGH, Omega, Saclay]

- Develop readout ASIC family for DRD6 prototype characterization
  - Inspired from CALICE SKIROC/SPIROC/HARDROC/MICROROC family
  - Targeting future experiments as mentionned in ICFA document (EIC, FCC, ILC, CEPC…)
  - Addressing embedded electronics and detector/electronics coexistence + joint optimization
  - Detector specific front-end but common backend
  - ⇒ allows common DAQ and facilitates combined testbeam

- Start from HGCROC / HKROC : Si and SiPM
  - Reduce power from 15 mW/ch to few mW/ch. Lower occupancy, slower speed
  - Allows better granularity or LAr operation
  - Remove HL-LHC-specific digital part and provide flexible auto-triggered data payload
  - *See talk on HKROC by Rudolph Rogly*
  - Extend to MCPs (PID) or HRPPD. First tests with EIC calo/PID

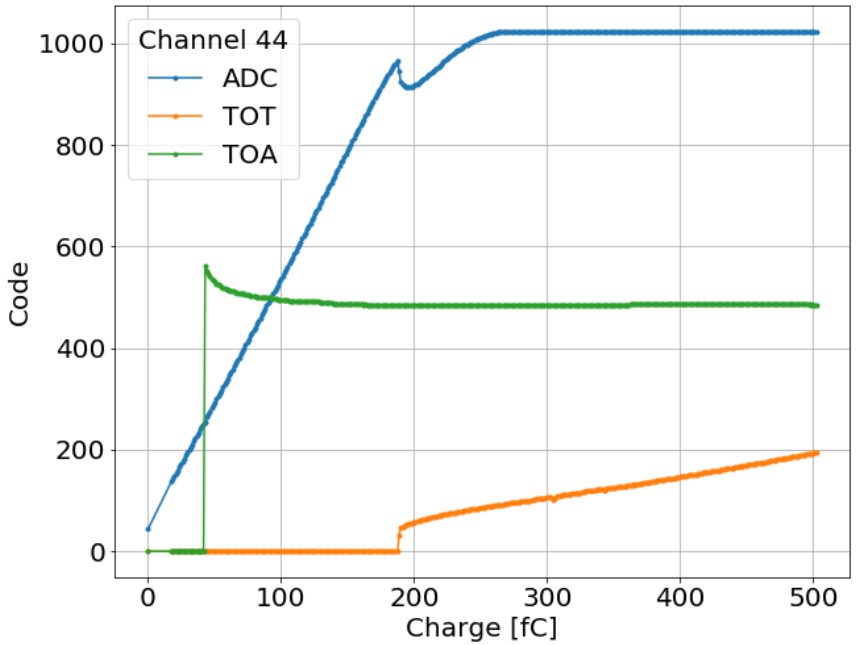
- Several other ASICs R/Os also developed in DRD6 and it is good !
  - FLAME/FLAXE, FATIC…
  - Waveform samplers : commercial or specific (e.g. SPIDER)
  - DECAL

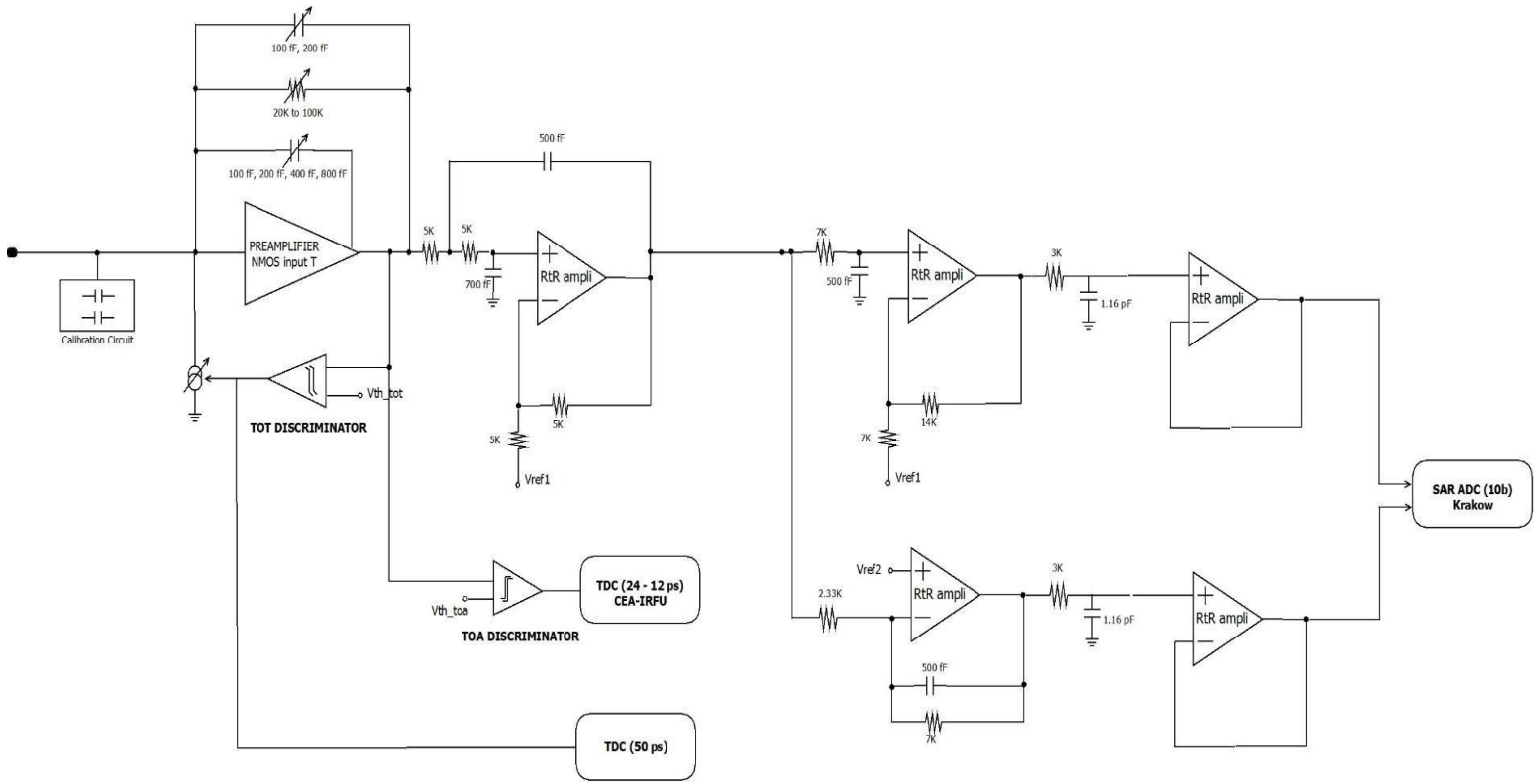


HGCROC : ADC and TOT

- ADC range 0 - 200 fC
- TOT range 200 fC - 10 pC
- Non-linear inter-region
- 200 ns dead time
- Not well adapted to SiPM version

=> go to dynamic gain switching



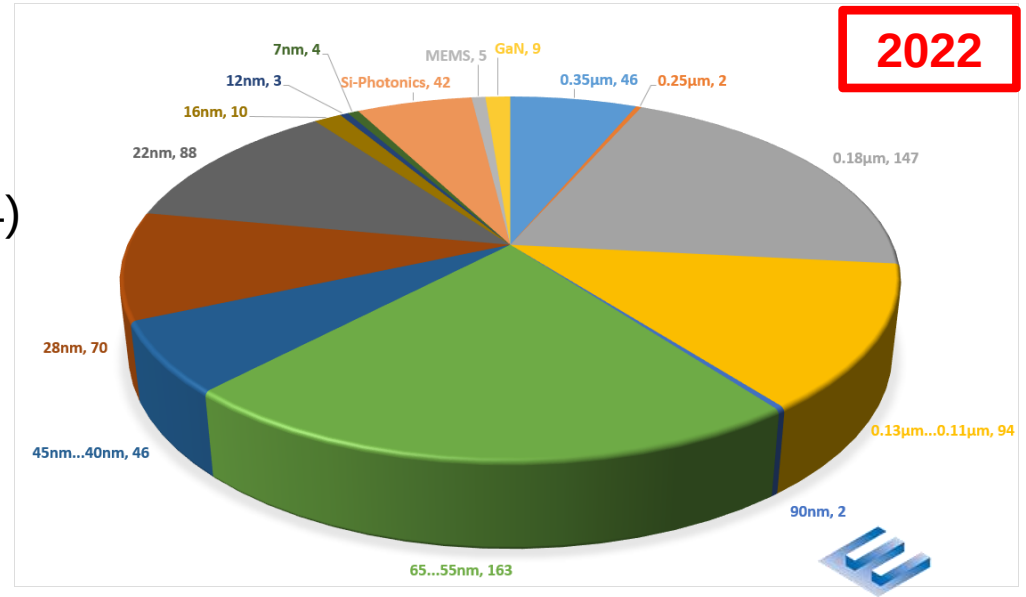


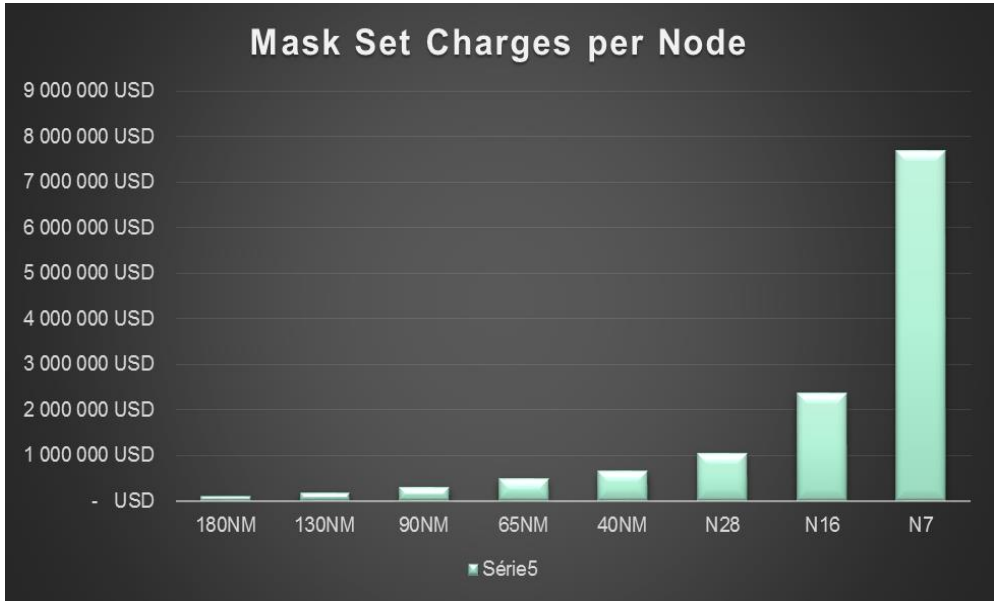
Technology choice for mixed signal ASICs

- TSMC 130nm : mixed signal, cheap
  - Very mature technology with good analog performance
  - 2.5 k€/mm² MPW, 300-350 k€/engineering run (20 wafers C4)
  - Perenity ?

- TSMC 65 nm : mixed signal, main stream
  - ~2-3 times lower power in digital, similar in the analog (compared to 130n)
  - 5 k€/mm², 700-800 k€/ engineering run

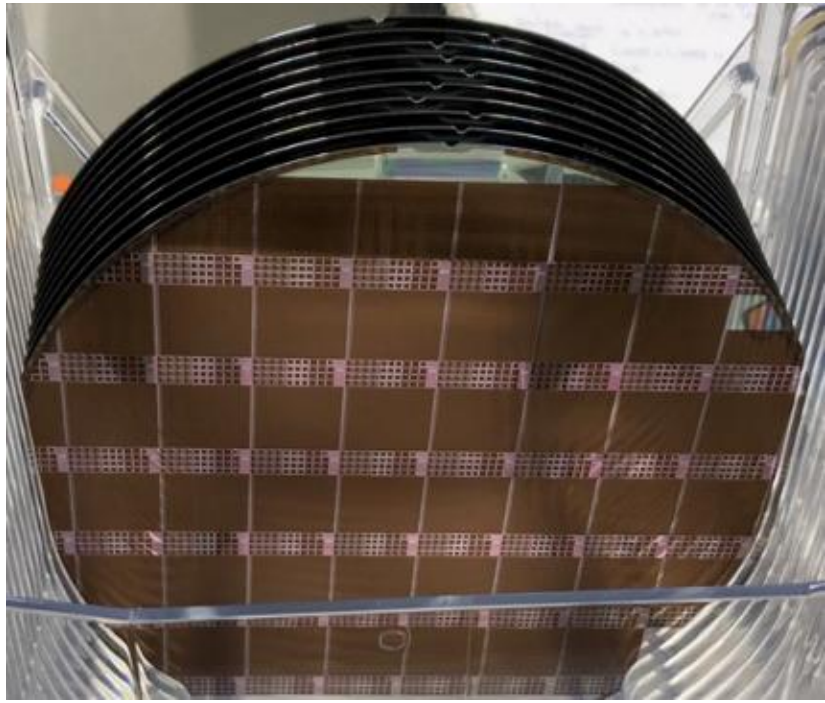
- TSMC 28 nm : digital oriented
  - High density integration (pixels)
  - High performance, lower power digital, similar in the analog
  - 10 k€/mm², 1-1.5 M€/ eng run





conclusion

- Importance of joint optimization detector/readout electronics



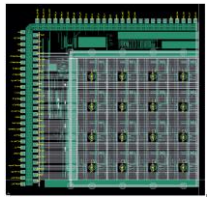
- Trend to reduce power and data volume
  - Pileup will be less of an issue, better granularity will be appreciated !
  - Low occupancy, auto-trigger, data-driven readout
  - Low power ADCs and TDCs (DRD7 with AGH&CEA)
- Picosecond Timing important R&D area
  - PID and/or calorimetry, several new detectors appearing : need R/O
- Next chips at OMEGA will target EIC, DRD1-4-6-7
  - Calorimetry and timing
- Technology choice to be addressed in coordination with other design groups
  - Cost sharing for engineering runs

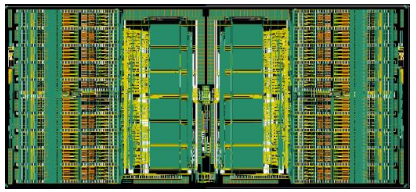
backup

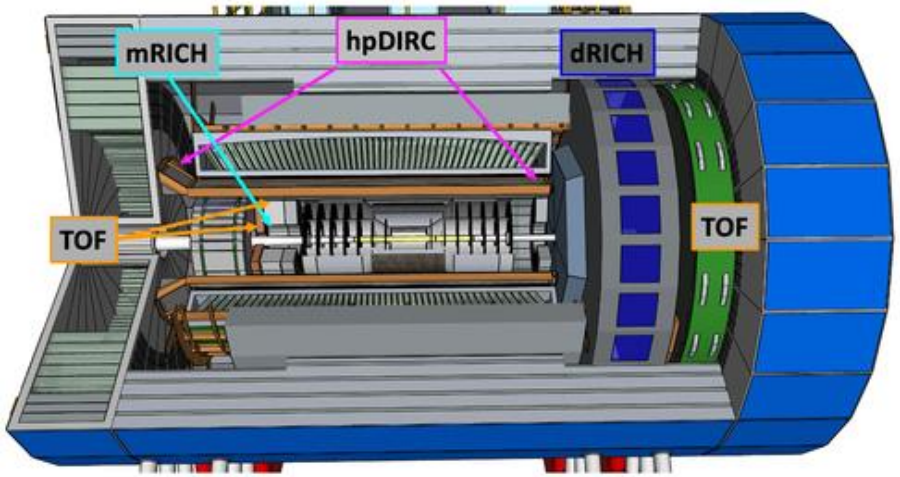
Chips for EIC : electron-ion collider at BNL

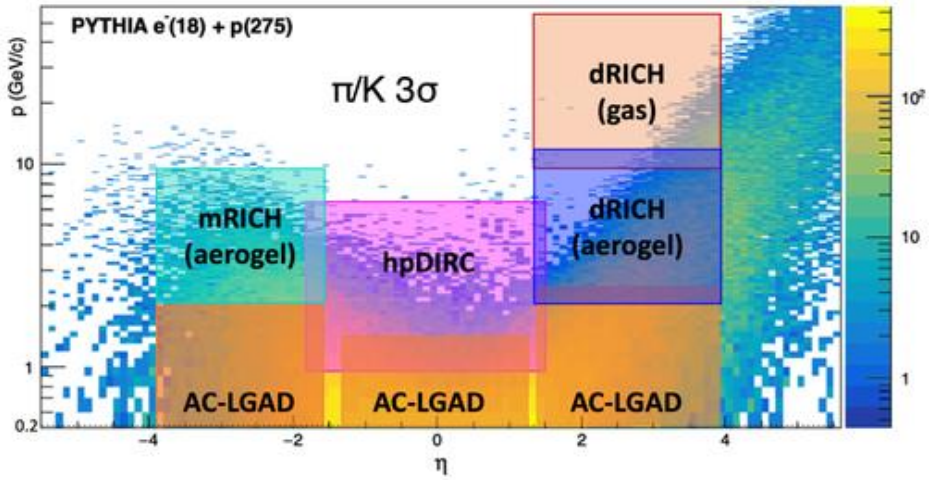
- PID and calorimeters
  - EICROC for AC-LGAD roman pots
  - HGCROC for calorimeters
  - « Event driven » DAQ

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		67k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	670k	100k
ASIC	ITS-3	EICROC FCFD HPsOC ASROC FAST	Discrete/COTS HGCROC3 ALCOR-EIC	SALSA

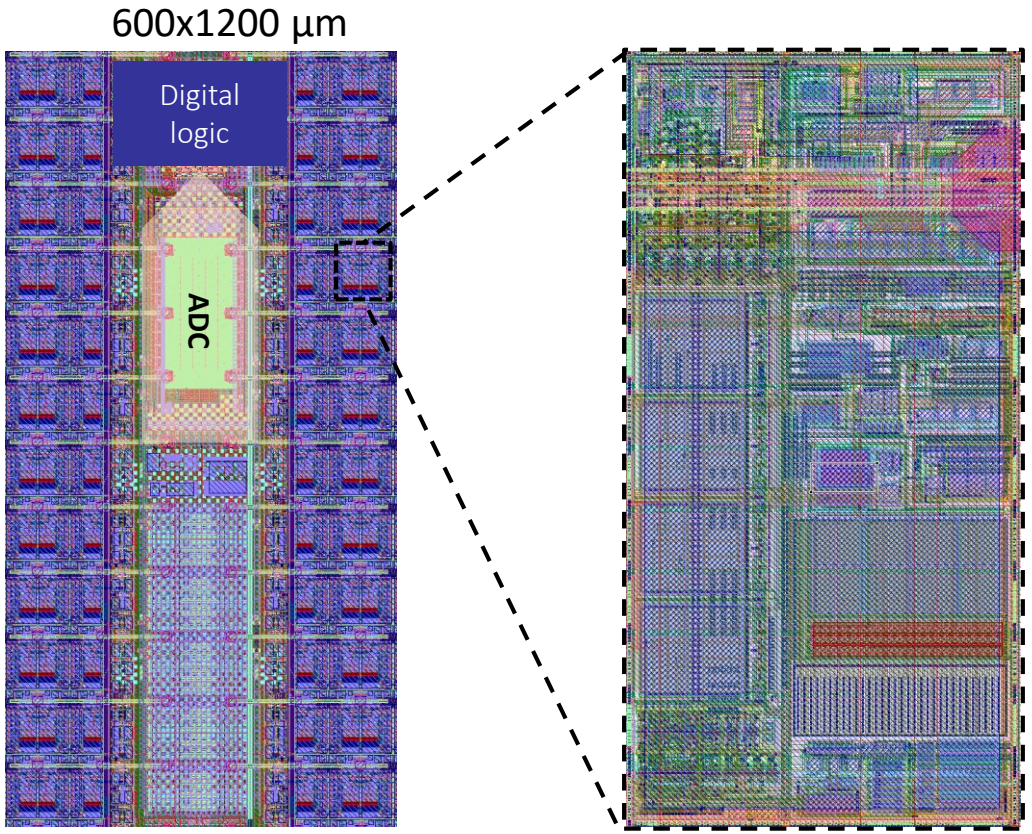








Dynamic gain switching : Pixel matrix [SLAC]

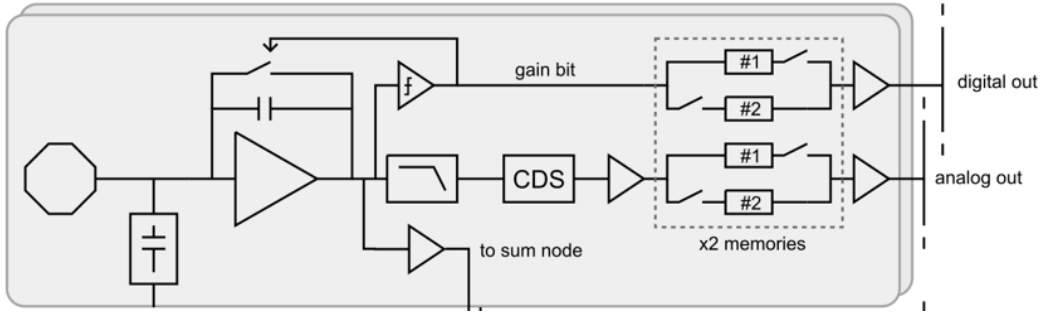


Cluster

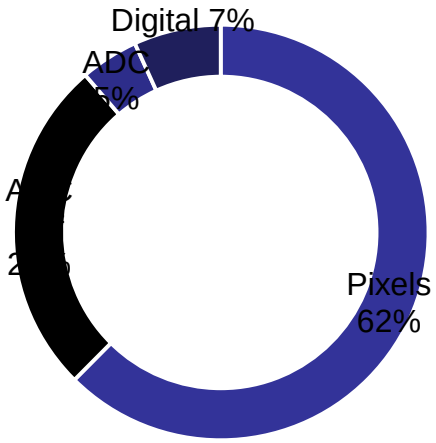
- 72 pixels → 1 ADC @ 8 MSPS
- Digital logic for pixel configuration and readout

Pixel

- Operates at 100 kHz – 1 MHz
- Si sensor: 100x100 µm^2
- ASIC: 50x100 µm^2



Pixel analog front-end block diagram



Power consumption of different blocks in matrix
(power density: 0.94 W/cm^2)