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## **ALICE Inner Tracking System upgrade: characterization of first chips fabricated in 65 nm CMOS technology**

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The Inner Tracking System of ALICE (A Large Ion Collider Experiment) will undergo a major upgrade during the next Long Shutdown of LHC aimed at enhancing the tracking capability. In particular, the three innermost sectors of the current vertex tracker will be replaced by truly cylindrical layers produced by using curved (wafer-scale) silicon sensors thinner than 50  $\mu\text{m}$ , based on monolithic active pixel structures realised in a 65 nm CMOS process. The innermost layer will be placed at only 18 mm of radial distance from the interaction point guaranteeing at the same time a material budget as low as 0.05% of a radiation length  $X_0$ .

The R&D on the sensor ASICs involves a series of submissions in silicon and the first one (named MLR1: Multi-Layer per Reticle 1) was completed at the end of 2020. MLR1 provided several test structures containing transistors, memories and small matrices of pixels with integration of front-end electronics inside the sensitive area of the pixels; these devices have been used to qualify the technology in terms of performance and radiation hardness. In particular, to evaluate the charged particle detection performance, this first submission includes 3 variants of pixel matrices: analog pixel test structure (APTS, 4x4 pixels of 10, 15, 20 and 25  $\mu\text{m}$  pitch, with analog readout); digital pixel test structure (DPTS, 32x32 pixels of 15  $\mu\text{m}$  pitch, with digital in-pixel discrimination and digital readout); CE65 (64x32 pixels of 15  $\mu\text{m}$  pitch, test structures with rolling shutter analog readout).

This contribution will provide an overview of these test structures, describing the results of characterisations performed with radioactive sources and beam tests in order to choose the best pixel pitch and sensor configuration, optimising timing, charge collection efficiency and stability after radiation damage. The obtained results show a satisfactory behaviour as 100% efficiency for charged particles in the range of GeVs and timing of few ns, giving the direction for the next submission (ER1: Engineering Run 1) directed to large, stitched sensor chips.

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