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FELIX Phase II, the ATLAS readout system for LHC Run 4

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The FELIX system has been introduced as a readout system for ATLAS in LHC Run 3, for a subset of the ATLAS subdetectors. An evolved version of FELIX, dubbed Phase II, will be deployed in Run 4 (2029 – 2032) and will serve all ATLAS subdetectors.
The FELIX Phase II system will be comprised of about 300 servers, each equipped with custom PCIe FELIX cards and a 400 GbE network interface. The system will receive detector data at the rate of 1 MHz for a total throughput of 4.6 TB/s.
The new FELIX PCIe card for Run 4, called FLX-182, is equipped with a Xilinx Versal Prime VM1802 FGPA/SoC, a PCIe Gen4x16 interface, four optical links to relay Timing, Trigger and Control information, and 24 optical links that operate up to 25 Gb/s to interact with the front-end electronics.
The FLX-182 runs FELIX firmware which has been redesigned and upgraded to deal with the higher data and trigger rates, as well as newly added communication protocols for the subdetectors in ATLAS. The firmware design has passed a preliminary design review in January 2022. The primary goals of the FELIX firmware are to decode and transfer the data from the front-ends into the host server memory and to receive and distribute precise timing, trigger and control information.
The software running on the FELIX server will also be upgraded to deal with the increased data and trigger rates.

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