SYSTEM DESIGN AND PROTOTYPING FOR THE CMS LEVEL-1 TRIGGER AT THE HL-LHC

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A. ZABI, ON BEHALF OF THE CMS COLLABORATION

OUTLINE

- **Context of triggering @ HL-LHC: scientific case and system requirements (technological choices)**

- **Phase-2 L1 trigger conceptual design and instrumentation: System interfaces & Architecture. Key features and hardware prototyping.**

- **Phase-2 Level-1 trigger algorithm design, firmware developments & testing: selecting physics with sophisticated firmware algorithms and expected performance. System demonstration.**

TRIGGERING @ HL-LHC

INTRODUCTION & DESIGN REQUIREMENTS

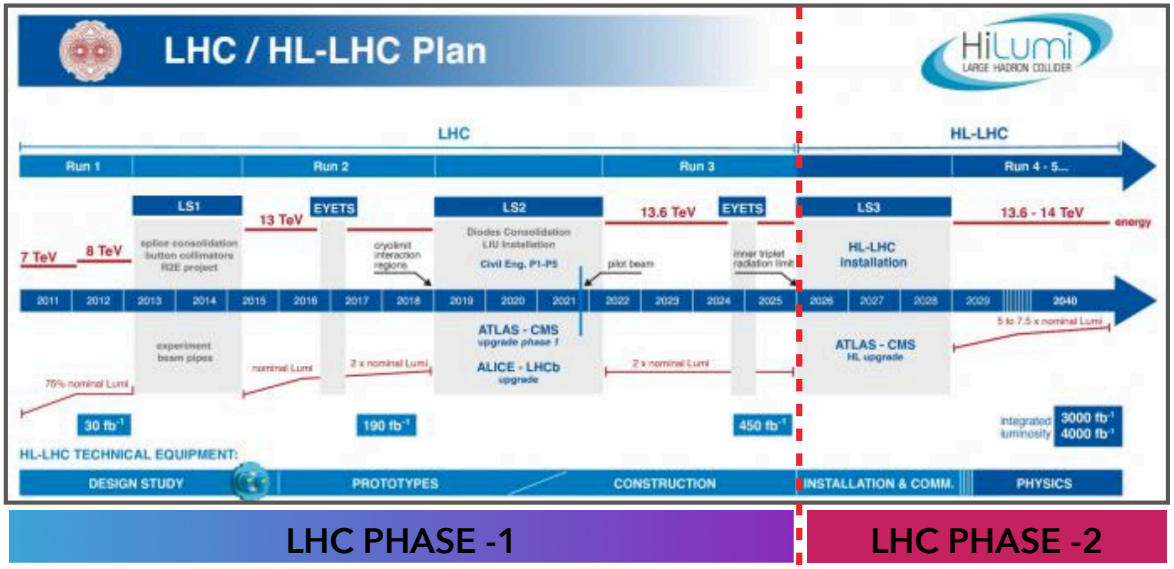
The scout of the HL-LHC

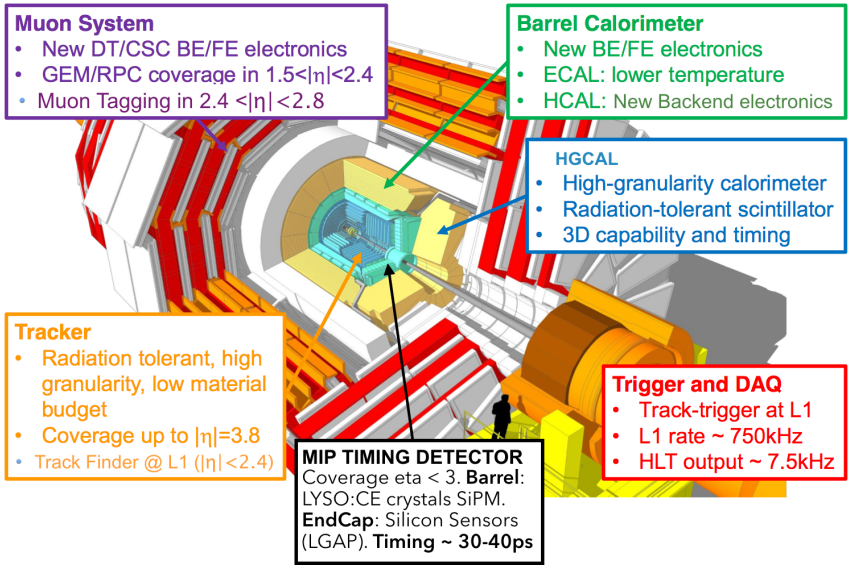
INTRODUCTION: CONTEXT OF TRIGGERING

- **HL-LHC Upgrade Project: offers an unprecedented opportunity to explore uncharted lands and achieve scientific progress.**
- **A new LHC machine and a new CMS Detector:**

The HL-LHC and the CMS Phase-2 detector

→ ***Set the context of triggering & define system requirements***





High-Luminosity-LHC: 13 TeV (Nominal : $5x10^{34}$ & 140 PU, Int Lumi = 3000 fb^{-1})

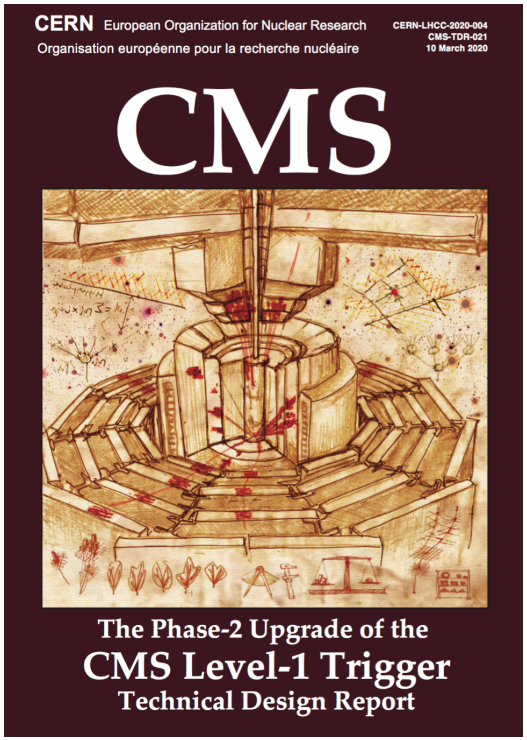
- **Ultimate: $7.5x10^{34}$ & 200 PU, Int Lumi = 4000 fb^{-1} (baseline for all TDR studies)**

→ ***unprecedented running conditions, exceeding machine design values 7 fold.***

PHASE-2 TRIGGER UPGRADE: KEY PARAMETERS & STRATEGY

- **CMS Phase-2 Trigger:**
  - CMS keeps a 2-level triggering approach: **L1 & HLT**
  - **Level-1 (hardware) system**
    - Increase bandwidth 100 kHz → 750 kHz
    - Increase latency 3.8 us → 12.5 us
- **Benefiting from upgrade of the CMS detector:**
  - Include high-granularity information (calo&μ)
  - Include tracking information (first time!)

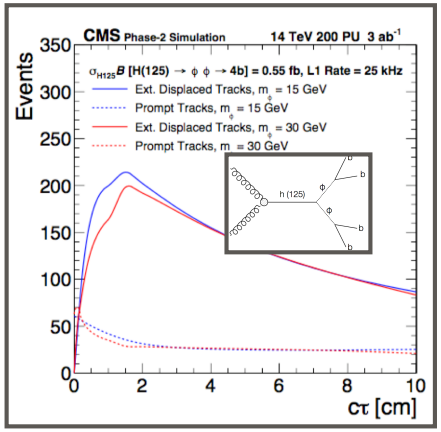
    → Manageable object rate (L1 Physics Menu)
- **Strategy:**
  - Exploit sub-detector back-end electronics
  - Sophisticated reconstructed objects and correlations → Enhanced physics selectivity
  - Expand reach with Scouting System

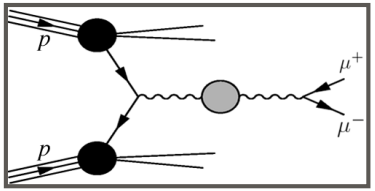


TDR approved in 2020

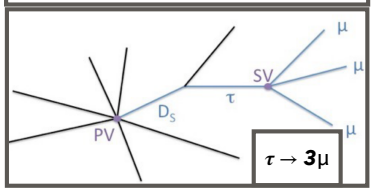
L1 PHASE II TRIGGER UPGRADE: SCIENTIFIC CASE

Maintaining thresholds is <u>NOT</u> the only motivation for upgrading the L1 trigger. HL-LHC research program opens a door to the unknown → **<u>the Phase-2 Level-1 Trigger system is our scout !</u>**
The goal is to extend the physics reach by increasing the available phase space



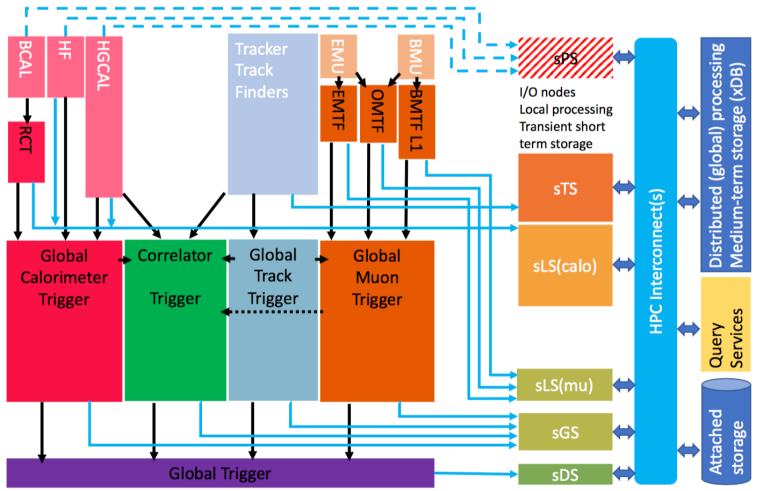


DarkPhoton(displaced mu)



L1 Trigger algorithm requirements:

- Object reconstruction closer to offline performance: higher-level trigger objects **(particle-flow)** w/ optimised response and resilient to pileup (up to 200)
- Sophisticated triggers to select specific topologies: VBF production, rare B-meson decays **(tracking@L1),** forward muon trigger for τ → μμμ **(muon extended coverage)**, dedicated algos for displaced jets and muons, etc.
- Expand reach: Low mass resonances



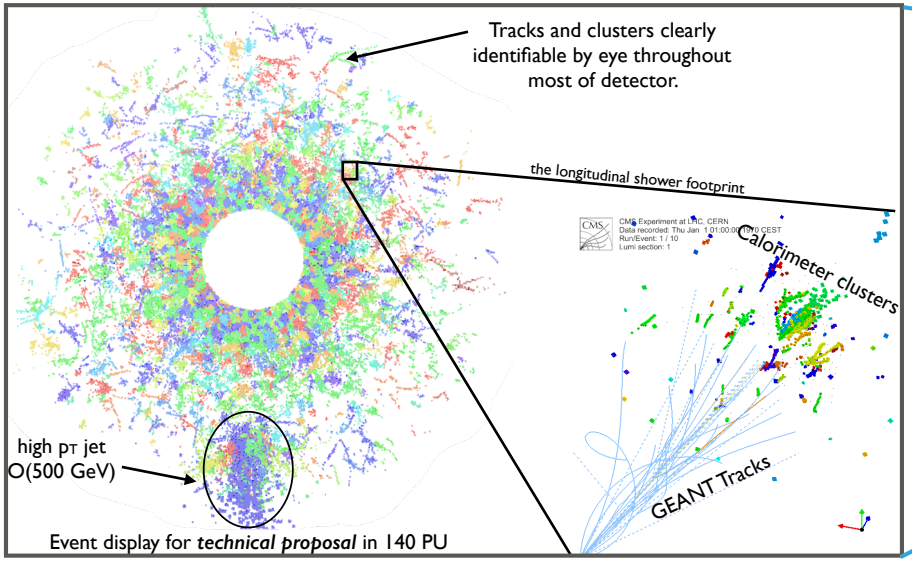
Scouting into HL-LHC data @ 40 MHz:

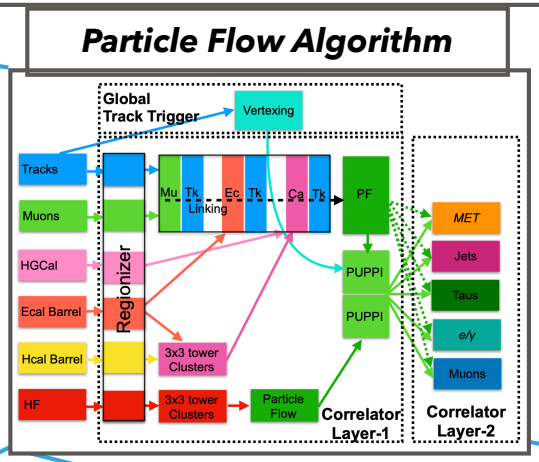
- Physics objects: reconstructed from L1 objects
- Storage: Only high-level information (selected events)
- Specific features: analyse multiple contiguous BX, identify signatures unreachable through standard trigger techniques

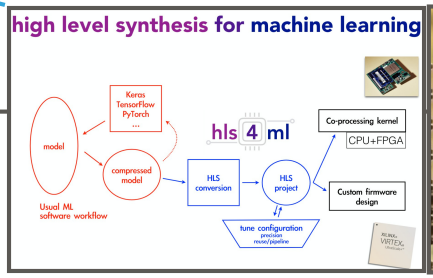
L1 PHASE II TRIGGER UPGRADE: TECHNOLOGICAL CASE

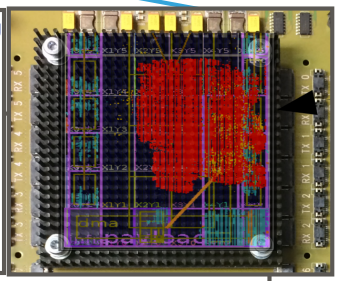
The Phase-2 Level-1 Trigger system performs precise physics selection using a global event reconstruction based on enhanced granularity already at hardware level.

Considering: Inputs > **70 Tb/s** (vs 2 Tb/s during LHC Phase-1), operate: 7.5e34 along w/ 200 PU events



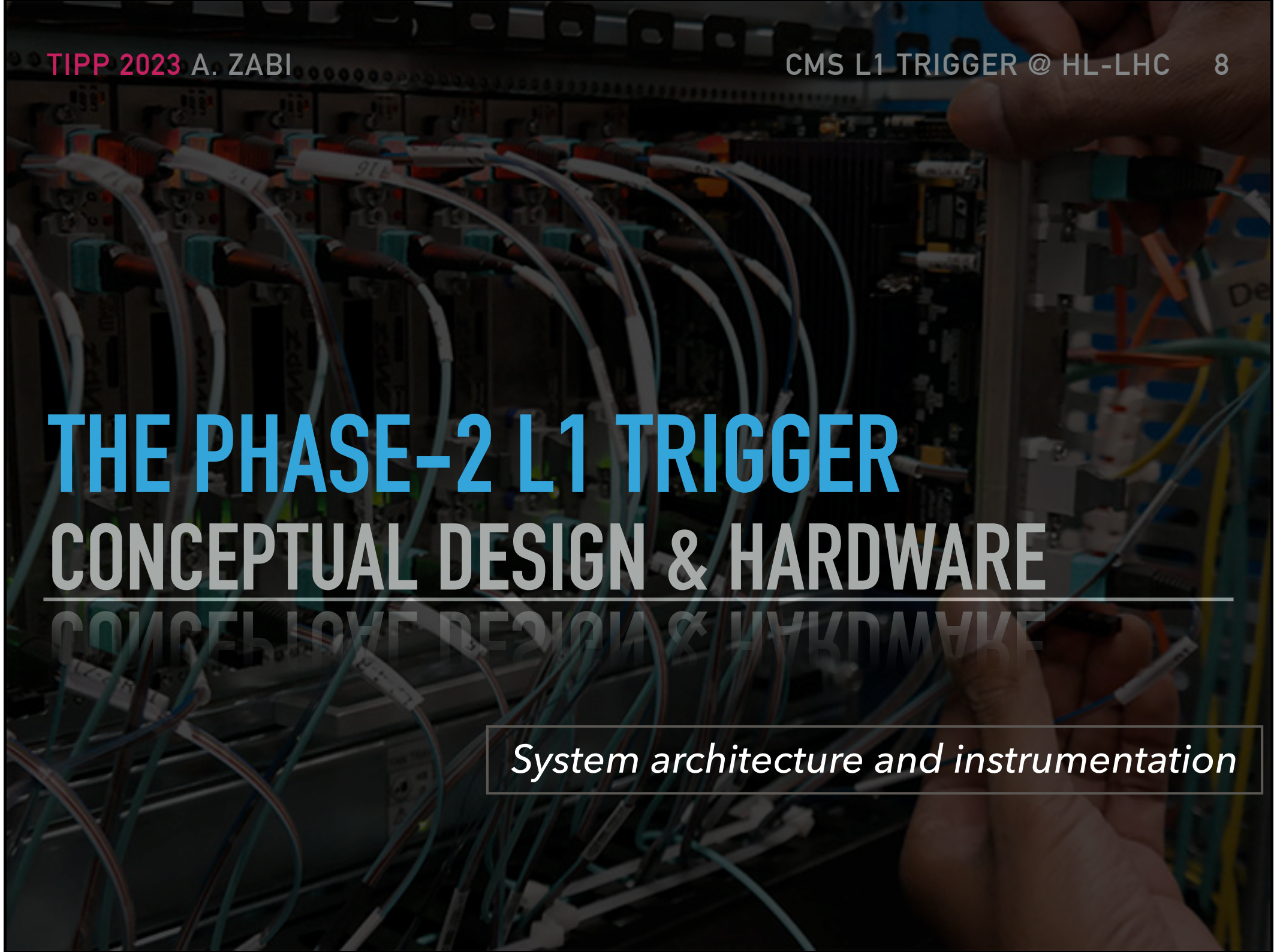






L1 Trigger requirements:

- Cutting-edge hardware: modern technology
  → FPGA VU9P x 8 resources of Virtex 7 (Phase-1), 28 Gb/s links
- High-Level-Synthesis: used successfully, much faster turn-around, novel techniques based on machine learning → *The Phase-2 L1 Trigger can do much more!*
- Advanced Architecture: platform and interconnections (ATCA) → robust, flexible & modular design
- Handling all technical issues: integration, commissioning, etc.

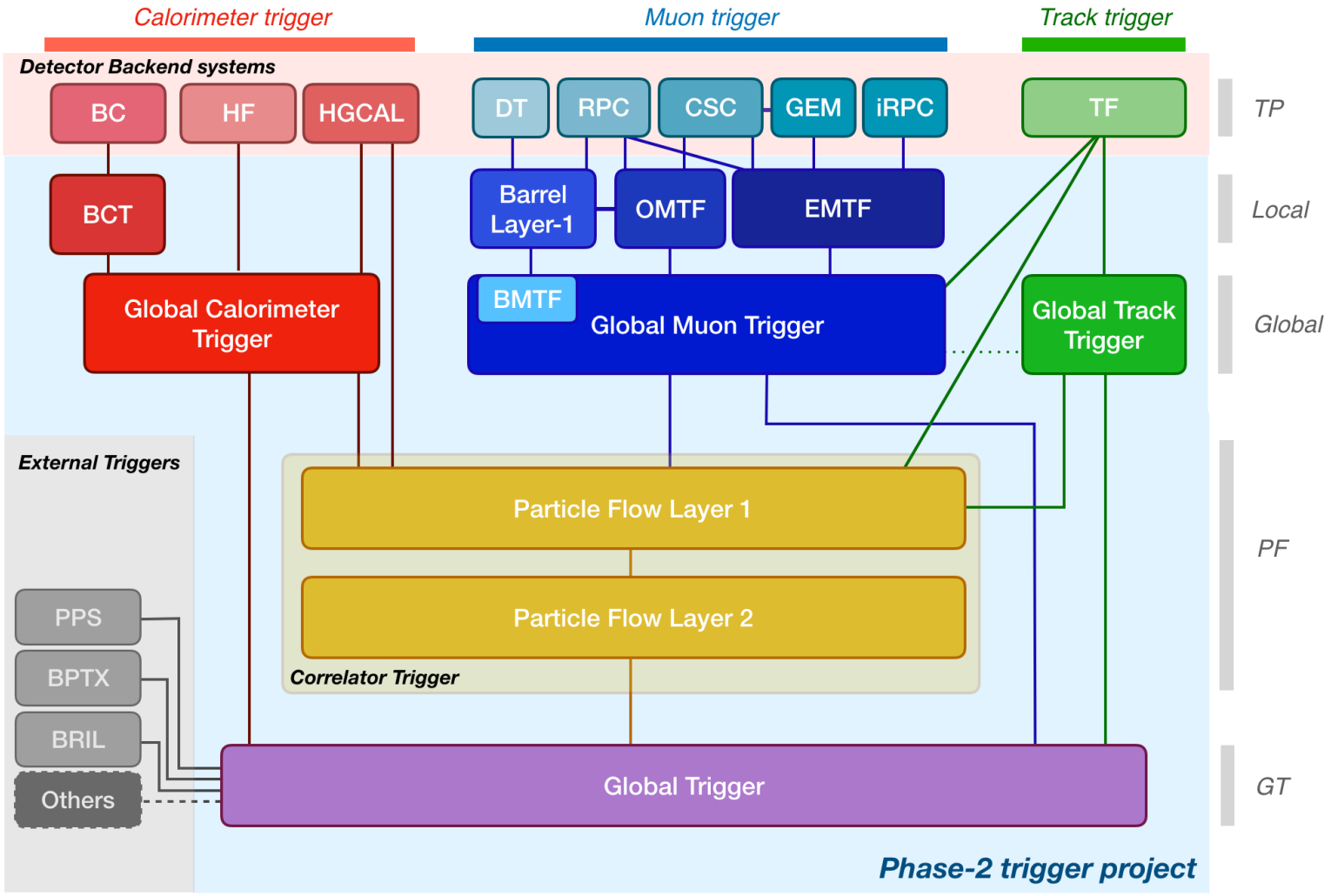


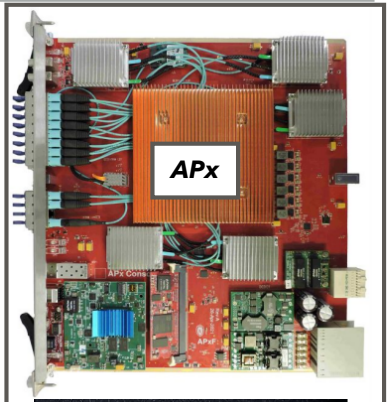
THE PHASE-2 L1 TRIGGER

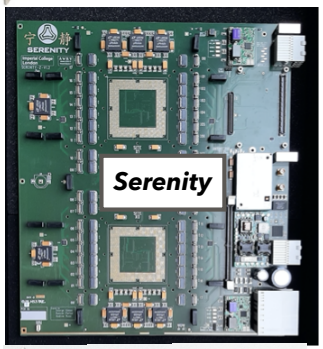
CONCEPTUAL DESIGN & HARDWARE

System architecture and instrumentation

LEVEL-1 PHASE II TRIGGER UPGRADE SYSTEM







- **Level-1 Architecture:** Efficient distribution and processing of trigger primitives, provision appropriate resources and interconnections, retain enough headroom future flexibility & Robustness
- **Level-1 technological choices**: generic processing engines (inspired from Phase-1 upgrade)
- **Key design feature:** Correlator Trigger. Collects all inputs and feed sophisticated algorithms
- **Design Constraints :** HW processors > 100 links , FPGA resources < 50 %, Latency (< 9.5 us (keep 20%) while HGCAL/TF~5us)

J. Konigsberg's talk: The upgrade of L1 muon trigger of CMS @ HL-LHC

HARDWARE PROTOTYPES

Design philosophy: Generic Processing Engines → I/O, FPGA → sophisticated algo, arch flexibility

Design evolution (since TDR): increased I/O and computing power

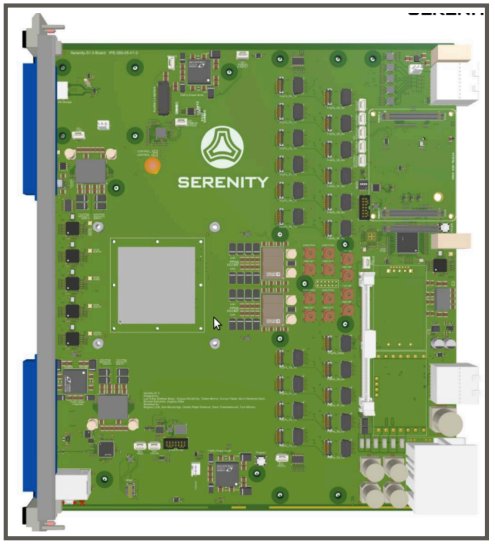
- FPGA : larger A2577 pin package, Xilinx Virtex Ultrascale VU13P
- Optics : New denser version of on-board flyover Samtec Firefly & QSFP
- Processors on board running commercial linux for flexible configuration and monitoring

APx-F:

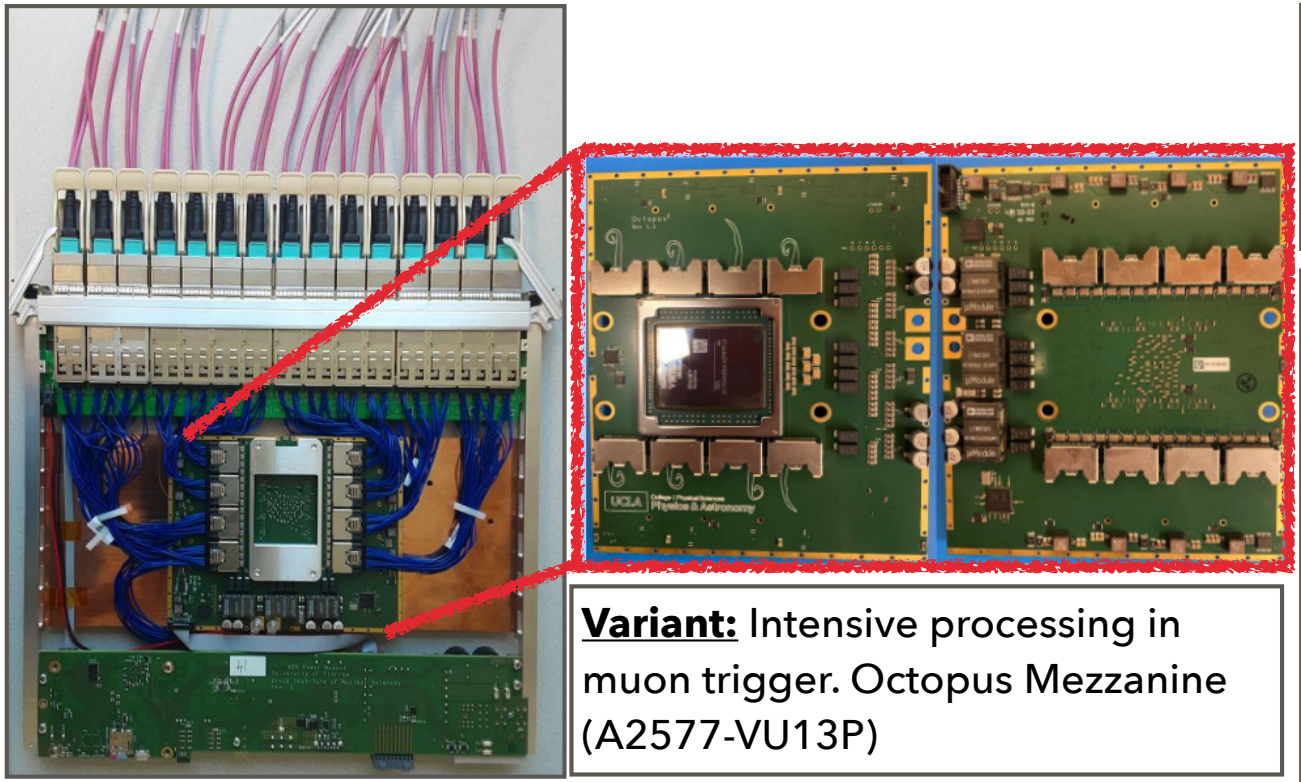
- Powered by a VU13P FPGA
- 120 bidirectional links (FireFly x12) up to 25 Gb/s
- Control, management, and monitoring by an embedded linux mezzanine (ELM) (ZYNQ SoC)
- Shelf management via custom IPMI mezzanine (OS)

Serenity:

- New halogen free design.
- 120 links with FireFly12
- Up to 144 bidirectional links (extendable to 192)
- Control & Monitoring: COM express (x86 processor)
- IPMI management through CERN IPMC

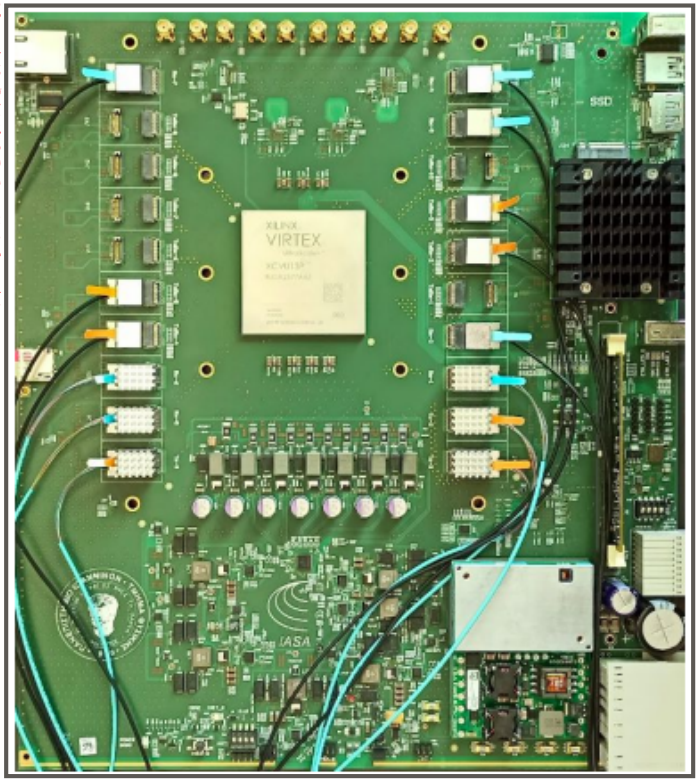


HARDWARE CAN DO MORE: EVOLUTION



BMT-L1: Barrel Muon Trigger

- Interface with FrontEnd lpGBT
- Optics: FireFly x4 25 Gb/s
- IPMC



Variant: Intensive processing in muon trigger. Octopus Mezzanine (A2577-VU13P)

X2O: Evolution from OCEAN Prototype (TDR)
Board redesigned with

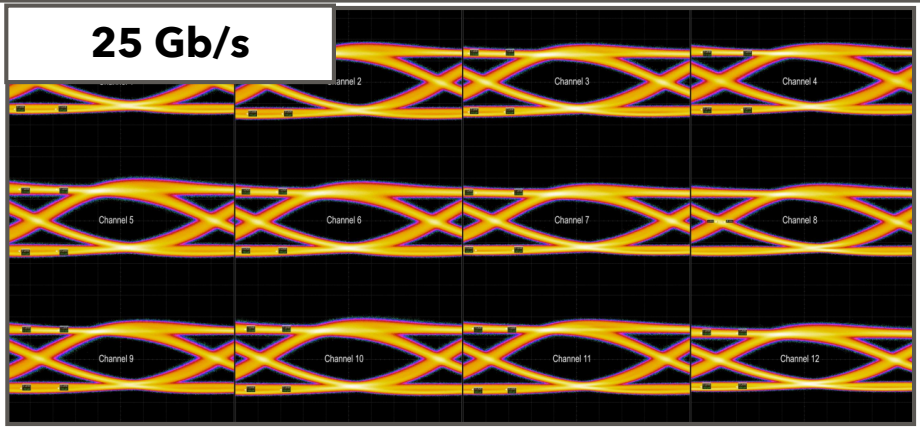
- Improved safety and interlock system with a lattice small FPGA
- New Optical Module
  - Up to 30 QSFP cages (120 links)
  - Compatible with 25G and 10G transceivers
- Power Module: Off-the-shelf Xilinx Kria, IPMC on ZYNQ
- Inter-module connections with cables

HARDWARE CAN DO MORE: OPTICS & THERMAL TESTS

Optics requirements:

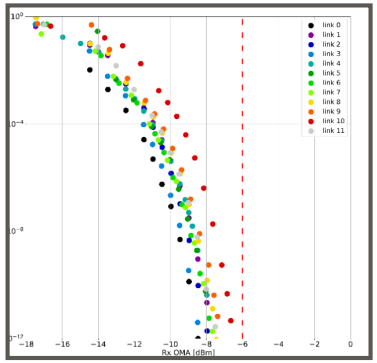
- Support sufficient signal integrity in both the electrical and optical domains by demonstrating a bit error rate (BER) much better better that 10^{-12}
- Optics should provide sufficient optical margin with a receiver sensitivity better than -6 dBm to ensure operability at end of life (as laser degrades)

25 Gb/s



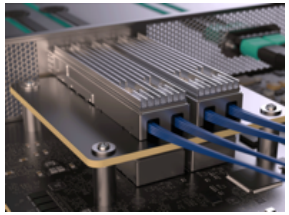
Samtec Firefly x12

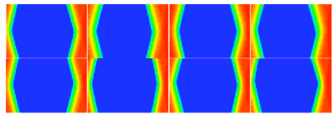
- One module: x12 RX or x12 TX
- Note Module in beta-stage
- Observing an RX sensitivity in OMA better than -6 dBm



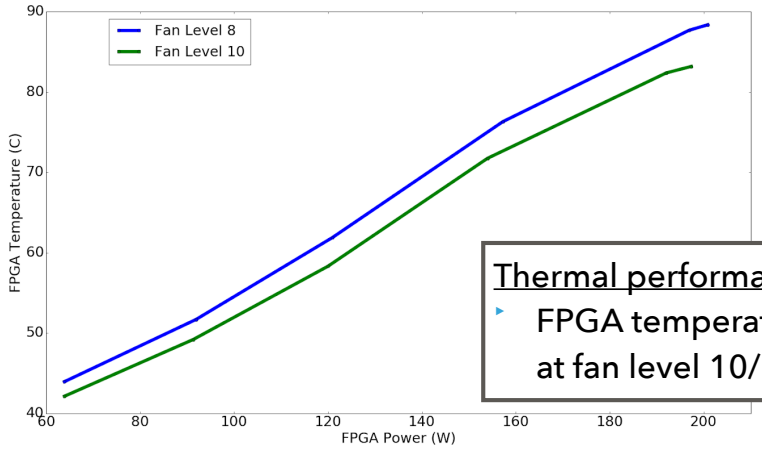
Alternatives: QSFP

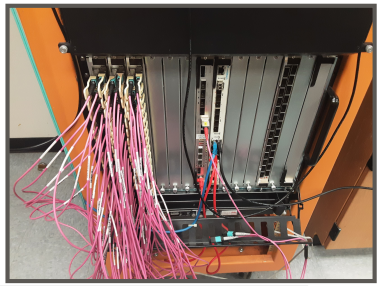
- widely used in industry
- x4 TX / x4 RX (x8 TX / x8 RX QSFP DD)
- Under qualification (BER etc)





QSFP on X2O



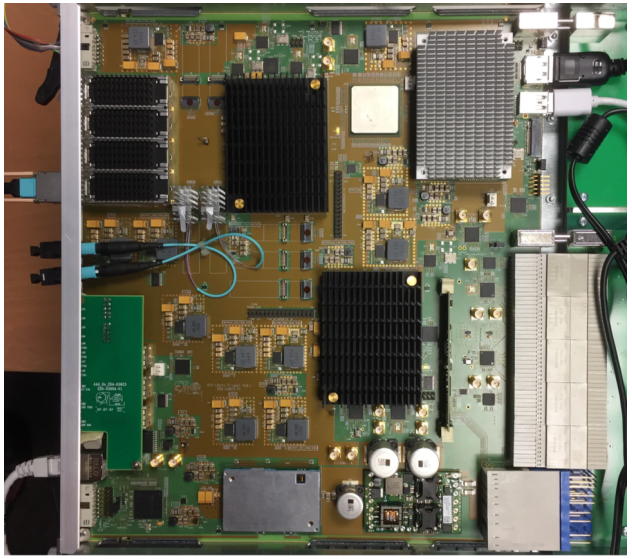


Thermal performance:

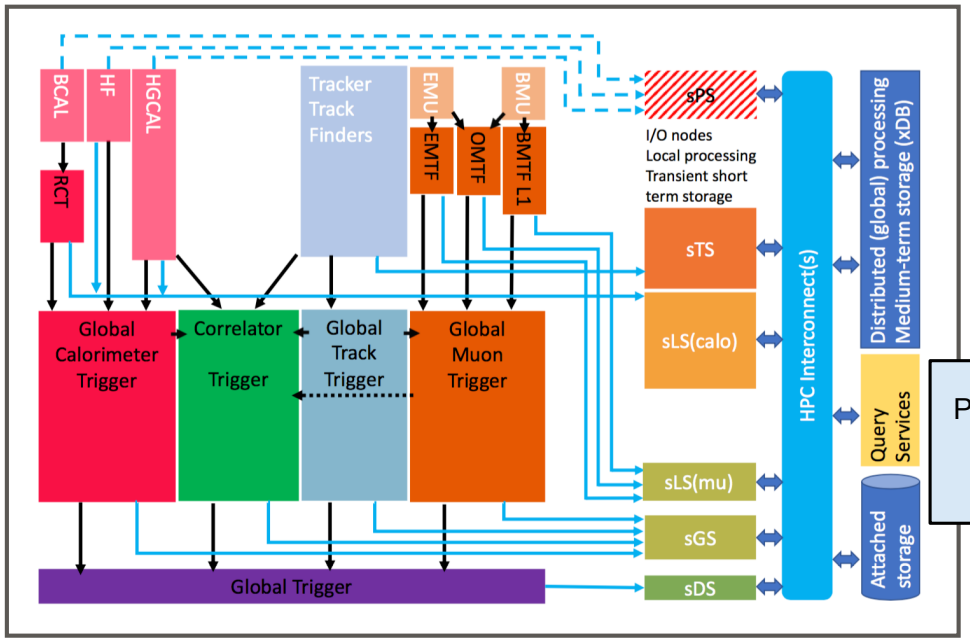
- FPGA temperature of 85C with 200W at fan level 10/15

SCOUTING @ 40MHZ: SCRUTINISING THE DATA

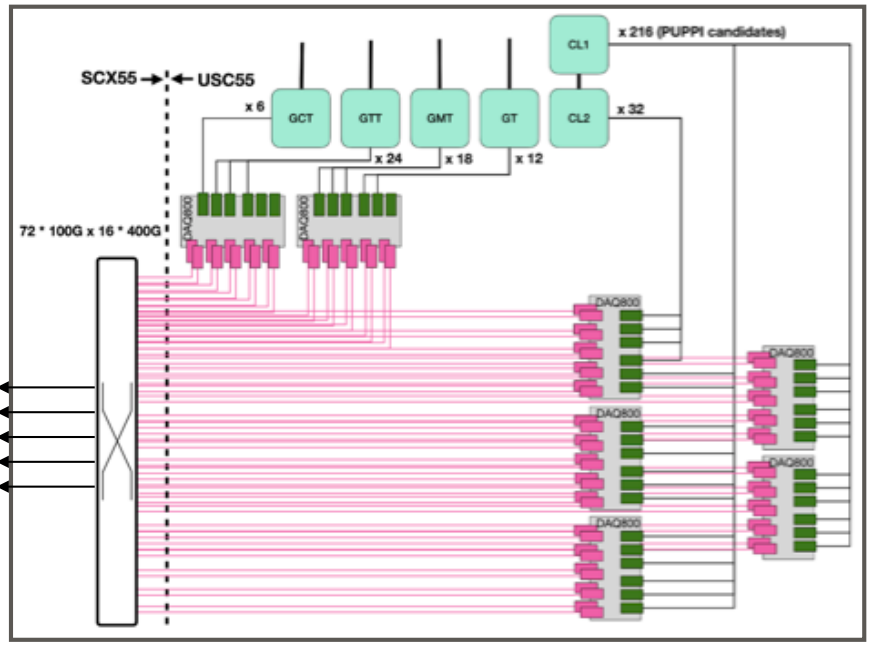
- Enables many features: real-time diagnostics (even at lower level systems), monitoring, testing new algorithms and developing menus, selecting an reconstructing physics objects w/o rate limitation.
- Analyses conducted trough queries (from storage)
- Demonstrated during LHC Run-2 with Level-1 Phase-1 muon output, now being prepared for Run-3 data taking
- Uses DTH board (DAQ800) designed for large readout detectors



DTH



Processing & storage



THE PHASE-2 L1 TRIGGER

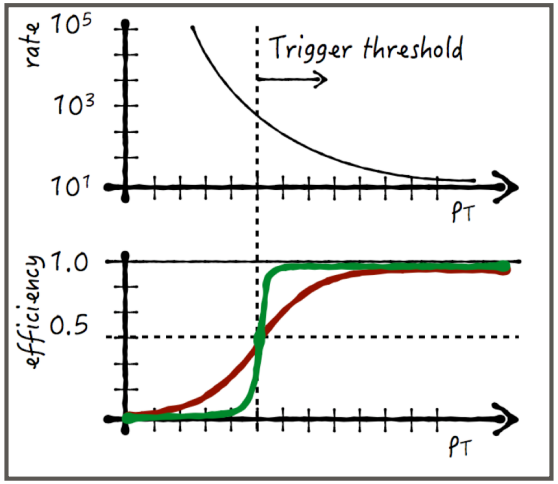
ALGORITHMS, FIRMWARE & TESTING

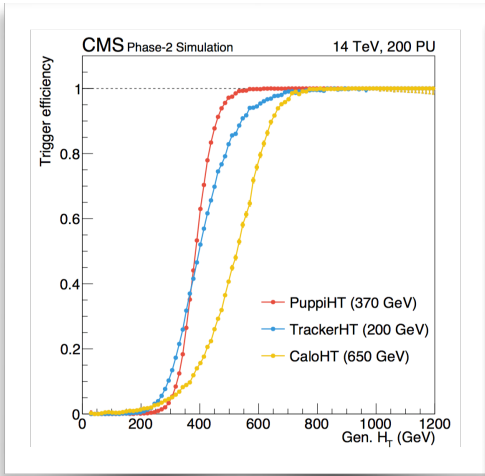
selecting physics

PHASE II LEVEL-1 TRIGGER: ALGORITHMS & MENU

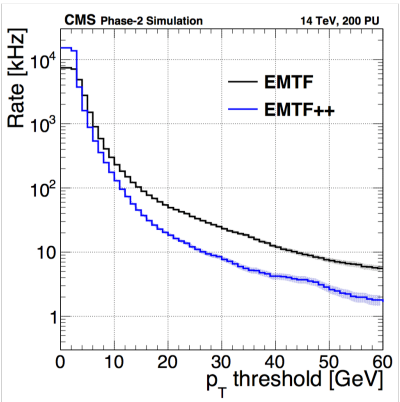
Algorithms for the Level-1 trigger:

- Extensive use of tracking to reach near offline performance (sharper efficiency turn-on curves) + reconstruction of **Primary Vertex.**
- Exploit complementarity of different object flavour:
  - **Standalone objects:** robust triggers based on independent sub-detectors
  - **Track-matched objects:** tracking used to confirm standalone Muon and Calo objects, significant improvement with simple design
  - **Particle-flow objects**: ultimate performance improvement, combine all information to match offline algorithms, require most processing time and resources for calculation

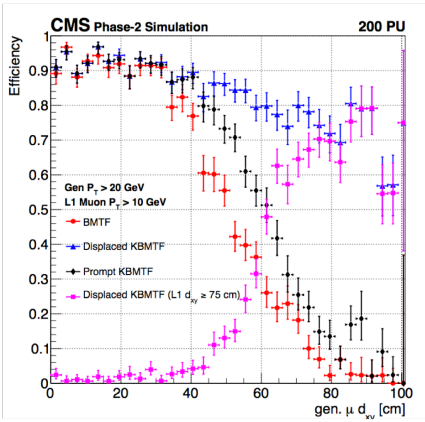




Particle-flow/puppiHT



Standalone forward Muon reconstruction Endcap



Displaced Muon trigger Barrel (Kalman Filter) → *Run-3*

Level-1 Menu:

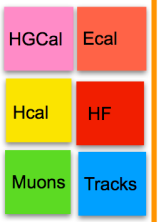
- Simplified: Phase-1 physics built from Run-2 L1 Menu (346 kHz)
- Extended: new triggering strategy to expand physics reach (+110 kHz)

GLOBAL EVENT RECONSTRUCTION @ LEVEL-1

- Availability of tracks & high-granularity calos
- Implement global event reco @ L1 (like PF)
- Additionally it makes sense to mitigate pileup
- *Challenge : can we run full PF+PUPPI within the hardware of the L1 trigger?*

PF takes in everything

Assemble All detectors

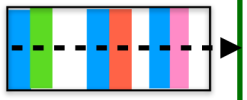


PF is local

Assemble Things in local regions η x φ

PF Links

Particle flow combines everything together to Particls

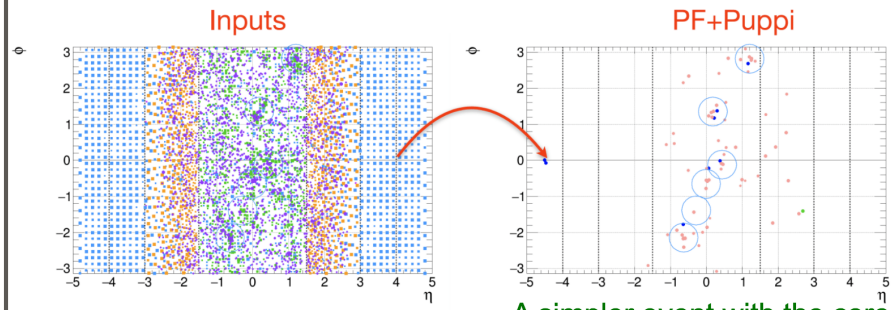


Can we run a local PU Algo?

PUPPI is local
Can parallelize it by region

Also its the CMS default PU algo

- What are the advantages of particle flow?

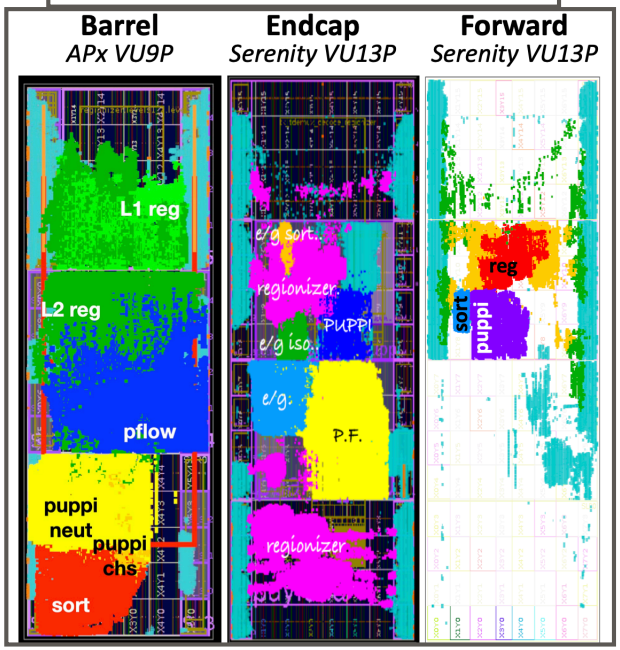


A simpler event with the core physics preserved

- Better resolution
- Ease of use → build particle level algorithms
- Reduction in bandwidth and reduction of resources

- **Demonstrated a working PF+PUPPI algorithm**
- PF+PUPPI hugely reduces the event complexity
- Allows for a lot of flexibility in downstream design
- L1 Algorithms looks like offline reconstruction
- PF+PUPPI developed with Vivado HLS (a lot of written by physicists along with engineers)

Hardware demonstrator

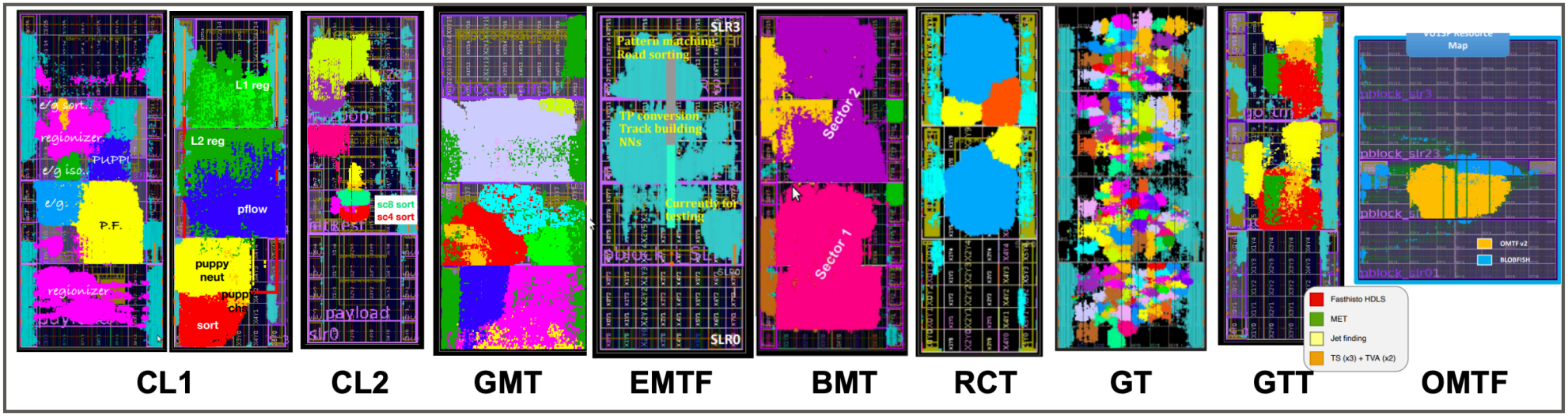


CMS Collaboration. Particle Flow CMS *JINST* **12** (2017) P10003, arXiv:1706.04965.
D. Bertolini, P. Harris, M. Low, and N. Tran, PUPPI, *JHEP* **10** (2014) 059, arXiv:1407.6013.

ALGORITHM INTO FIRMWARE

Firmware design:

- Algorithm developed mostly in C → High Level Synthesis (HLS). Using Vivado HLS, Vitis HLS
- Many tools available for Machine Learning inference: hls4ml, Conifer for BDT evaluation
- New fixed point arithmetic in C++ [taken from Xilinx libraries] → emulator firmware
- Continuous integration of the firmware in repository



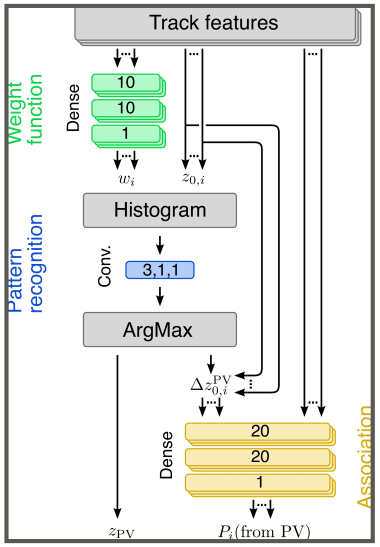
Firmware integration:

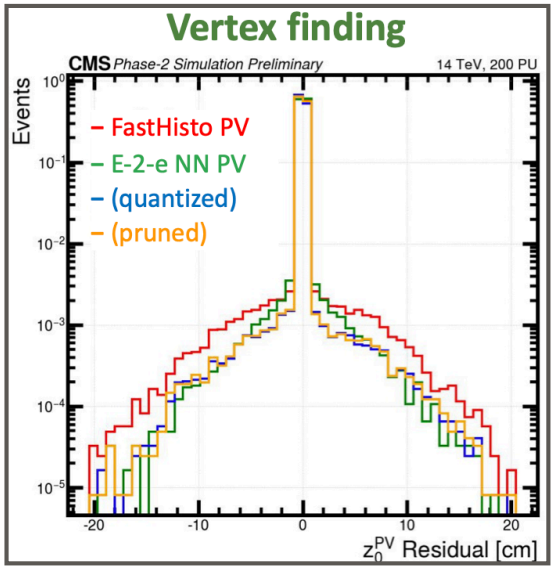
- All algo & manage I/O
- Verify timing, resources utilisation & latency: all using less than 50% resources, whole system evaluated to 8.6us (well within 9.5us)
- 100% correspondance emulator - firmware
- **Common framework wrapper** → firmware implementation board agonistic

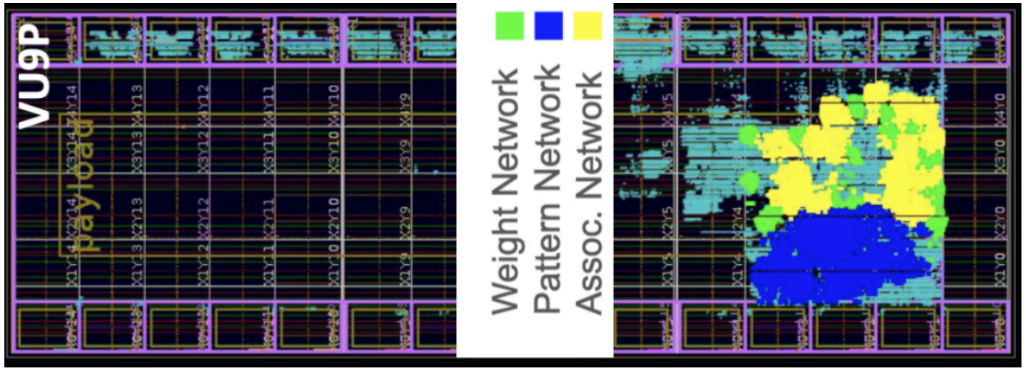
RECENT DEVELOPMENTS HIGHLIGHTS

NN Vertex Finding:

- Combinaison of dense BDTs and CNN to perform Vertex Finding and Track-to-Vertex association
- Firmware quantised and pruned to fit within FPGA
- ***Improved performance wrt to baseline (reduction in the tails of the residual by 50%***

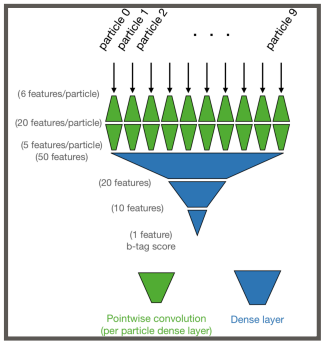


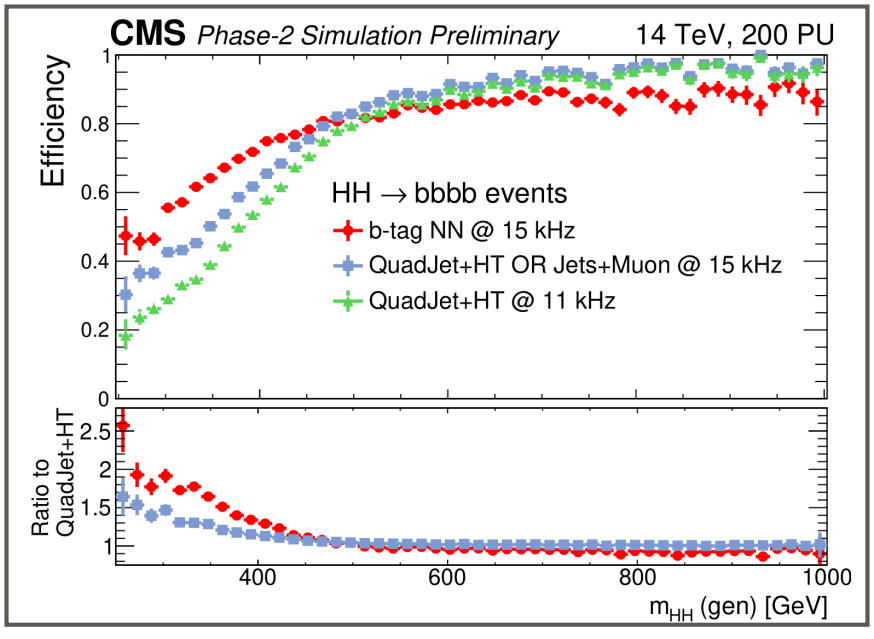




b-tagging:

- Training NN to ID jets from b-quarks
- Runs on PUPPI particles within each jet and discriminate between b-quark jets and those from light quarks and gluons
- ***Better performance compared to QuadJet+HT for M(HH) < 500 GeV (or Jets+Muon triggers)***

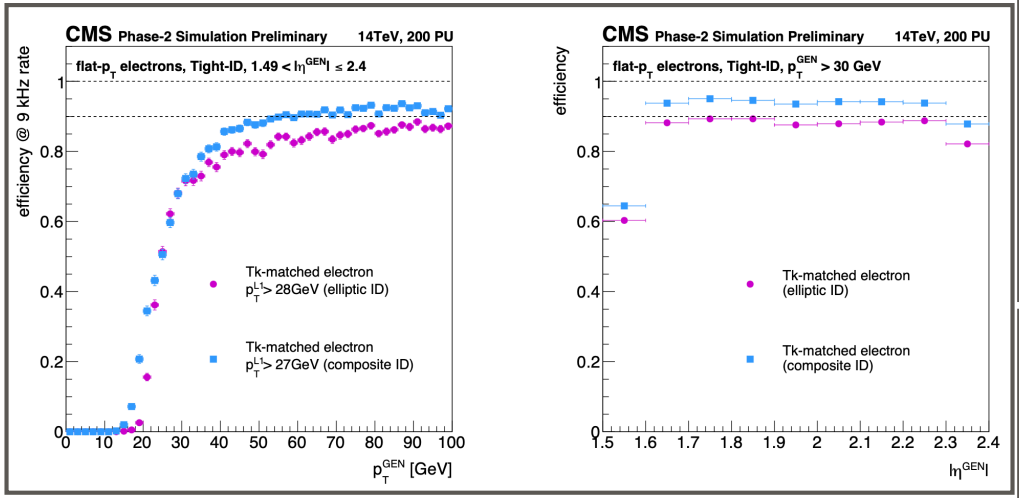


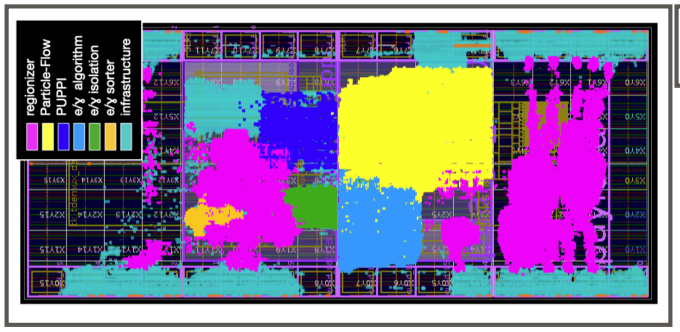


RECENT DEVELOPMENTS HIGHLIGHTS

Electron-ID:

- New Composite-ID, combines information about tracks and clusters in the HGCAL into a single model for matching and identification
- A single BDT model: controlling the identification of track and calorimeter deposit and the tightness of the matching.
- 10% more efficiency for the same rate

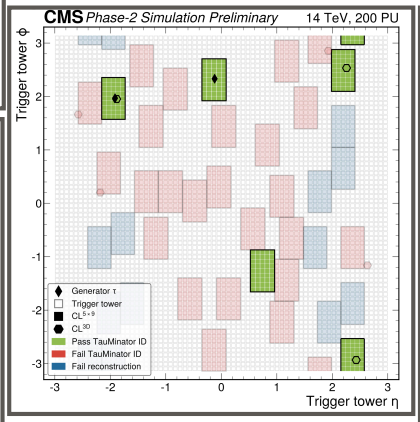


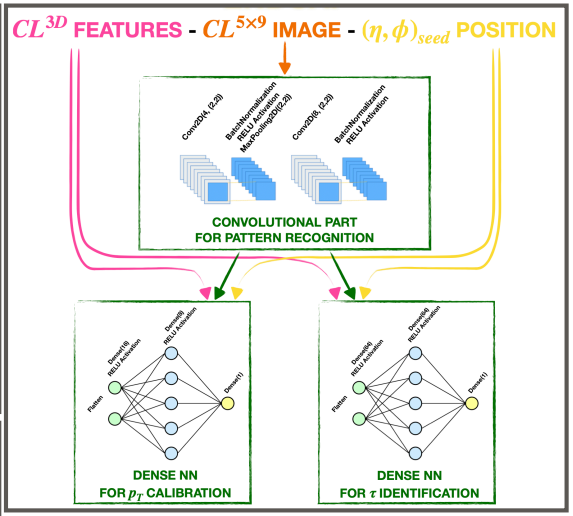


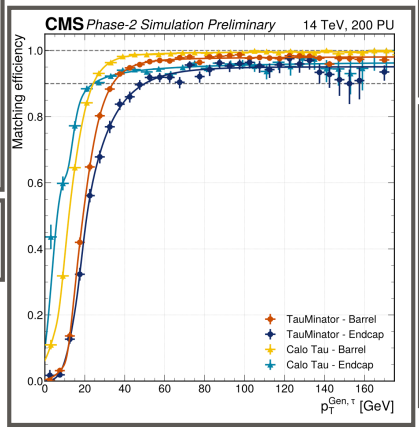
	LUT	FF	BRAM	DSP
e/γ IP	3.1%	0.4%	0.0%	1.6%
Total	24.4%	17.6%	29.5%	14.3%

Tau reconstruction: Tauminator

- Training dedicated CNN to reconstruct and identify Tau-induced signal in calorimeters (5x9)
- Elegant way to deal with different geometries in Barrel (Crystals) and EndCap (HGCAL 3D clusters).





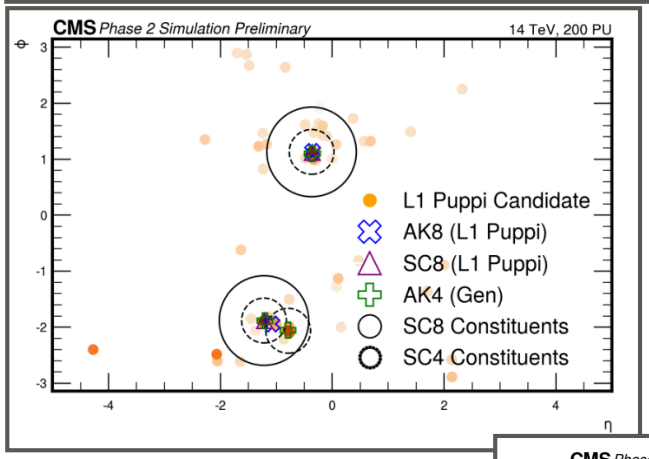


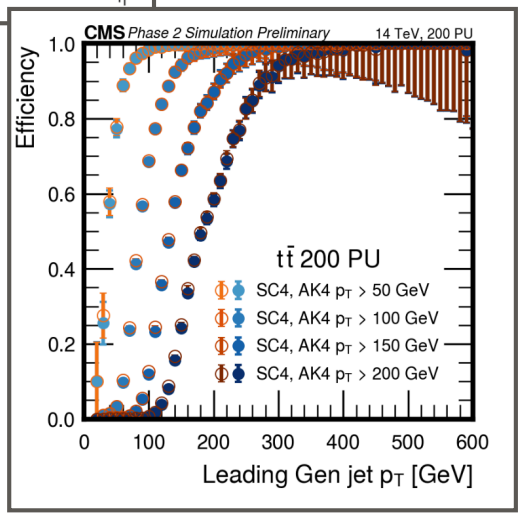
- Much improved efficiency with respect to CaloTaus
- 21% rate reduction on DoubleTau with 90GeV threshold

RECENT DEVELOPMENTS HIGHLIGHTS

SeededConeJets:

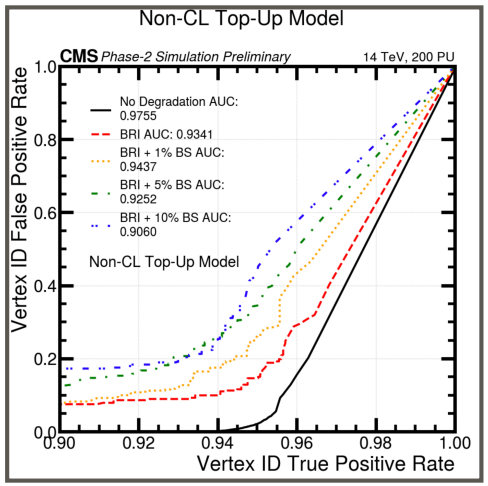
- Jet finding based on PF candidates
- Iterative approach computing distance between each particle and jet radius (SC4 or 8), compute jet axis and energy.
- Jet matching anti-kt jets

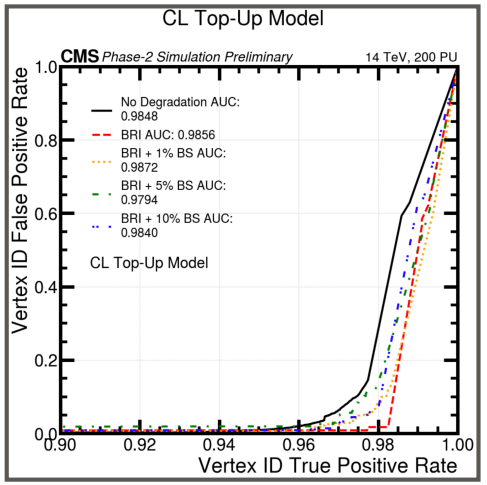




Continual learning:

- Elegant way to deal with changing detector conditions (ageing, noise, LHC interfill, etc.)
- Train a model with a continuous stream of data. Learns from a sequence of partial experiences rather than all the data at once.
- Update model to changing conditions without large MC production.
- Method tested on Vtx reconstruction



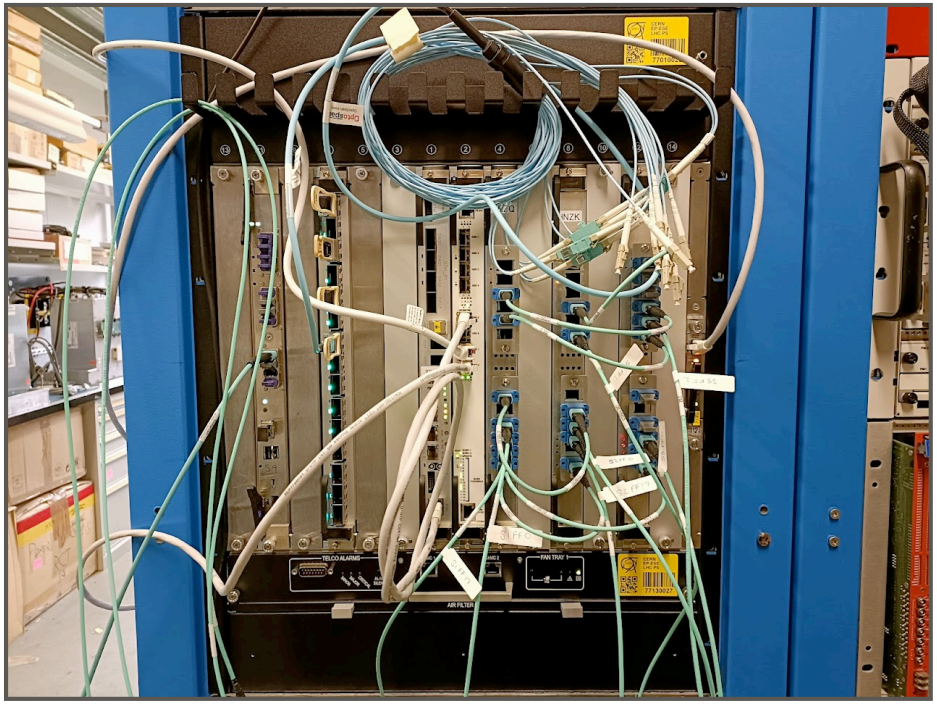


Mention some algorithm for run 2 tested in Run-3

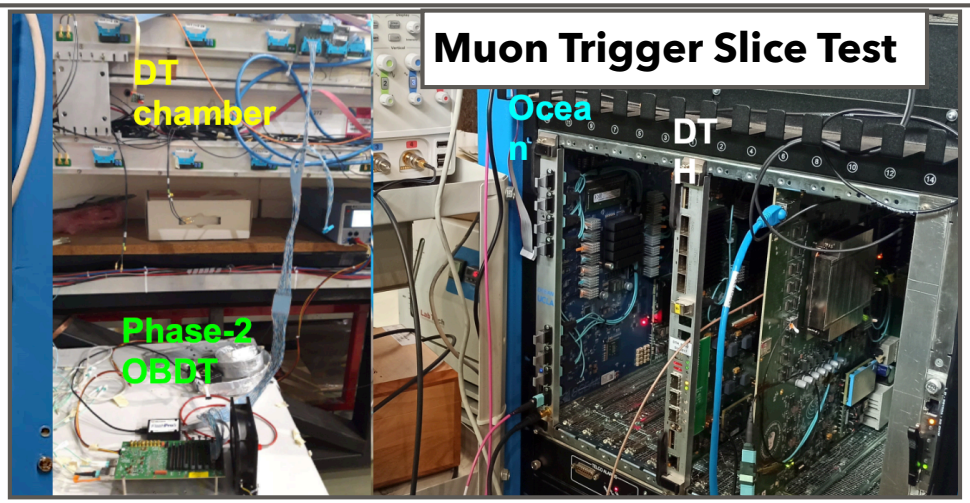
TESTING AND SYSTEM DEMONSTRATION

Phase-2 Level-1 Trigger system demonstration

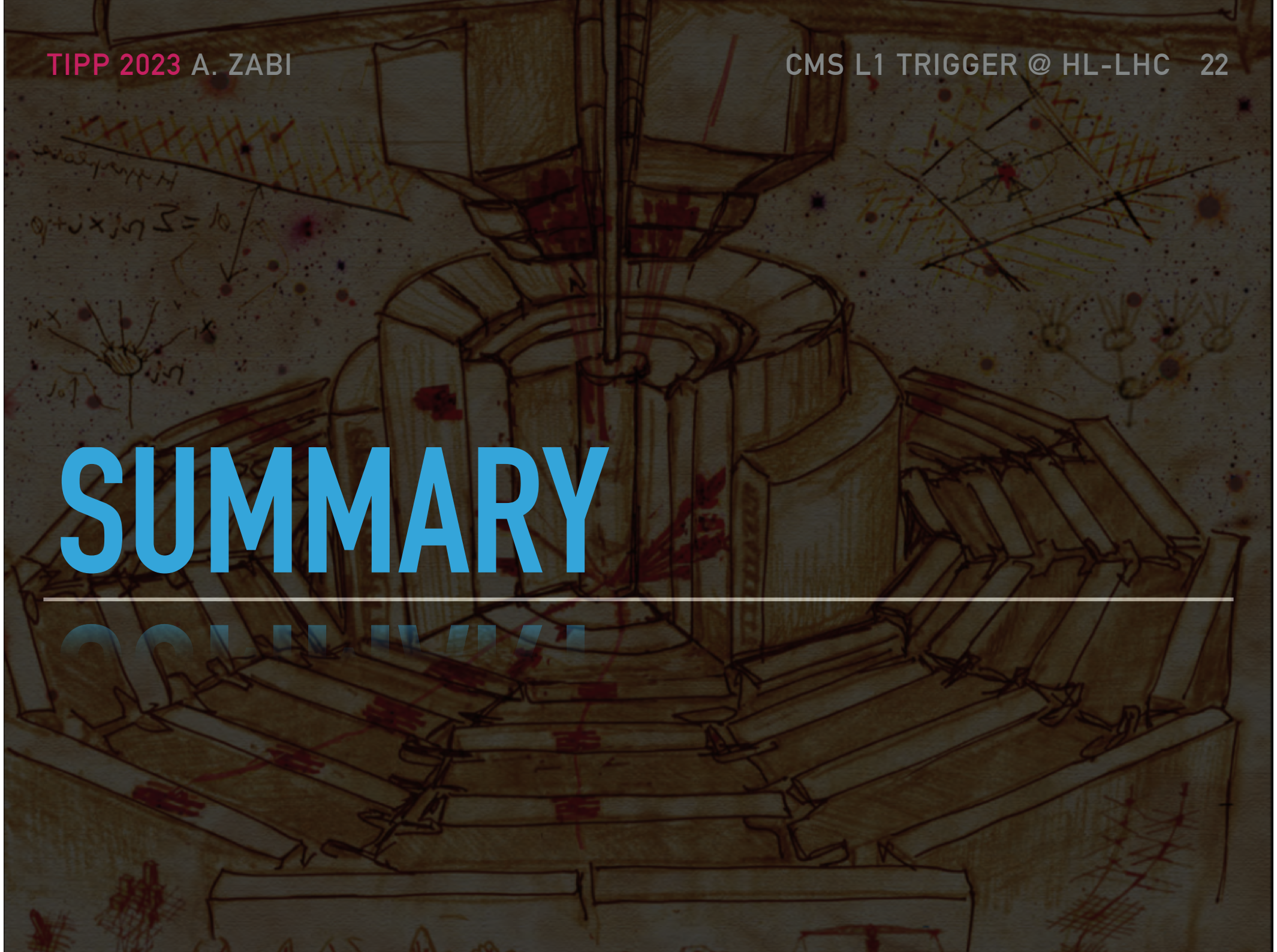
- Single-board and multiple board tests performed
- Integration centers across the globe: larger scale integration @ CERN (904). Multiple flavour board tests.
- Slice test in Muon Barrel Trigger during Run-3. Installation @P5: DT–>BMT–>GMT–>GT
- **Board interconnection: protocol**
  - Links (asynchronous) operation @ 25.78 Gb/s
  - L1 Trigger boards sending packets only once (no retransmission) → error proof
  - Protocols (64/66b or 64/67b) encoding achieved low error rate, validated recovery mechanism etc.



Building 904 @ CERN



Muon Trigger Slice Test



SUMMARY

CMS PHASE II L1 TRIGGER UPGRADE

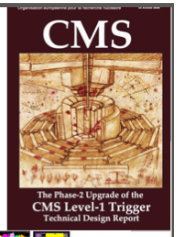
- CMS proposing solid solutions to triggering and data acquisition challenge @ HL-LHC
- Phase-2 Level-1 Trigger Upgrade project: project approved in 2020 (https://cds.cern.ch/record/2714892?ln=en), steady progress with construction
- Level-1 Hardware trigger with enhanced capabilities complying with physics requirements. Sophisticated algorithms (particle-flow) are prototyped in FPGAs and exploit target hardware (VU13P/25Gb/s links)
- Modular and flexible architecture
- Hardware development lines pursuing 4 flavours of ATCA boards meeting the requirements of the project.
- Hardware demonstration ongoing and planned for testing with live data during LHC Run-3

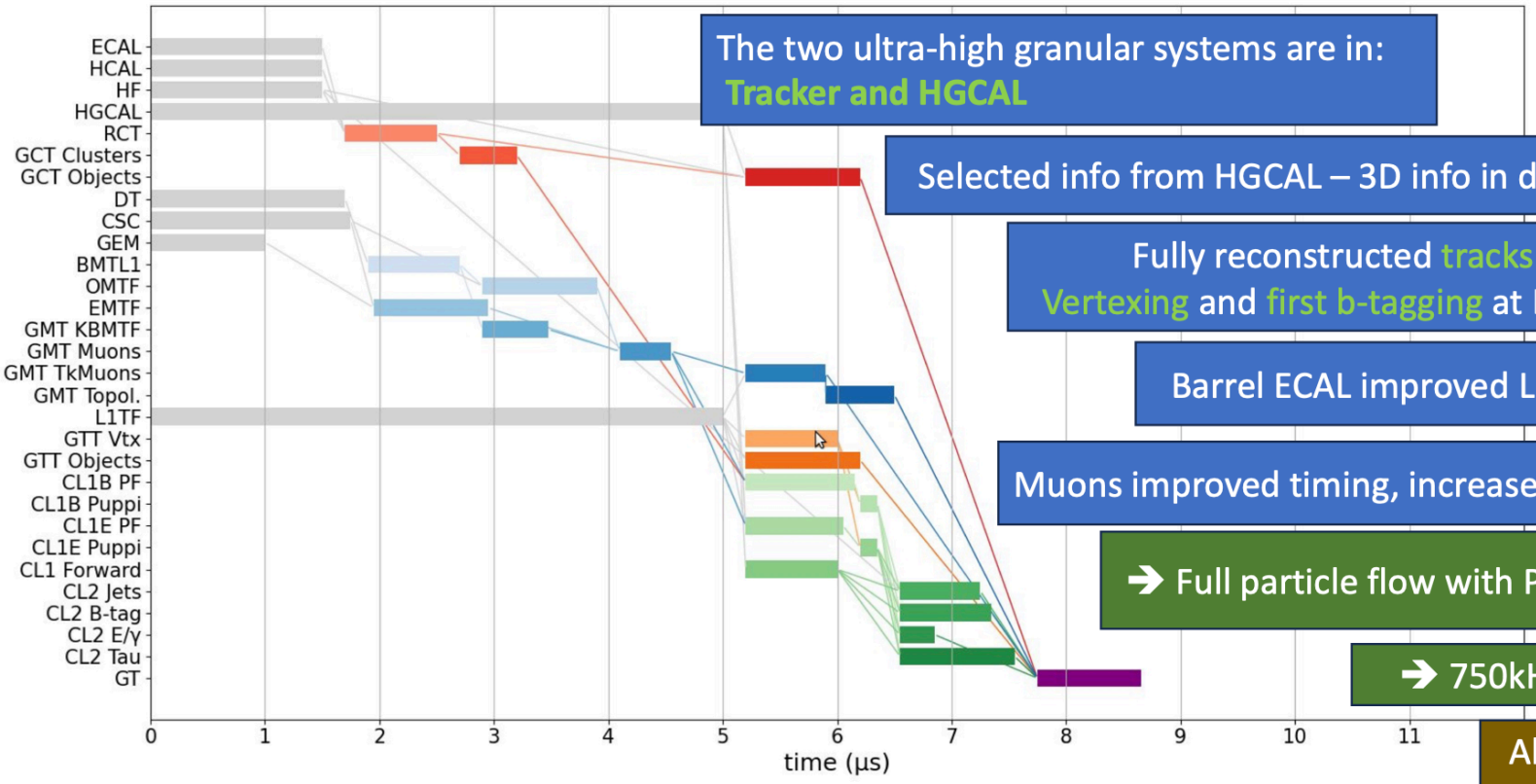
BACK UP

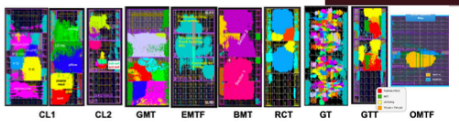
REFERENCES

- **Vertex:**
  - https://cds.cern.ch/record/2792619?ln=en
  - https://cds.cern.ch/record/2814727?ln=en
- **B-Tagging**
  - https://cds.cern.ch/record/2814728?ln=en
- **Continual Learning**
  - https://cds.cern.ch/record/2859651?ln=en
- **Seeded Cone Jet**
  - https://cds.cern.ch/record/2859652?ln=en
- **TauMinator**
  - https://cds.cern.ch/record/2868783?ln=en

Globally Incorporating **Level-1 Trigger** Aspects for Achieving **Equal or Lower PT** Thresholds in **HL-LHC** Compared to Run 3 in initial TDR designs







The two ultra-high granular systems are in:
Tracker and HGCAL

Selected info from HGCAL – 3D info in dedicated system stream

Fully reconstructed tracks above 2 GeV
Vertexing and first b-tagging at L1 – σ_z about 1mm

Barrel ECAL improved L1 granularity: factor 25

Muons improved timing, increase redundancy and eta coverage

➔ Full particle flow with PU mitigation

➔ 750kHz to High Level Trigger

All Phase II systems compatible with 12.5 µs latency
(3.5 µs today)

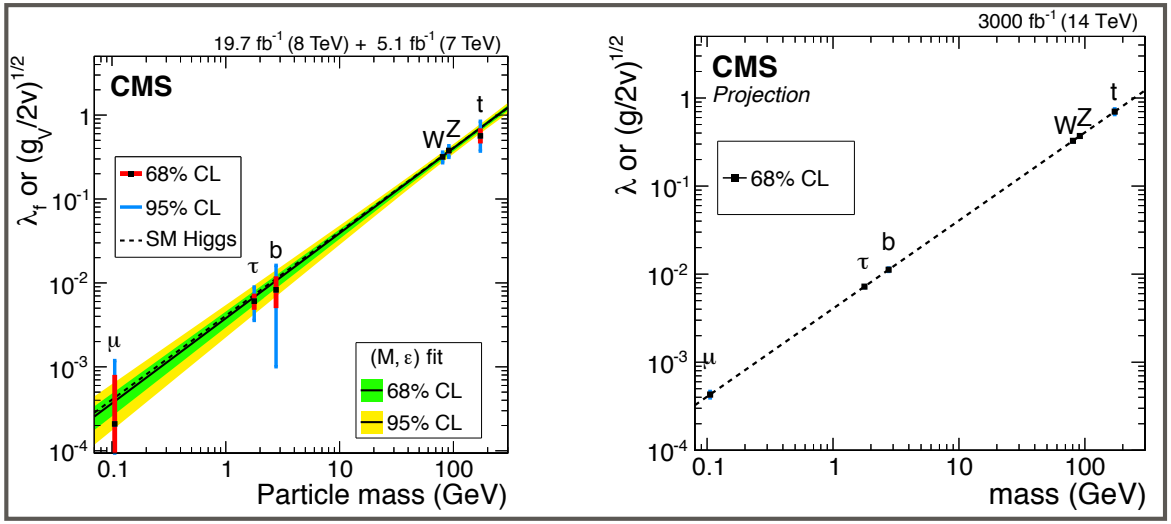
Level-1 Trigger latency – preliminary, based on algos in **firmware in test systems**

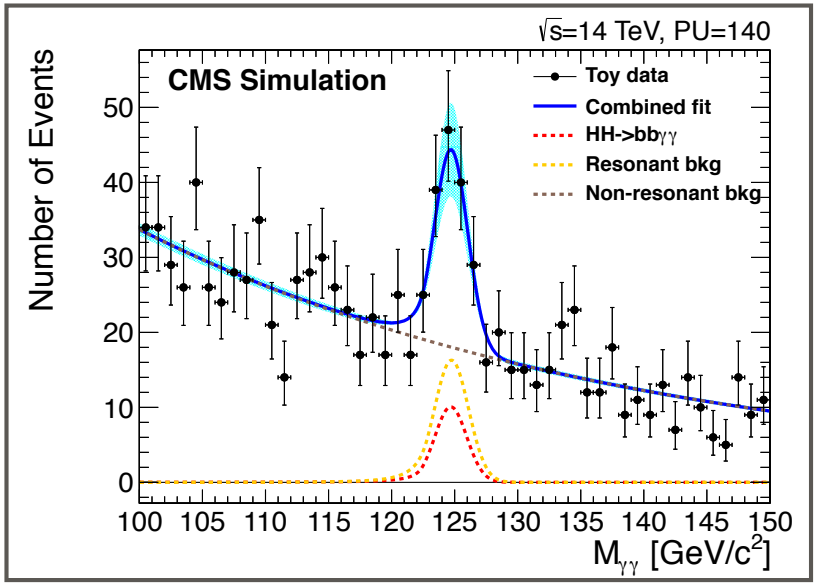
More info, comprehensive presentation at TIPP,
System Design and Prototyping for the CMS Level-1 Trigger at the High-Luminosity LHC, Alexandre Zabi
The Upgrade of the Level-1 Muon Trigger at the CMS experiment for the High-Luminosity LHC era, Prof. Jacobo Konigsberg

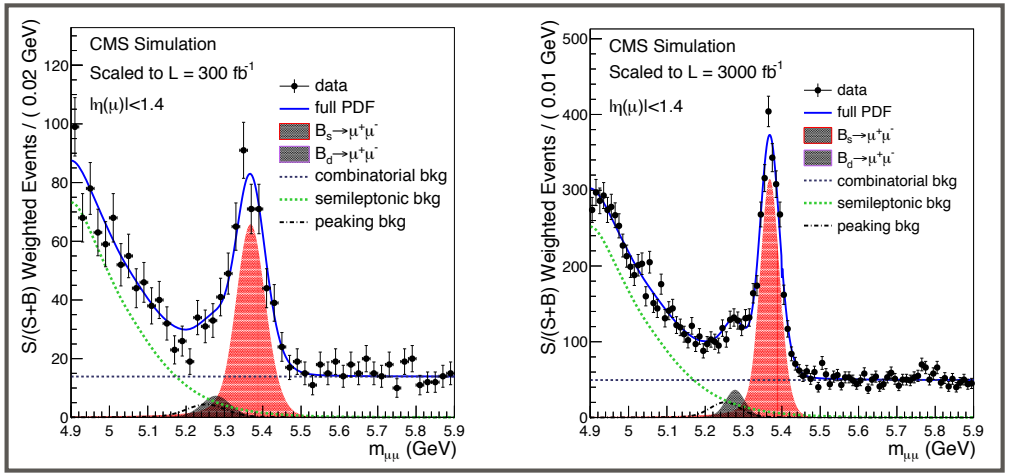
PHYSICS @ HL-LHC

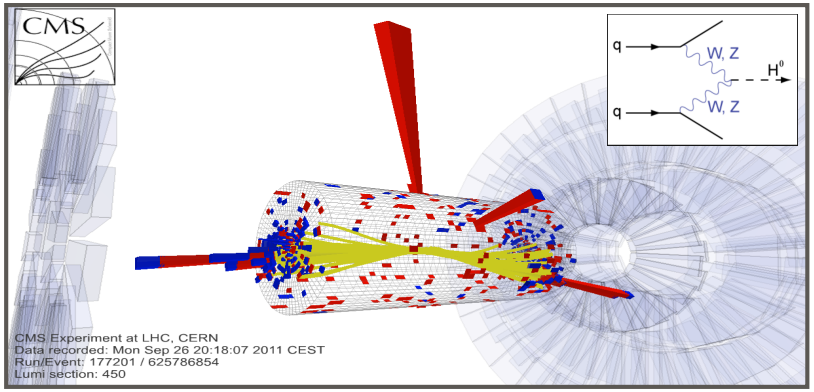
CMS Phase-2 physics drivers

- **Exploring the unknown** : Searches for new physics beyond the Standard Model (SM) DM, LLP,etc.
- **Standard Model as tool for discovery** : Precise knowledge of SM processes, probe anomalous couplings, 4 tops, VBS, VBF, etc. Higgs Sector: couplings (Hcc, Hμμ), differential xc, self-coupling HH
- **Understanding the Standard Model**: parton shower, underlying event, differential measurements







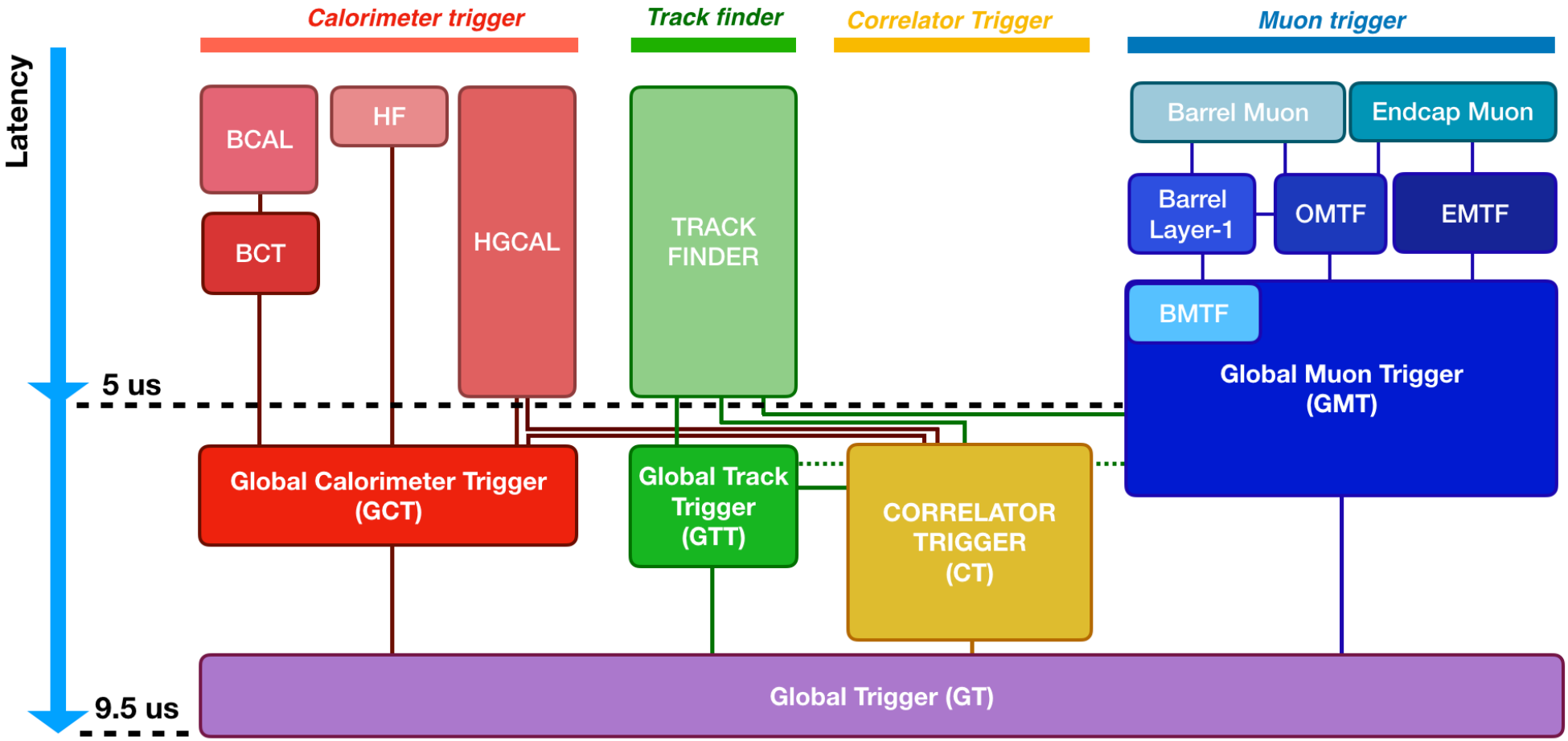


LEVEL-1 PHASE II TRIGGER UPGRADE SYSTEM

Phase-2 L1 trigger: latency

Latency budget = 9.5 us (20% margin to get to 12.5 us)

- **5 us** on region processing
- **4.5 us** on producing triggerable objects (including correlations) & final decision

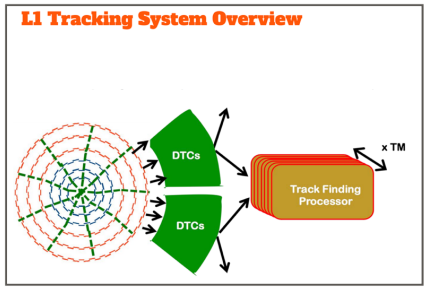


PHASE II TRIGGER UPGRADE INTERFACES

TRACK FINDER INPUT

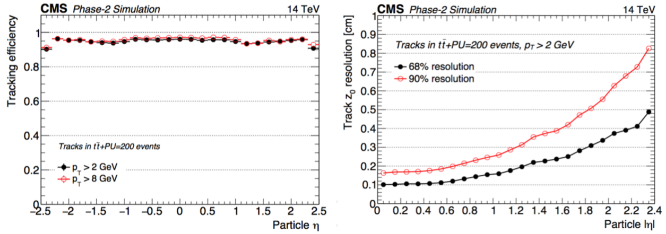
MAIN FEATURES: **Outer Tracker**

- Trigger primitives |η|<2.4 & 9 phi sectors
- TMUX = 18
- Track finding algorithm: hybrid (fully reco tracks)
- Upper limit of 110 Tracks/sector (+40% extended tracking for displaced tracks)
- **L1 Track word = 96 bits**
- OUTPUT: 3 exact copies Correlator Trigger, GTT and GMT
- Latency = 5us



Track parameter	Number of bits
q/R	15
ϕ	12
tan(λ)	16
z_0	12
d_0	13
χ^2/dof	4
bend-χ^2	3
hit mask	7
track quality MVA	3
other quality MVAs	6
spare	5
total	96

Table 2.1: Content of the L1 Track word.



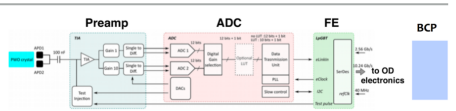
Excellent tracking efficiency

BARREL CALORIMETER INPUT

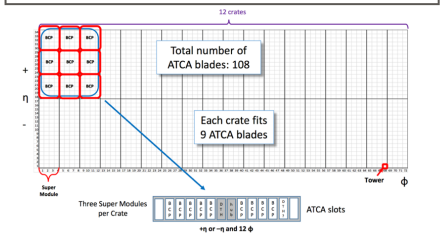
MAIN FEATURES: **Barrel Calorimeter**

- Provide ECAL crystal level information (optimal matching with tracks)
- HCAL allows to access depth info (pile-up removal in jets under study)
- TMUX = 1
- *Objects and format:*
  - *ECAL Crystals = 16 bits*
  - *ECAL Clusters (3x5) = 40 bits*
  - *HCAL Towers = 16 bits*
  - *HF Towers = 10 bits*
- *OUPUTS: GCT → Correlator Layer-1*
- *Latency = 1.5us (ECAL) & (HCAL)*

Both system provide timing information ECAL ~ 30 ps pT>50 GeV, HCAL~0.5 ns pT>50 GeV



Moving Trigger Primitive logic in back end : BCP



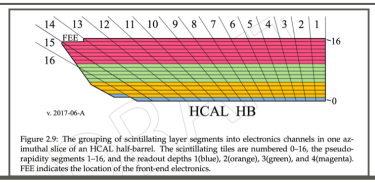
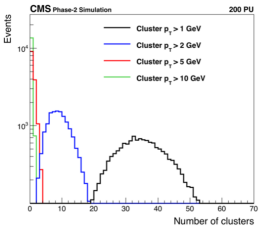


Figure 2.9: The grouping of scintillating layer segments into electronics channels in one azimuthal slice of an HCAL half-barrel. The scintillating tiles are numbered 0–16, the pseudorapidity segments 1–16, and the readout depths 1(blue), 2(orange), 3(green), and 4(magenta). FEE indicates the location of the front-end electronics.

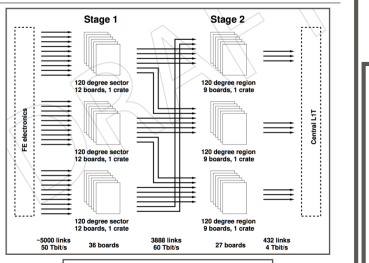


ENDCAP CALORIMETER INPUT

MAIN FEATURES: **HGCAL**

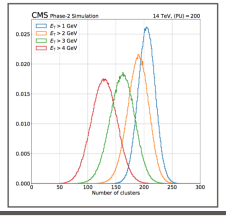
- High granularity calorimeter (50 Layers)
- TP Backend system to build 3D-Clusters & shower shapes.
- TMUX = 18
- Objects and format:
  - 3D Clusters = 128 - 416 bits
  - Towers = 16 bits
- OUTPUT: 2 exact copies to Correlator Trigger Layer-1 & GCT.
- Latency = 5 us

No timing information available.



Data type	Content	Minimal size / bx (bits)	Maximum size
Header	Total energy, BX, $N_{clusters}$	32 × 6	-
Cluster	Position	32	-
	Energies	32	-
	Shape variables	64	352
Total clusters		128 ×(≈ 900 clusters)	416 ×(≈ 300 clusters)
Tower	Energy	12	-
	EM fraction	4	-
Total 2600 towers		43 k	-

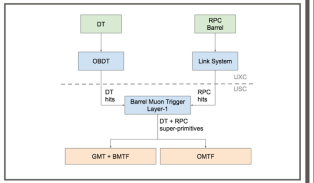
Table 2.4: Data sent to the central L1T



MUON BARREL INPUT

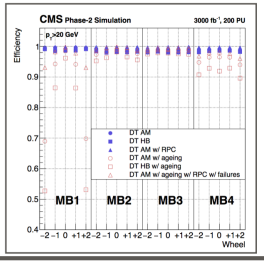
MAIN FEATURES: **DT&RPC**

- **DT:** new electronics, including TDC w/ ~2ns resolution (better BX ID, spatial resolution, fake rejection)
- **DT TP Algorithms :** Majority Mean-Timer and Analytical Method both exploiting fine detector information (DT cells & correlation among superlayers)
- **RPC :** new readout w/ timing (1/16 BX granularity = 1.5 ns) + faster links
- **DT+RPC Super Primitives:** combines RPC clusters (timing) and DT TP (position)
  → better performance (robust against ageing)
- TMUX = 1
- Objects and format
  - DT+RPC = 64 bits
  - Expecting 28 segments (long + transverse)
- OUTPUT: GMT(BMTF) & OMTF
- Latency = 2-3 us



Muon Barrel Super primitives

Data field	Position	Bending angle	BX in-orbit	Sub-BX time	Chi2	Quality	Superlayer	RPC info
Bits	17	12	12	5	4	4	2	8



MUON ENDCAP INPUT

MAIN FEATURES: **CSC/RPC/iRPC/GEM**

- **CSC:** new electronics, finer granularity of TP (improved bend direction and angle resolution)
- **RPC :** same as barrel upgrade
- **iRPC :** 1.1 ns time resolution
- **GEM/ME0:** precise measurement of muon bending angle (better reach and rate control)
- **CSC-GEM** super primitives can improve bend direction resolution (under study). Could also CSC + (i)RPC
- TMUX = 1
- Objects and format
  - CSC segment = 32 bits
  - RPC Clusters = 15 bits
  - iRPC Clusters = 41 bits
  - GEM Clusters = 14 bits
  - GEM ME0 segment = 24 bits
- OUTPUT: OMTF & BMTF
- Latency = 1 us - 1.75 us (CSC)

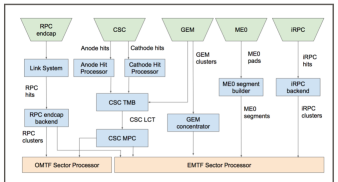
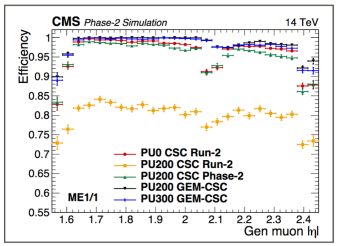


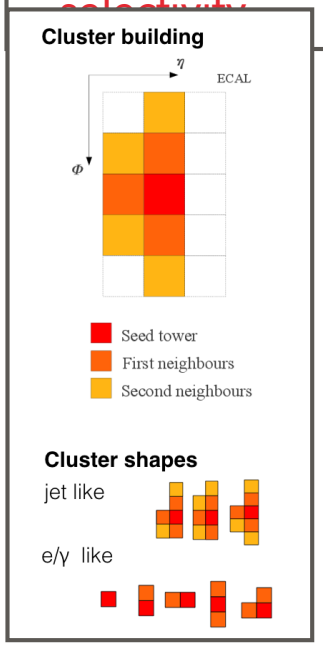
Figure 2.17: Muon endcap trigger primitive architecture.



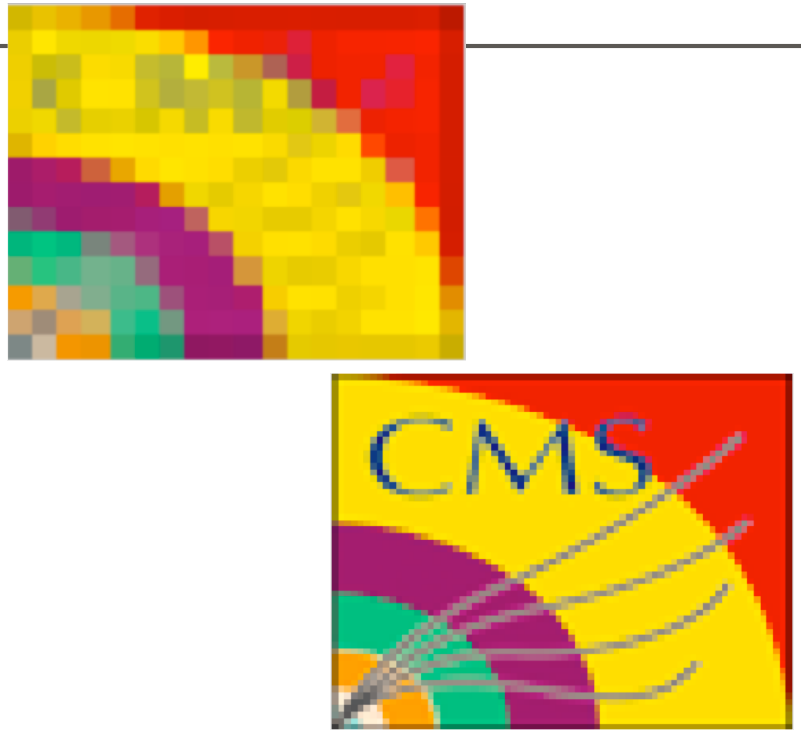
TECHNOLOGICAL CHOICES

Phase-2 L1 Trigger Design: Key technological features (inspired from the L1 Phase-1 upgrade)

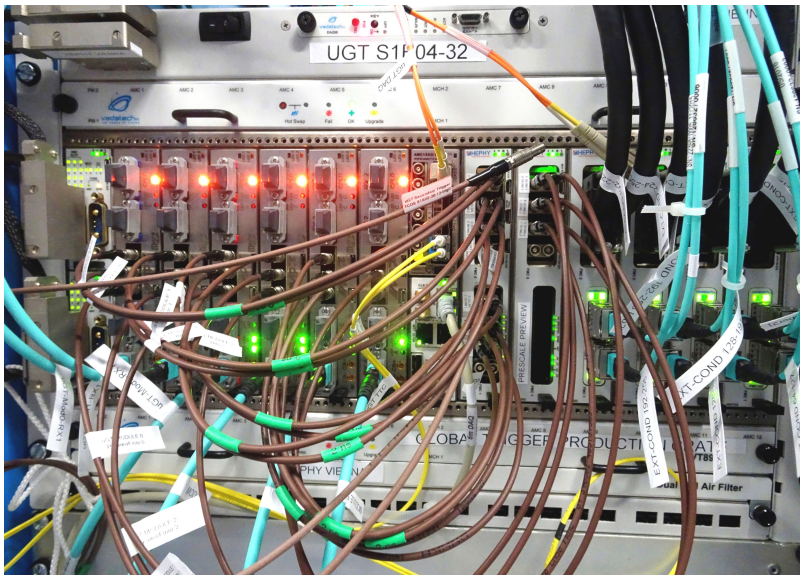
- **FPGA:** The extensive use of state-of-the-art FPGAs → optimised reconstruction, identification, isolation and energy calibration of trigger objects using high-granularity detector information.
- **High-speed optical links:** facilitate the aggregation of data from across the entire detector → A complete view of the detector (evaluation of global quantities MET, pileup, specific VBF)
- **Flexible and modular architecture:** Reconfigured to adapt to HL-LHC running conditions and physics needs. Extra resources → Compute sophisticated quantities → richer menu and increased selectivity



Phase-1 EG algo



Phase-1 Upgrade: increased calorimeter granularity



Phase-1 Upgrade: Expanded architecture