



CERN CMS  
Beam Radiation, Instrumentation and  
Luminosity (BRIL) group



Dept. of Computer Systems  
Tallinn University of Technology, Estonia

Konstantin Shibin on behalf of BRIL (CMS)

---

# Electronics design and testing of the CMS Fast Beam Condition Monitor for HL-LHC



Technology & Instrumentation in Particle Physics (TIPP 2023)  
September 7th 2023, Cape Town

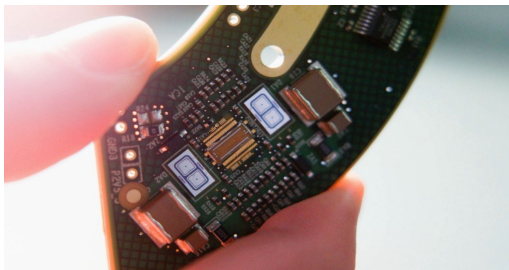
# Need for a new Dedicated Luminometer

Dedicated standalone luminometer in CMS measures beam luminosity and beam-induced background (BIB) independent of other infrastructure.

- Always on when beams are present
- Orthogonal systematic error to other CMS subsystems

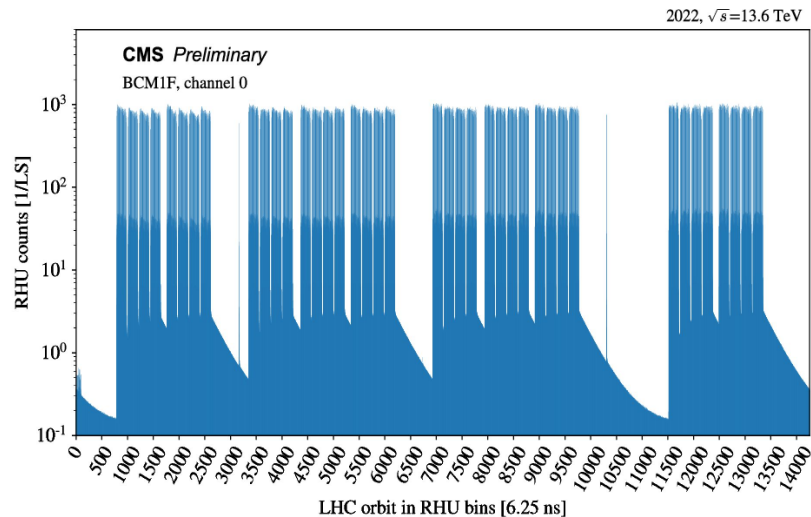
Previous luminometer BCM1F designed for BIB and luminosity measurement has been **successfully used in LHC Run 2 & 3**

- Fast, asynchronous front-end ASIC
- Simple design: analogue read-out, signal processing at the back end (BE)
- Run-3 design based entirely on Si-pad detectors
  - Designed for  $1.5 \times 10^{15}$  1 MeV n eq fluence
  - Excellent linearity



There is a strong need for a new upgraded independent luminometer for HL-LHC

- Per-bunch luminosity measurement at full 40 MHz rate
- Improved sub-bunch timing resolution allowing BIB measurement
- Ambitious luminosity precision goal for Phase-2 (2% online and <1% offline)

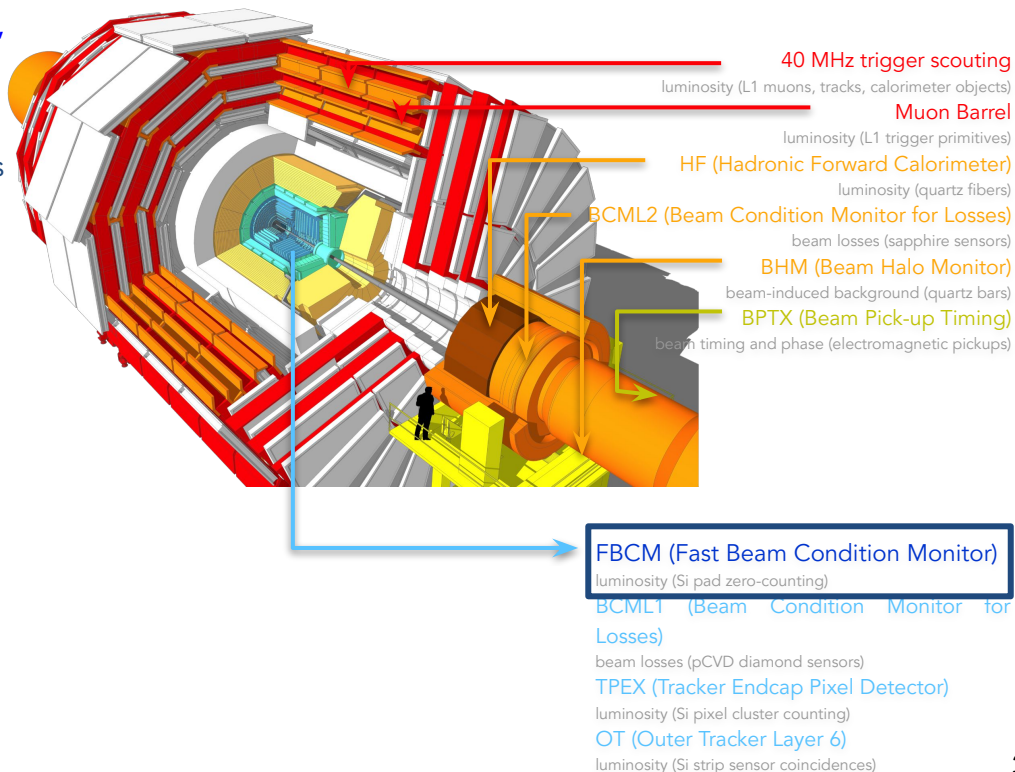


Example histogram of measured BCM1F raw counts integrated over 1 lumi section (LS~23 s). The "afterglow" tails following every bunch train are clearly visible. Detector has timing resolution of 4 bins in each bunch-crossing

# Fast Beam Condition Monitor (FBCM)

Fast Beam Condition Monitor is the next dedicated luminometer constructed by the Beam Radiation, Instrumentation and Luminosity (BRIL) group of CMS

- Planned for Phase-2 upgrade (HL-LHC)
- Upgrade and the successor of previous luminometer BCM1F
- New front-end and back-end electronics
- More sensors and measurement channels
  - 48 in BCM1F vs. 288 in FBCM
- CO<sub>2</sub> cooling for components
- Binary (semi-digital) signals instead of analog



## Fast Beam Condition Monitor (FBCM) aims at higher performance for HL-LHC

Simple front-end (FE) electronics system with **dedicated rad-hard 65 nm ASIC**

- Binary output starting at time of arrival (ToA) and lasting for time over threshold (ToT) sampled upstream by a low power gigabit transceiver (IpGBT)
- Signal processing in FPGA-based back-end (CERN Apollo board)

**Measuring BIB & luminosity** by applying the 'zero-counting' algorithm with hits on Si-pad detectors

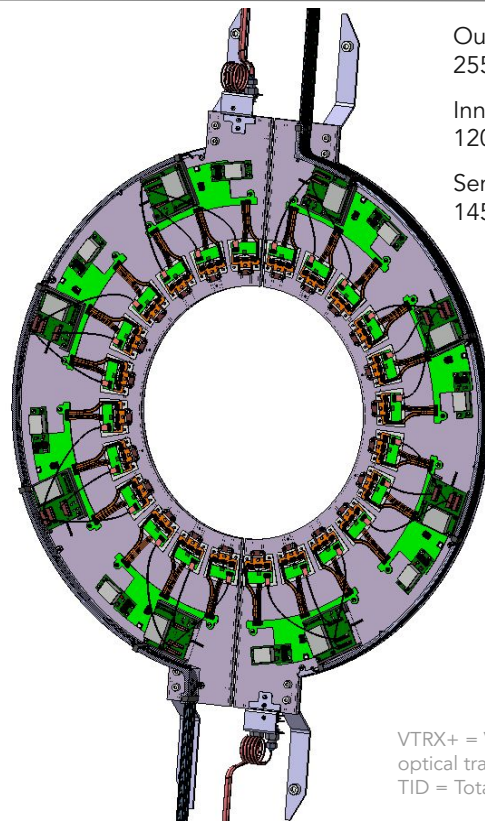
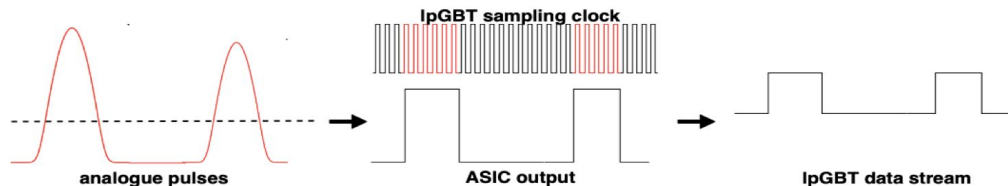
- Data collected in histograms in the back-end

Modernising the electronics (system architecture) - design uses **standard HL-LHC electronics** components for high-radiation environment: IpGBT, VTRX+ & DC-DC converters

- Widely used across CMS and qualified to the radiation levels at the FBCM location (expected 1 MeV n eq fluence is  $\sim 2.2 \times 10^{15} \text{ cm}^{-2}$  for 4000 fb<sup>-1</sup>, TID(Si) is  $\sim 109 \text{ Mrad}$ )

Moving from a tightly integrated detector system to a **highly modular system**

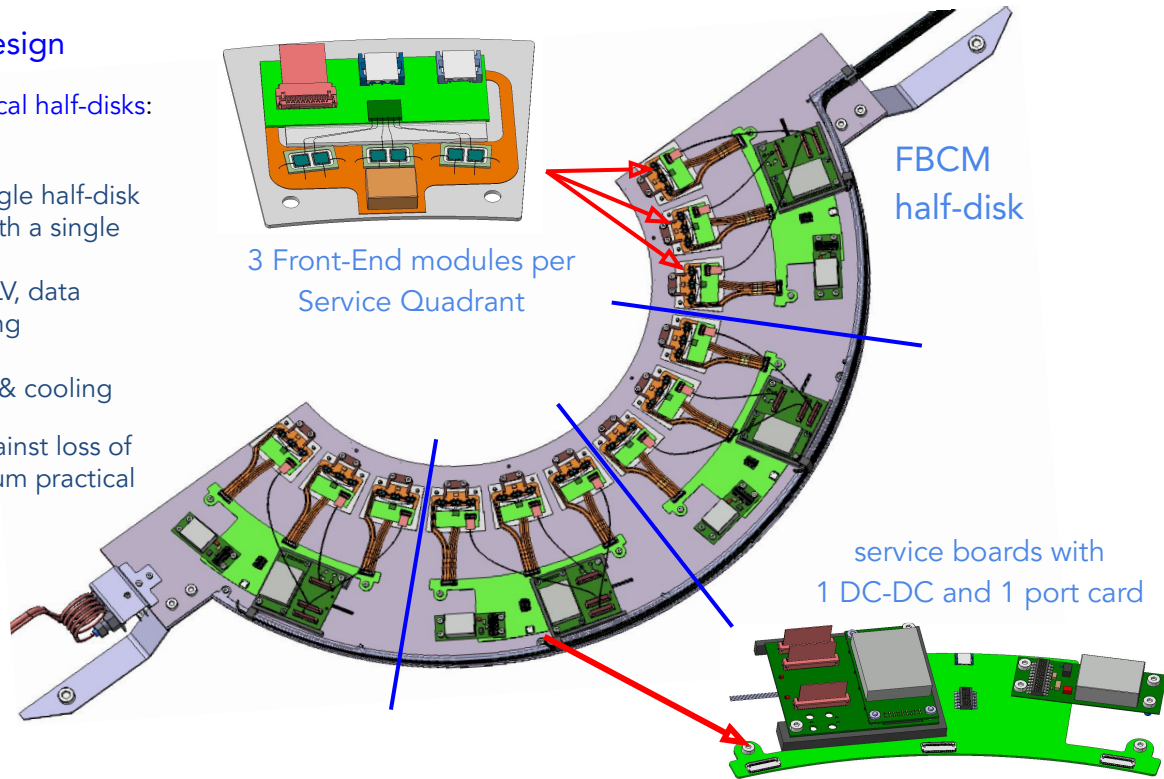
- to avoid 'single-point-of-failure' scenarios for large detector sub-assemblies
- to facilitate design, production and integration, and to ease the replacement of failing components



VTRX+ = Versatile Link + optical transceiver  
TID = Total Ionizing Dose

## FBCM uses a fully symmetric modular design

- Full FBCM system is **4 identical mechanical half-disks**:  
2 per each end of CMS
- **4 identical service quadrants** within a single half-disk
  - **3 identical front-end modules** with a single FBCM ASIC & 6 Si-pads
  - Service board providing FE HV/LV, data read-out, slow-control, monitoring
  - DC/DC converter and portcard
  - Supported by common services & cooling
- FBCM performance is **highly tolerant** against loss of individual channels, yet maintain maximum practical granularity in services
- **CO<sub>2</sub> cooling** for sensors, ASICs, port cards and DC-DC converters

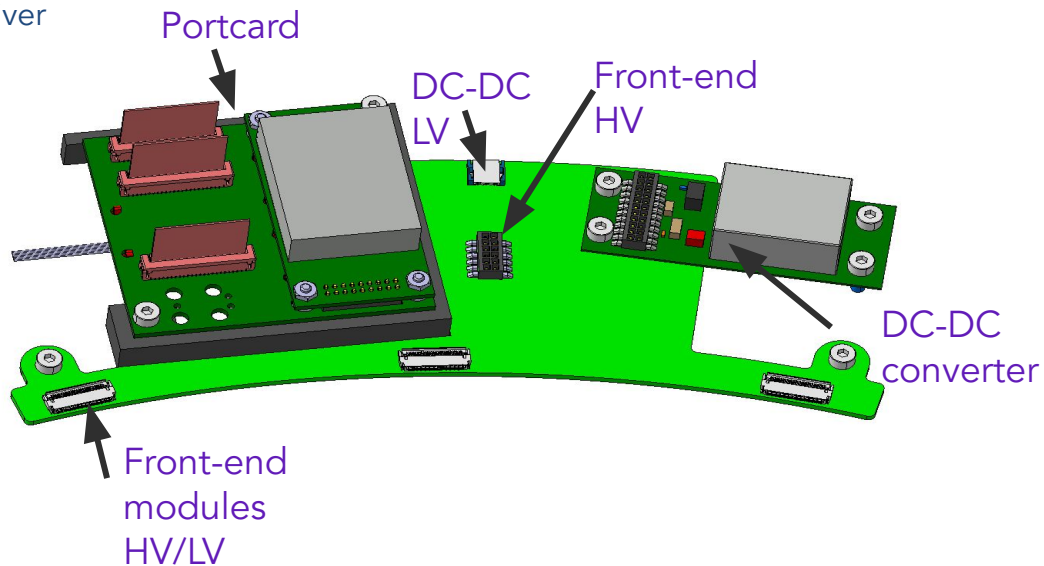


## Service board contains:

- IT portcard
  - 3 **lpGBT**: low-power gigabit transceiver
  - 3 **VTRx+**: Versatile Link + optical transceiver
  - **E-links** to front-end modules
  - **bPOL12V**, **bPOL2V5**: DC-DC converters
- Connectors for HV/LV power of front-end modules
- DC-DC converter (**bPOL12V**) for 1.2V front-end power

## All components standard rad-hard HL-LHC

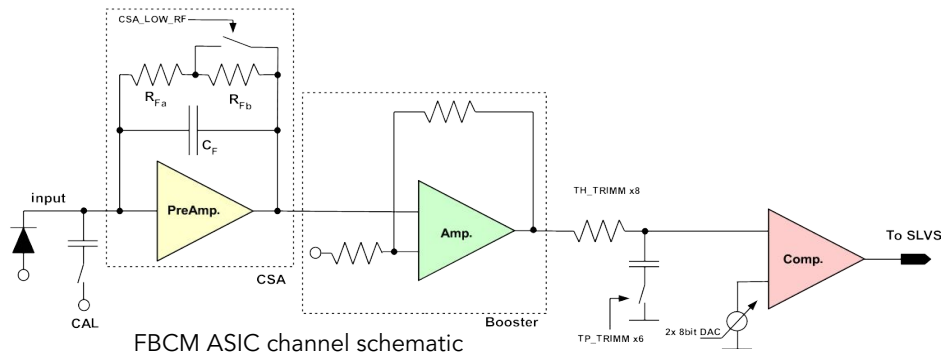
- lpGBT, VTRx+
- bPOL12V, bPOL2V5
- Qualified connectors





## Radiation-hard 65 nm binary front-end ASIC: 200 Mrad and $2.5 \times 10^{15} \text{ n/cm}^2$

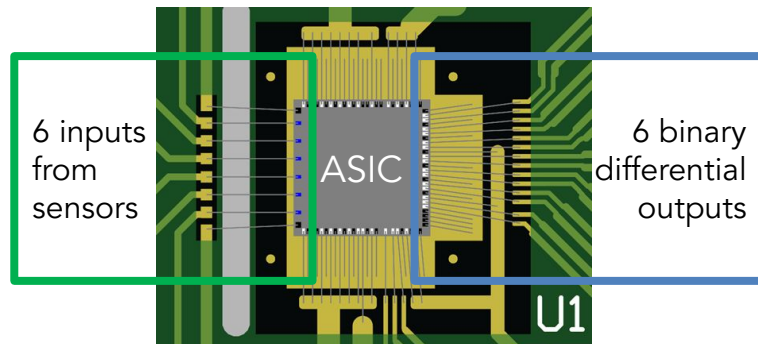
- Fast amplifier and comparator (sensor signal to threshold)
- Electronic noise below 900 e<sup>-</sup>
- Double hit resolution after discrimination: 25 ns
- Fast return to baseline after hit with multiple MIPs (150 fC)
- 6 channels per chip, SLVS output
- Trigger-less (asynchronous) readout
- SEU-protected I2C register block for ASIC configuration
- 3x3 mm<sup>2</sup>, wire-bonded



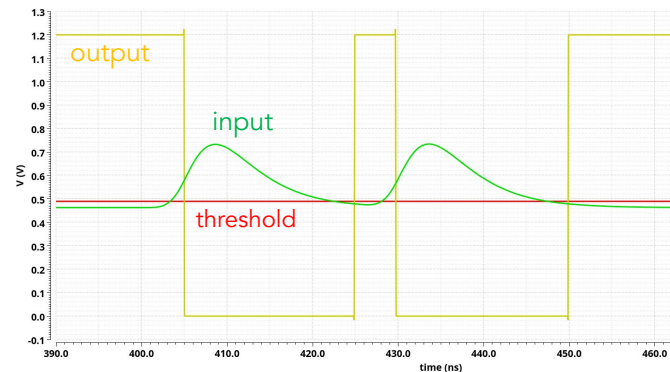
FBCM ASIC channel schematic

SLVS = Scalable Low-Voltage Signal

SEU = Single Event Upset (bitflip)



FBCM ASIC top view on test board



FBCM ASIC response to two consecutive 4.5fC signals

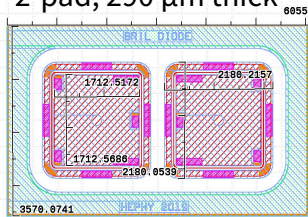
At FBCM sensor location expected 1 MeV n eq fluence is about  $2.5 \times 10^{15}$  for 3000 fb<sup>-1</sup> (outer tracker:  $1.5 \times 10^{15}$ ; inner tracker:  $1 \times 10^{16}$ ), planning for replacement after about 1500 fb<sup>-1</sup>

Two types of sensors are available for tests:

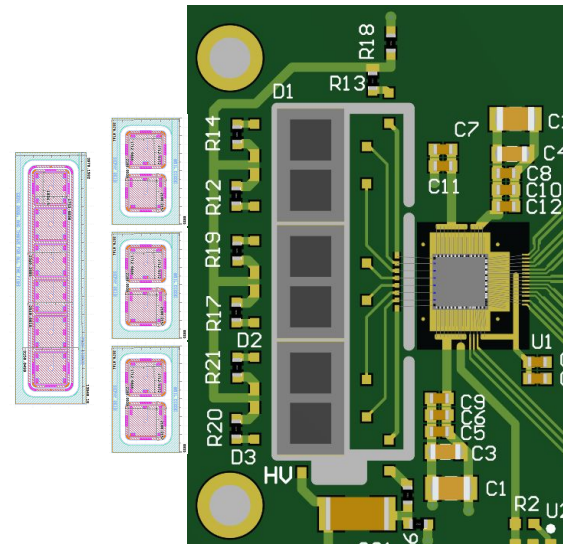
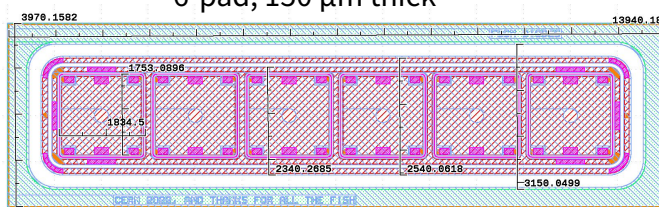
- 290  $\mu$ m (same as used in Run 3 BCM1F system)
  - better S/N (pre-radiation:  $\sim 35$ , after  $1 \times 10^{15}$ : 10.7)
  - high leakage current when irradiated  $\rightarrow$  high shot noise
- 150  $\mu$ m (need to validate these sensors for use in final system)
  - more rad-hard but lower signals
  - common GND ring to limit sensitive volume
  - worse S/N (pre-radiation: 17, after  $2.5 \times 10^{15}$ :  $\sim 8$ )
  - lower leakage current, thus shot noise

Final choice after test beam with ASIC and both types of irradiated sensors

2-pad, 290  $\mu$ m thick



6-pad, 150  $\mu$ m thick

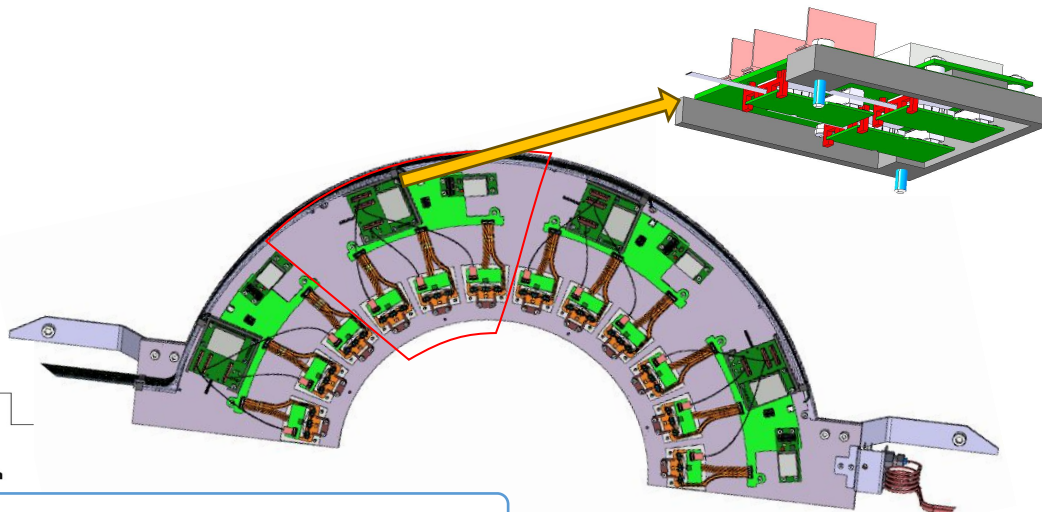
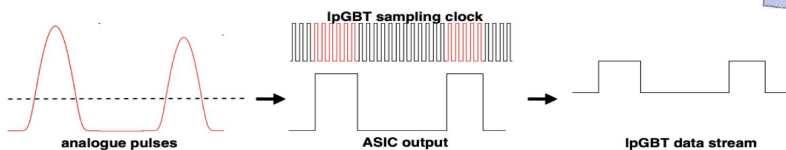


FBCM test board with ASIC and sensors



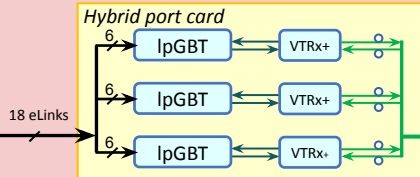
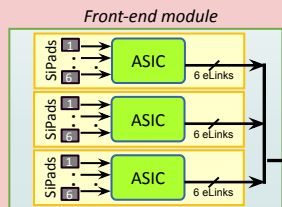
## Data-taking path:

1. Analog signal from sensors
2. ASIC comparator binary output
3. IpGBT (transceiver) & VTRx+ (optical interface)
4. Optical fiber to counting room
5. Back-end Apollo FPGA board
6. ToA and ToT sub-bunch-crossing histograms

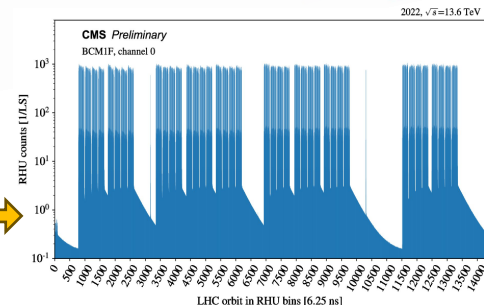
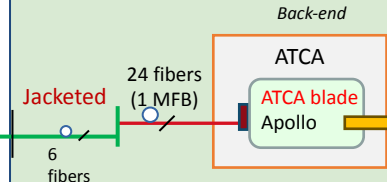


## Architecture of 1/4 of a quarter of FBCM

### High radiation (detector)

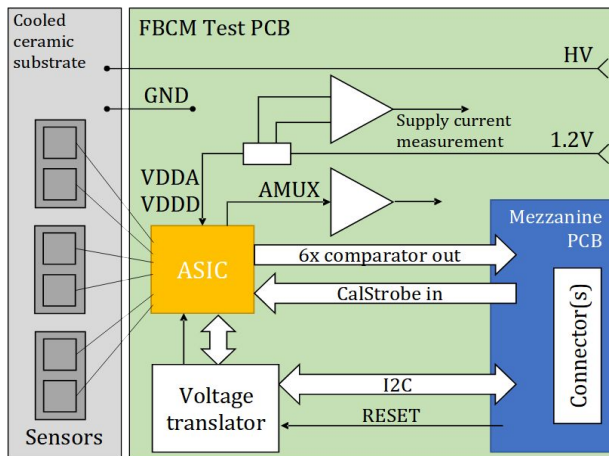


### No radiation (counting room)

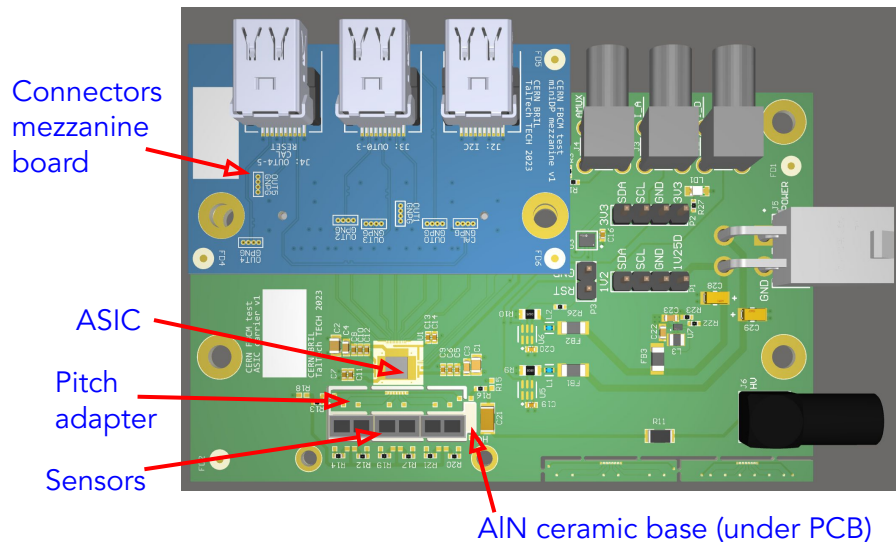


BRIL and TalTech are collaborating in the development of the test system for FBCM:

- Carrier board with ASIC, power, measurement, sensor connections
- AIN plate with sensor bias (HV) and good cooling properties
- Replaceable mezzanine board to allow connection to:
  - Back-end via galvanic links
  - Back-end via IpGBT optical links
  - Oscilloscope via SMA break-out



FBCM test board architecture



Test system is developed to support all testing needs throughout the project lifetime

## 2023 Stage 1: Lab bare ASIC tests (for several chips):

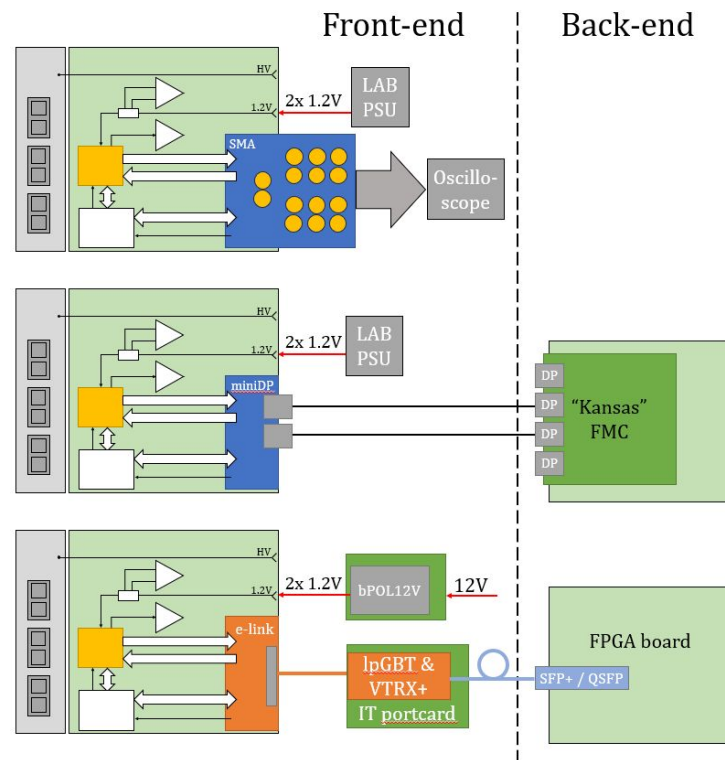
- ASIC validation and initial qualification using test points and AMUX output
  - I2C configuration using Raspberry PI Pico
  - Calibration strobe (Raspberry PI Pico, pulse generator, scope)

## 2023->2024 Stage 2: Lab ASIC + sensor + firmware test:

- ASIC testing with back-end FPGA firmware
- Galvanic connection (miniDP)
- Use radioactive source, check spectra with the scope
- Test with lpGBT links (when available)

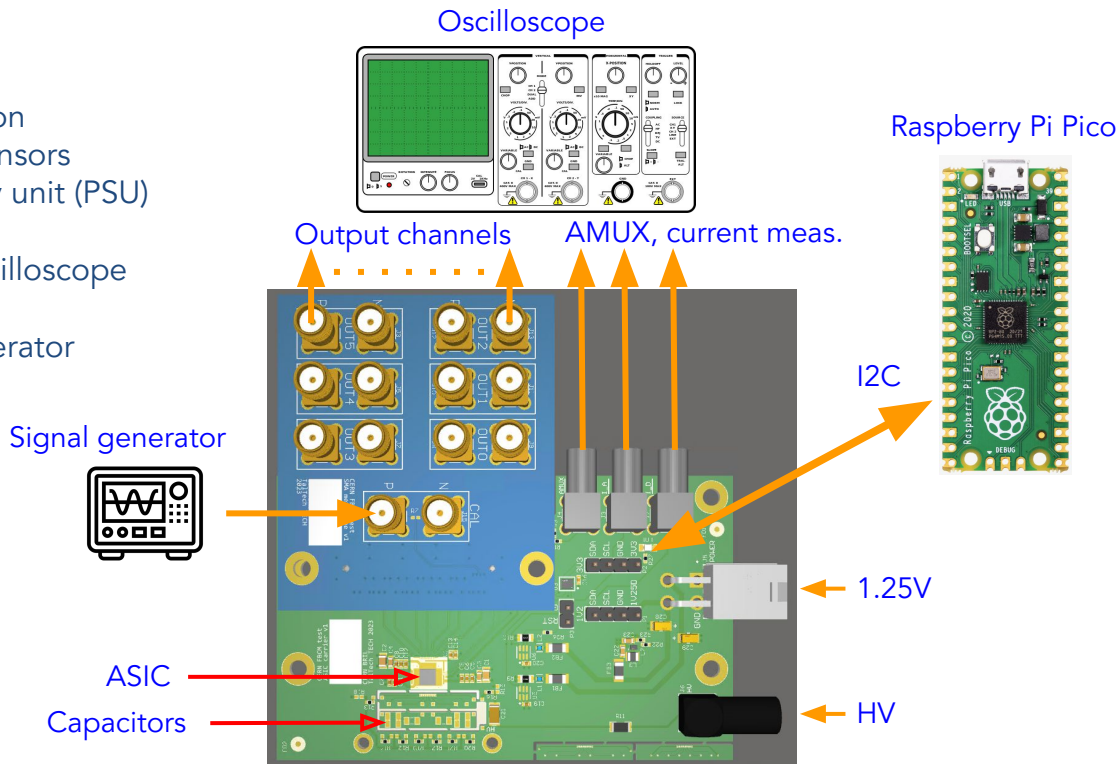
## 2024 Stage 3: test beam ASIC + sensor test + firmware:

- Qualification of ASIC & sensors before and after irradiation
- Gradually increase complexity of the system, approaching final design
  - DC-DC powering
  - Full read-out chain with lpGBT and VTRx+
  - I2C and reset via portcard
  - Firmware to decode lpGBT dataflow
  - Histogramming in the firmware
  - ToT monitoring



## Setup for initial ASIC testing

- ASIC validation and initial qualification
- At first with capacitors to emulate sensors
- Power (1.25V) from lab power supply unit (PSU)
- I2C configuration using Raspberry Pi
- Analog signal measurement with oscilloscope
- Current consumption measurement
- Calibration strobe from a signal generator



## Setup for sensor and FW testing

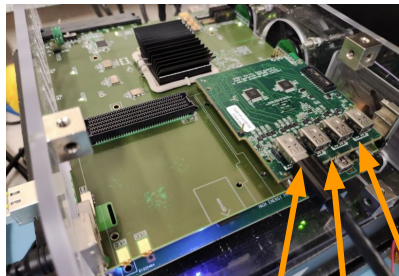
- Sensors mounted and wire-bonded
- Galvanic connection (miniDP) to back-end
- Back-end firmware on FC7 FPGA board
- Power (1.25V) from lab PSU
- I2C configuration using Raspberry Pi
- Calibration strobe from FPGA

## System tests and validation with test beam

- Test and read-out of the system with a radioactive source
- Fresh and irradiated sensors will be tested

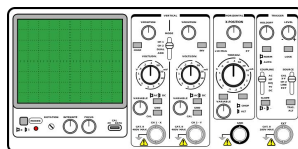
FC7 is a test and prototyping board used across CMS, hosts Kintex-7 FPGA with multi-gigabit transceivers and 2 FPGA mezzanine cards (FMC) slots.

## FC7 FPGA board + KSU-FMC



miniDP

## Oscilloscope



AMUX, current meas.

## Raspberry Pi Pico

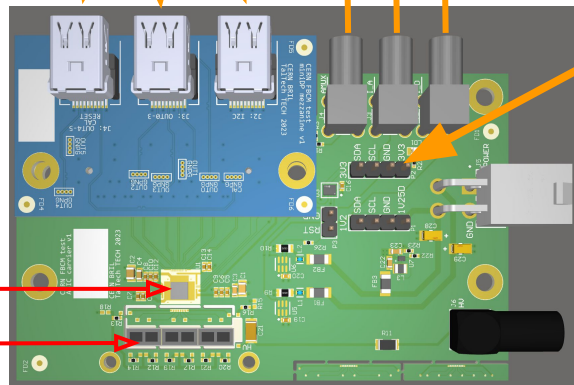


I2C

1.25V

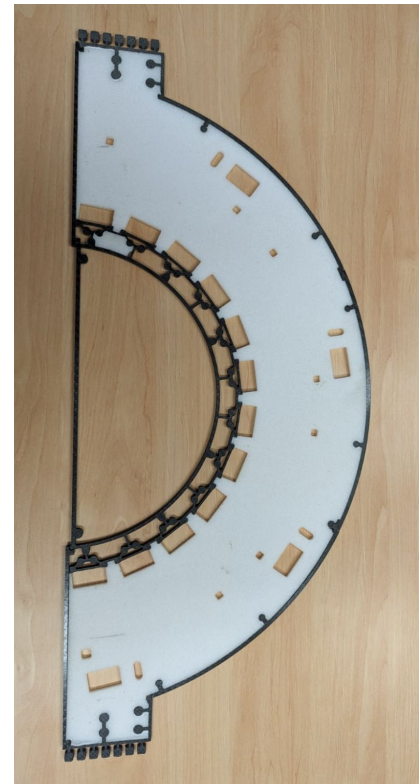
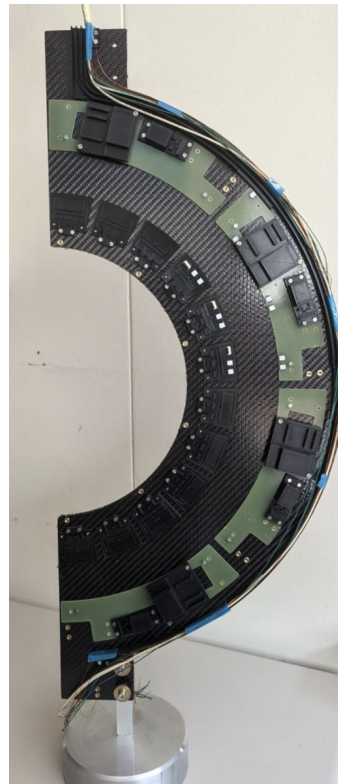
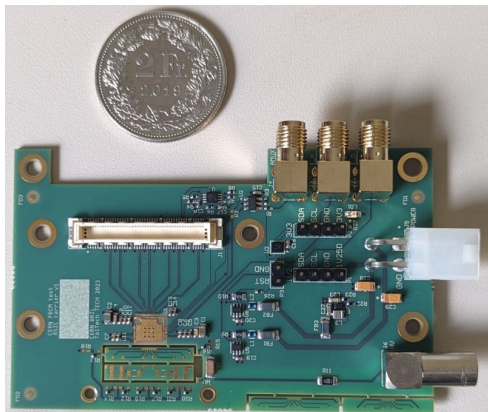
HV

ASIC  
Sensors  
(fresh and irradiated)





- FBCM ASIC expected September 2023
- Test board and adapter mezzanines manufactured
- Half-disk mock-up available
- Thermal prototype
- DC-DC module customization finished
- Portcards being modified to add I2C master port
- Characterization and irradiation campaign for 6-pad sensors ongoing
- Mechanical design being optimized to improve thermal performance





- **Dedicated stand-alone luminometer** Fast Beam Condition Monitor (FBCM) is under development and prototyping
  - Fast binary front-end with dedicated ASIC and sensors
  - On track for Phase-2 upgrade (HL-LHC)
  - Instrumental for HL-LHC to achieve luminosity measurement with 2% uncertainty online and < 1% offline
- FBCM designed to be **reliable and highly modular system**
  - Avoids single point of failure
  - Designed for robustness and maintainability
  - Uses standard and tested HL-LHC radiation-hardened components: optical links, power supplies
- **Testing and characterization of FBCM system** starts soon
  - Electronic design of the front-end test system ready
  - Several stages for testing of ASIC, sensors, firmware
  - ASIC and sensor irradiation campaign is scheduled. Final decision on the choice of the sensor technology will be made based on the outcomes
  - System tests and validation with test beam