

# The ATLAS Level-1 Topological Processor:

## Phase-I upgrade and Phase-II adaptation

### Outline:

- Introduction of the ATLAS hardware trigger system
- New Topo for Run 3
- Challenges for Run 4

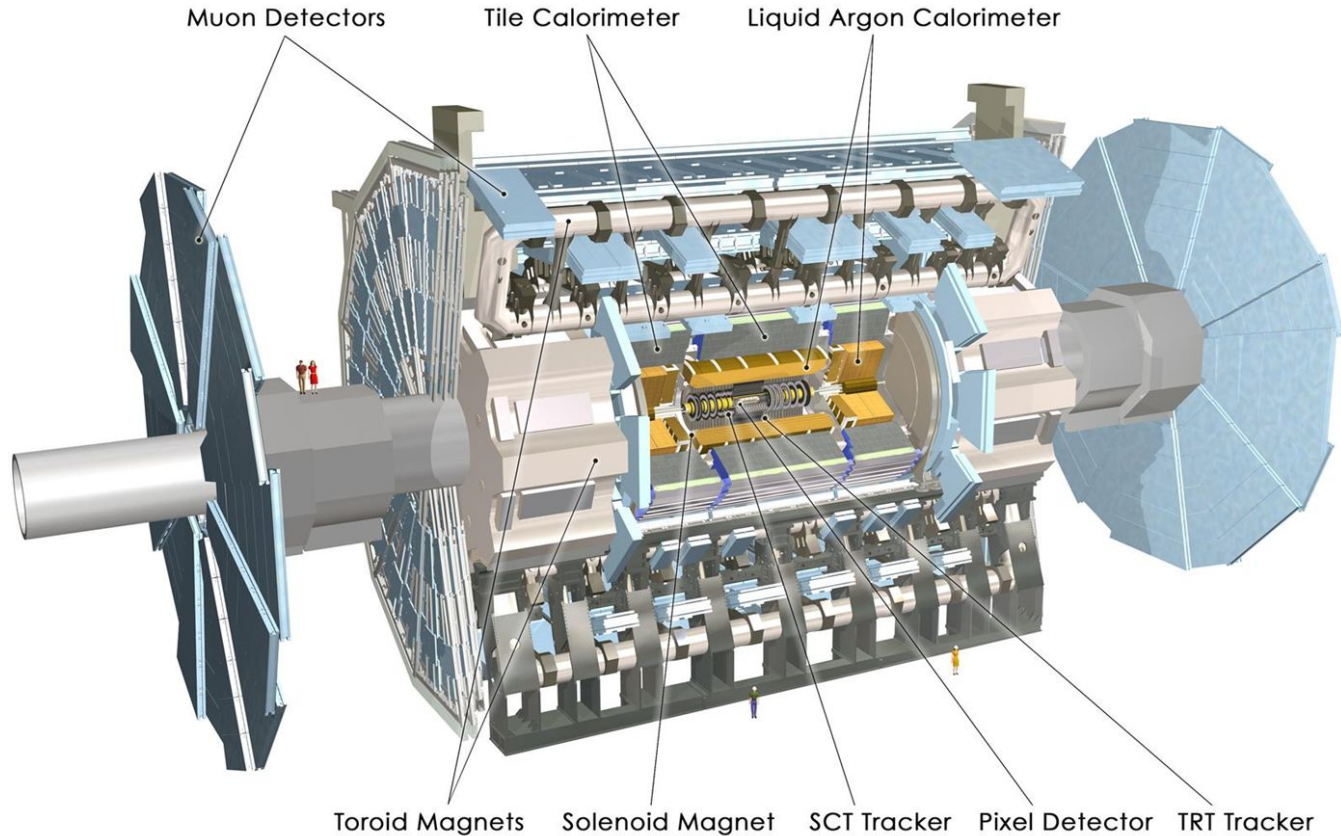
Emanuel Meuser *on behalf of the ATLAS TDAQ Collaboration*  
TIPP2023 | Capetown | 04.09.2023 - 08.09.2023



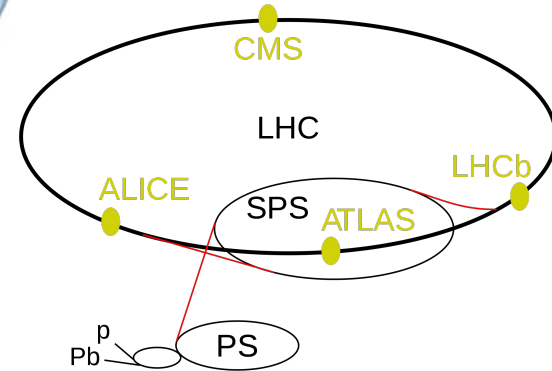
JOHANNES GUTENBERG  
UNIVERSITÄT MAINZ



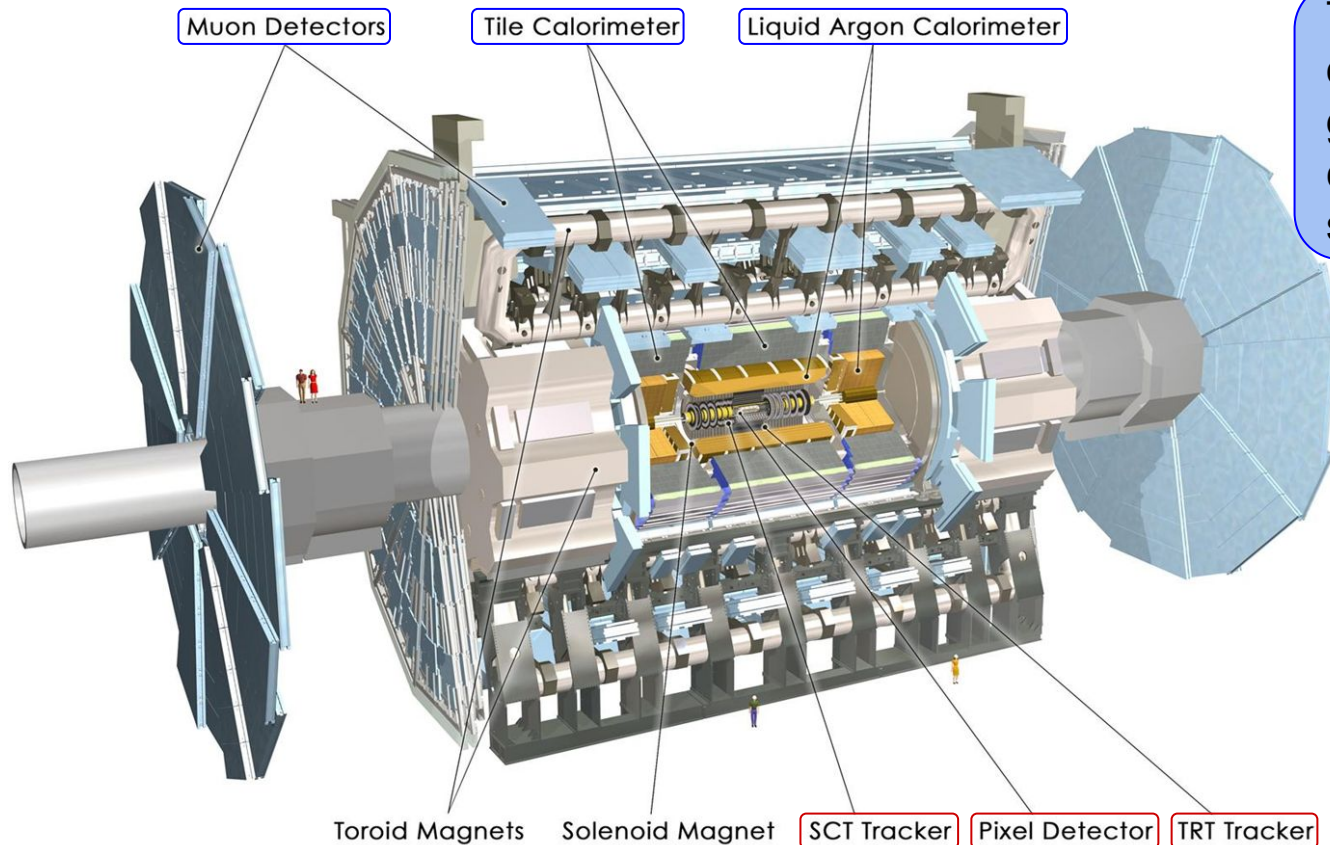
# Overview - The ATLAS detector



Bunches collide with a frequency of 40 MHz (every 25 ns)



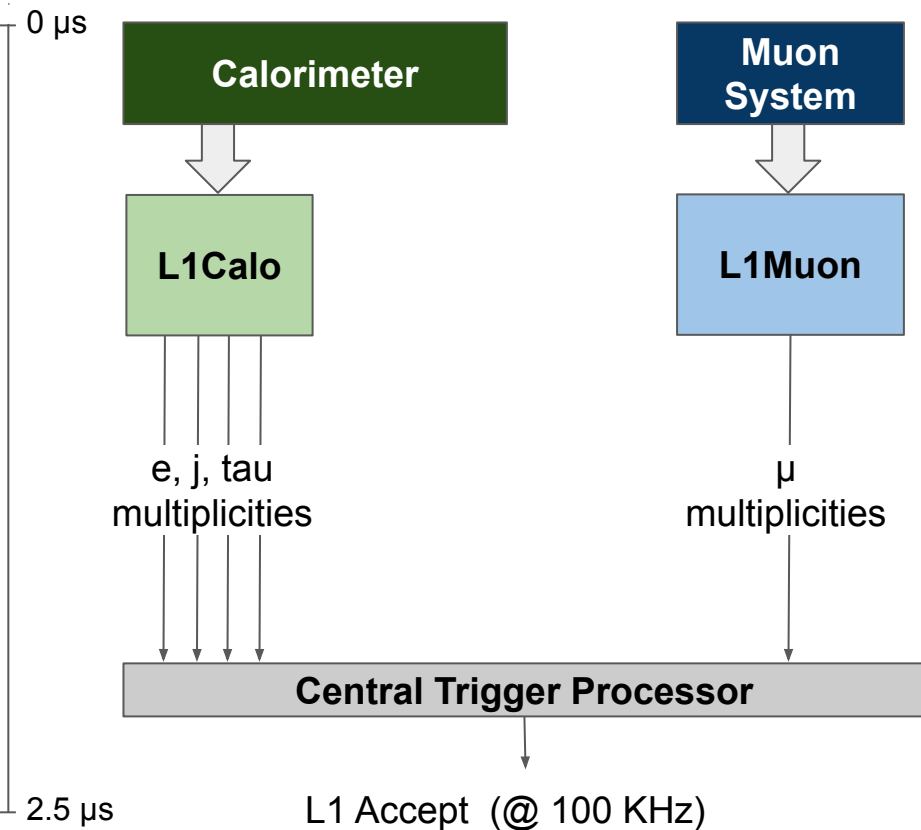
# Overview - The ATLAS detector



The hardware trigger works on information of reduced granularity from the calorimeters and the muon spectrometer at 40 MHz

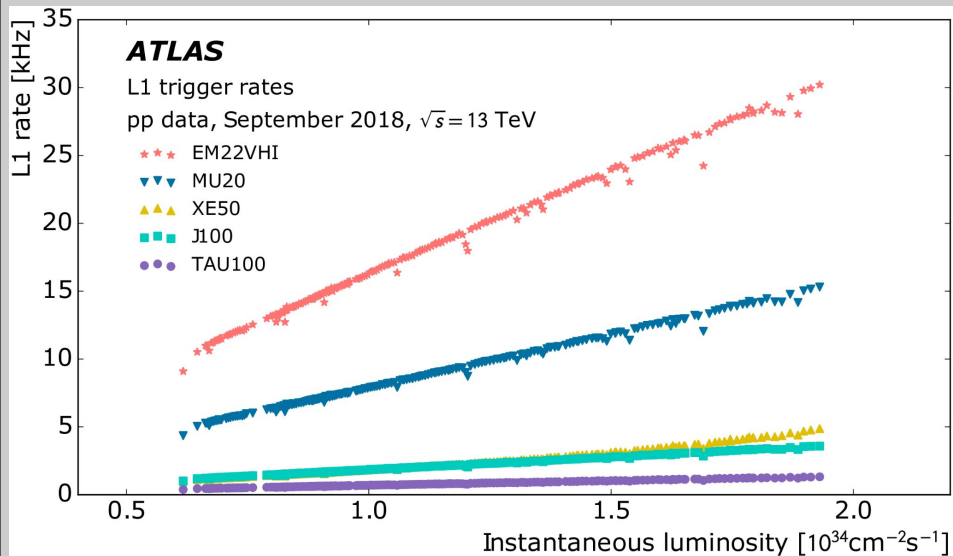
Inner detector cannot be read out full at LHC BX frequency of 40 MHz!

# ATLAS Level-1 Trigger System - Run 1 (2011 - 2012)



The Run1 L1-Trigger was based on multiplicities of Clusters and Muons over a certain energy threshold However:

- Increase in luminosity (and subsequently pileup) increases rate
- To reduce the rate, the thresholds have to be raised

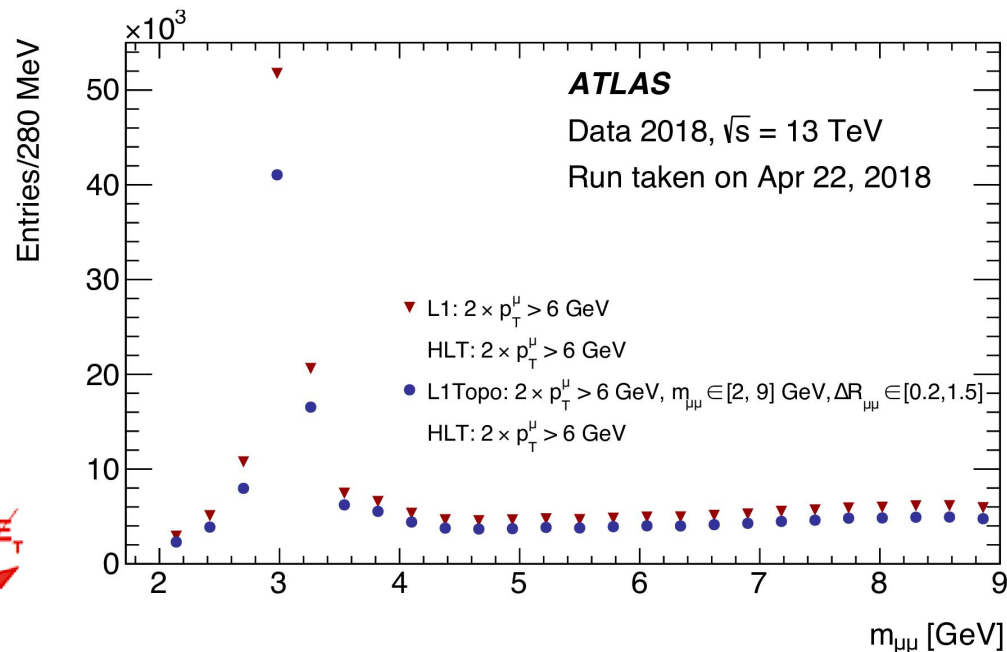
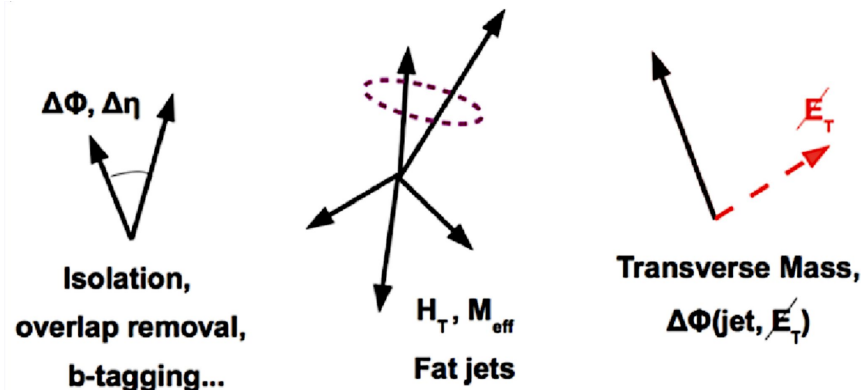


# Concept of a topological trigger

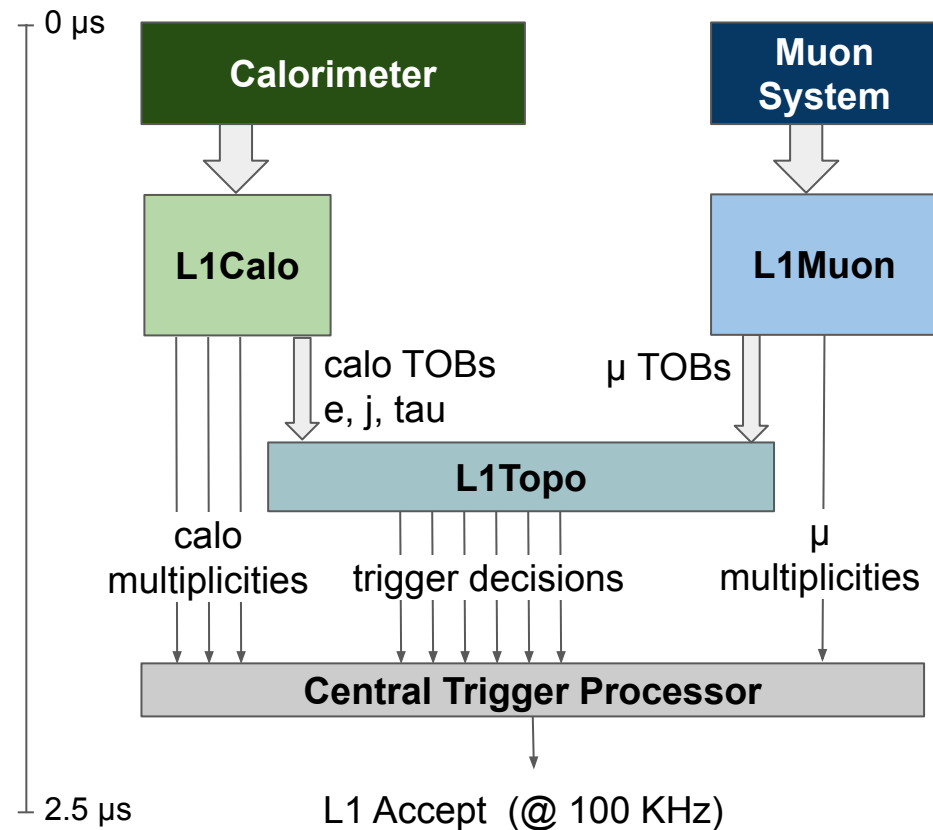
Introduce additional topological criteria:

- $\Delta\eta$
- $\Delta\phi$
- $\Delta RSqr$
- Invariant Mass
- Hardness  $H_T$  ( $\sum Jet p_T$ )

Reduction of rate without change of thresholds => no bias!

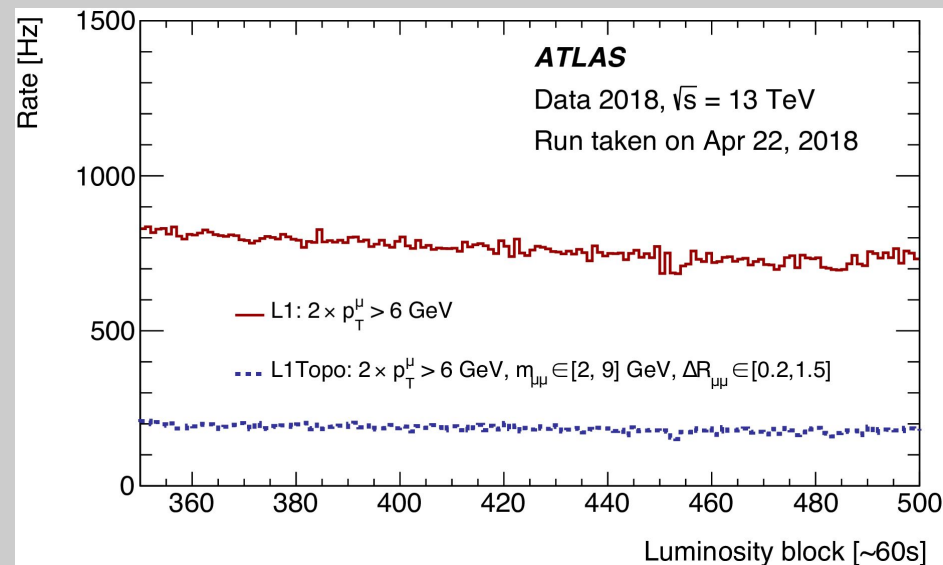


# ATLAS Level-1 Trigger System - Run 2 (2015 - 2018)

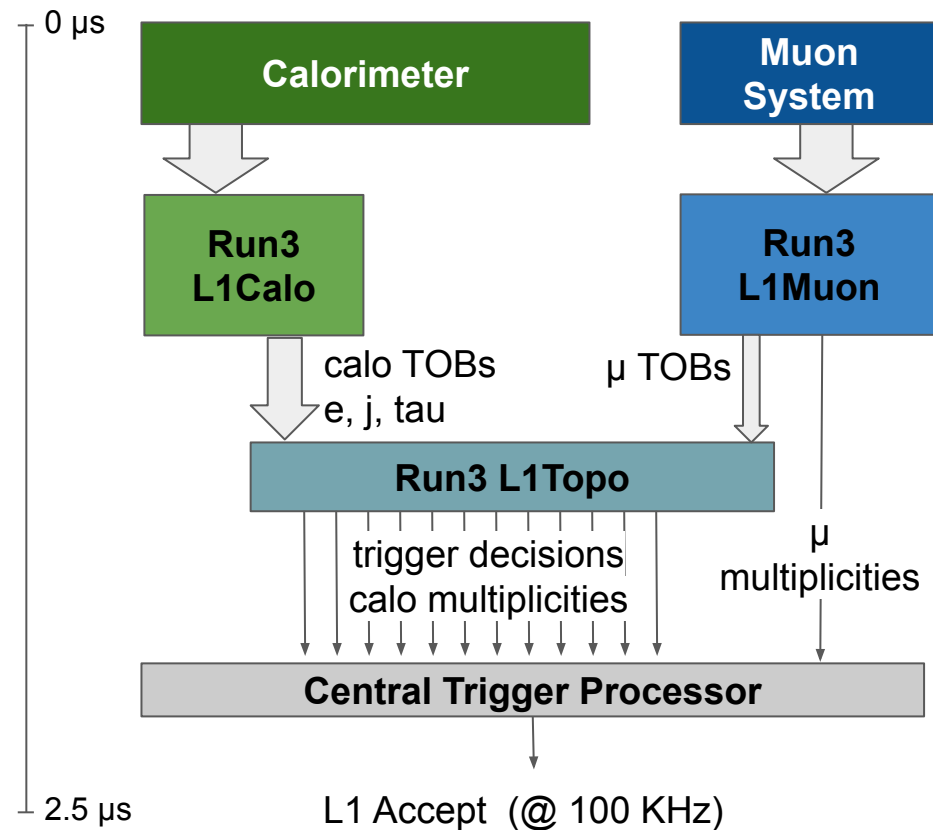


## Introduction of L1Topo in Run2:

- L1Calo and L1Muon send Trigger Objects (TOBs) to L1Topo
- Additional trigger decisions based on topology of trigger objects
- lowers rates significantly



# ATLAS Level-1 Trigger System - Run 3 (2022 - 2025)



Phase-1 Upgrade of the L1 Trigger system:

- Upgrade of [L1Calo](#) + L1Muon
- Increase in granularities and better identification
- Increases number of TOBs
- calo multiplicities now done by L1Topo
- higher bandwidth and performance requirements on L1Topo

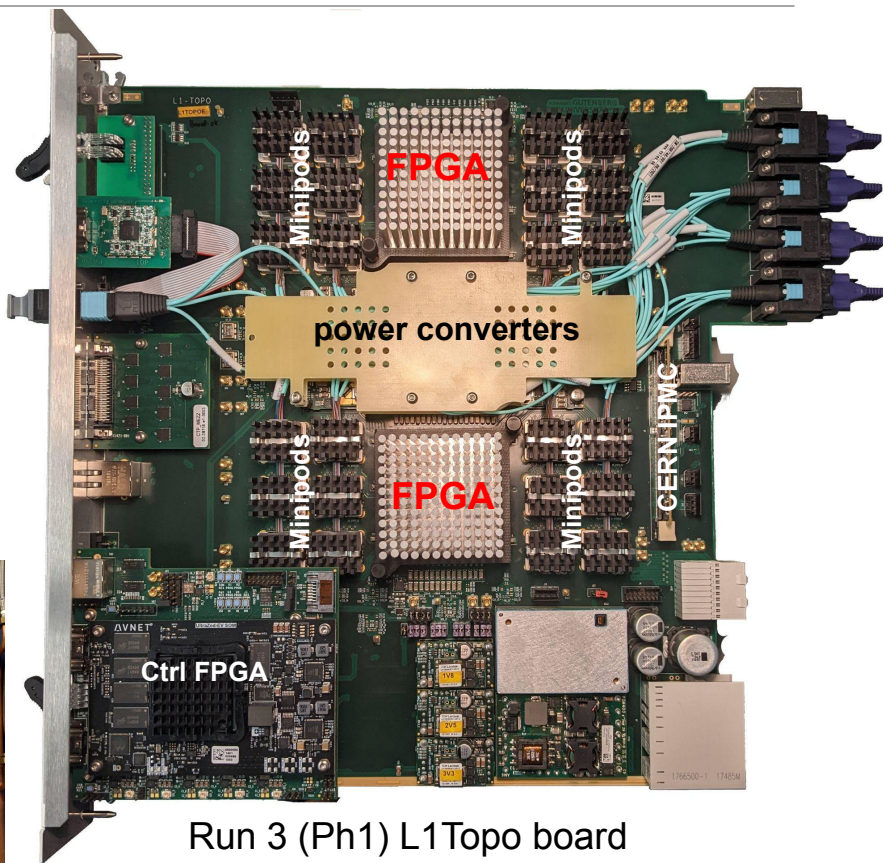
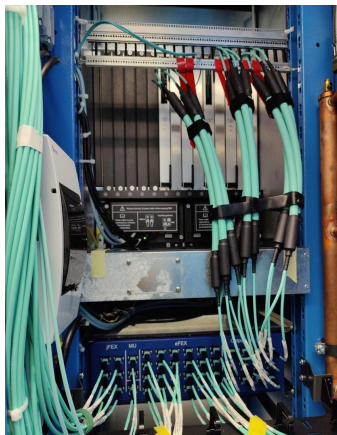
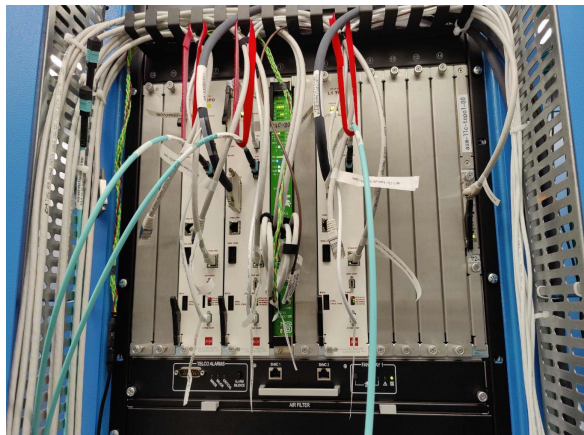
=> New topological trigger system needed:

**The Run3 L1Topo**



# Run 3 L1Topo - Hardware Overview

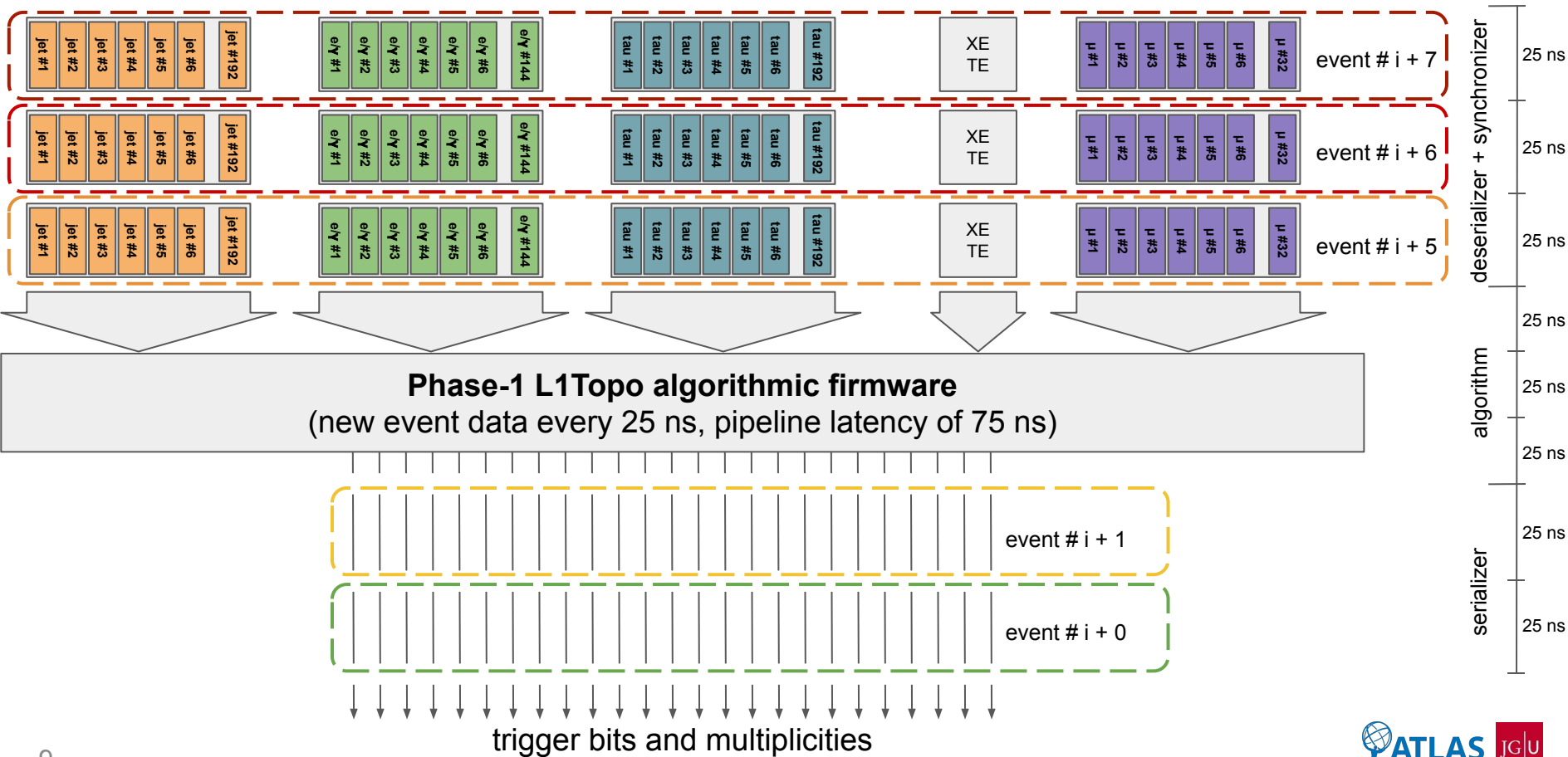
- 3 dual width, **custom-designed** ATCA boards
- 2 processor FPGAs (VU9P) per board
- 12 Minipod opto/electrical transceivers per FPGA
  - 10 receivers and 2 transmitter per FPGA
  - running at 11.2 Gbps per channel
  - system's total receiving bandwidth at 8 Tbits
- Zynq SOM as module controller
  - FPGA + ARM
  - Provides control signals to FPGAs
  - Programs processor FPGAs on power up
- Last board installed 28th of January 2022



Run 3 (Ph1) L1Topo board



# Run 3 L1Topo - LHC BX synchronous firmware (25 ns = 1 tick)



# Run 3 L1Topo - algorithmic firmware overview

## Run3 L1Topo algorithmic firmware:

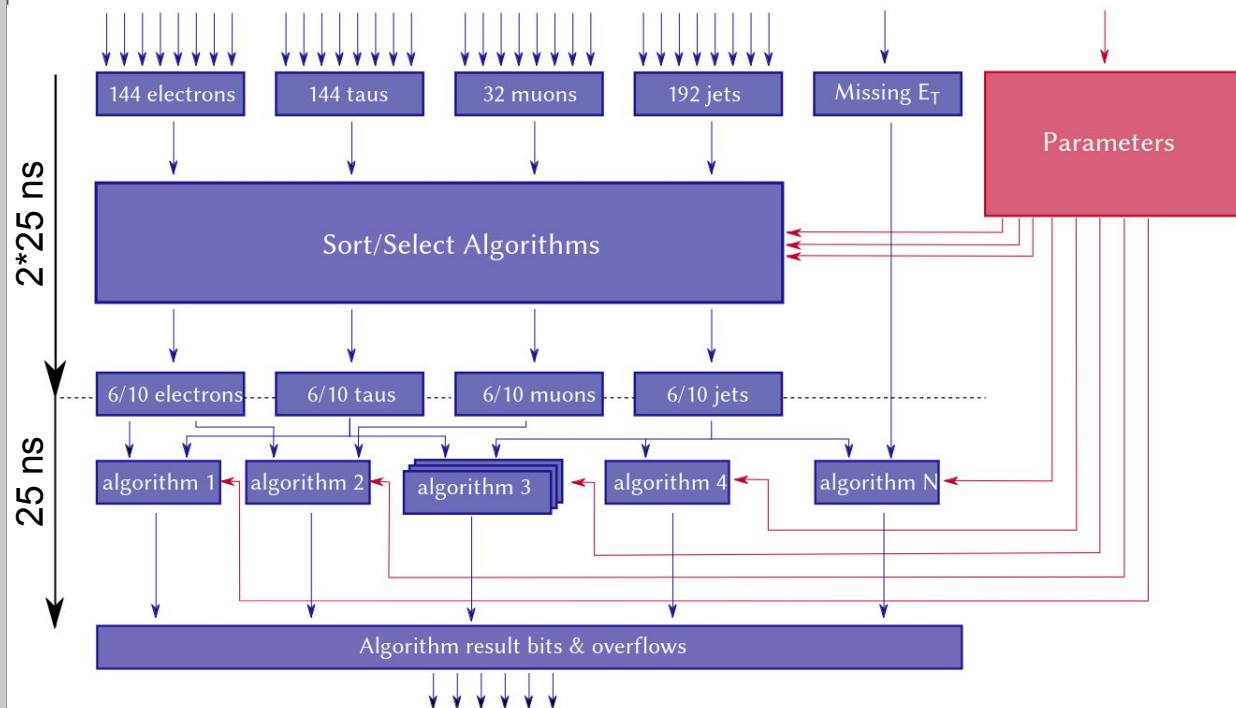
2 stage approach:

1. Sort/Select stage:

- 2\*25 ns latency budget
- reducing the # of TOBs in 2 ticks

2. topological algorithms:

- 25 ns latency budget
- calculations performed in single tick



# Run 3 L1Topo - algorithmic firmware overview

## Example chain from L1Topo:

### FjJjs23ETA49: ( $2 \times 25$ ns)

**In:** 192 jet TOBs

- select jets TOBs in fwd region ( $2.3 < |\eta| < 4.9$ )
- sort by  $E_t$

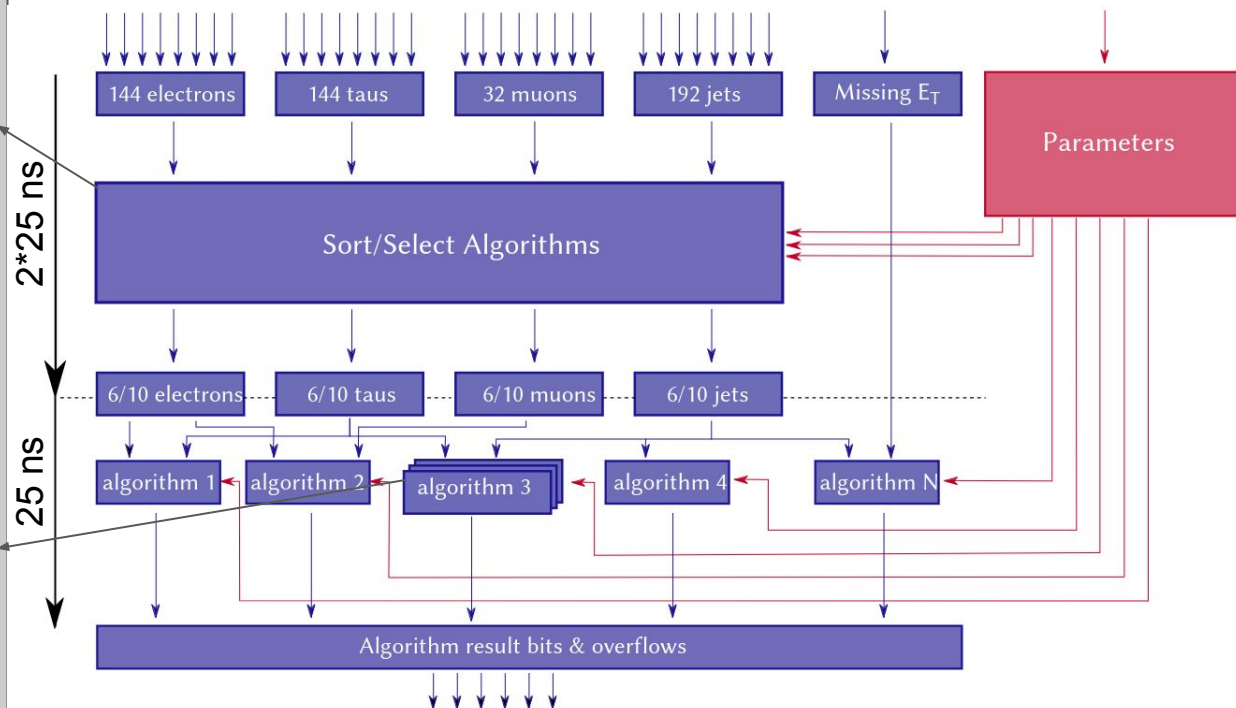
**Out:** 6 sorted fwd jet TOBs

### ZAFB\_DPHI: (25 ns)

**In:** 6 sorted fwd jet TOBs and 10 selected e TOBs

- further  $E_t$  criteria on TOBs
- Calc  $\Delta\phi$  for all 60 comb.
- Calc Invm for all 60 comb.
- Trigger for if comb. meets  $E_t$ ,  $\Delta\phi$  and Invm thresholds

**Out:** Accept/Reject (trigger bit)



# Run 3 L1Topo - example topological algorithm

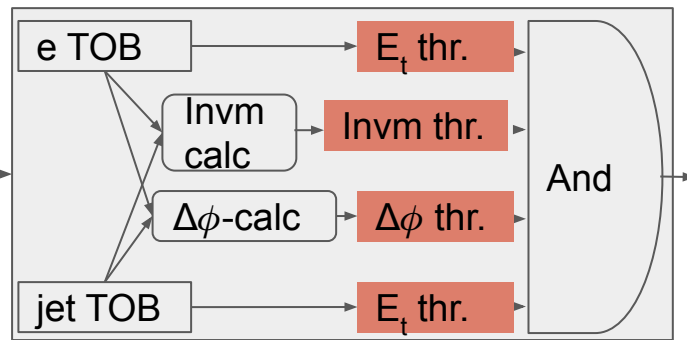
## ZAFB\_DPFI: (25 ns)

**In:** 6 sorted fwd jet TOBs and 10 selected e TOBs

- further  $E_t$  criteria on TOBs
- Calc  $\Delta\phi$  for all 60 comb.
- Calc Invm for all 60 comb.
- Trigger for if comb. meets  $E_t$ ,  $\Delta\phi$  and Invm thresholds

**Out:** Accept/Reject (trigger bit)

trigger logic  
for one  
combination



trigger logic for all 60  
combinations in parallel within  
a single clock tick (25ns)

6  
sorted  
fwd  
jets

10 selected e - Tobs

a b c d e f g h i j

	1	2	3	4	5	6	7	8	9	10
1	a	b	c	d	e	f	g	h	i	j
2	a	b	c	d	e	f	g	h	i	j
3	a	b	c	d	e	f	g	h	i	j
4	a	b	c	d	e	f	g	h	i	j
5	a	b	c	d	e	f	g	h	i	j
6	a	b	c	d	e	f	g	h	i	j

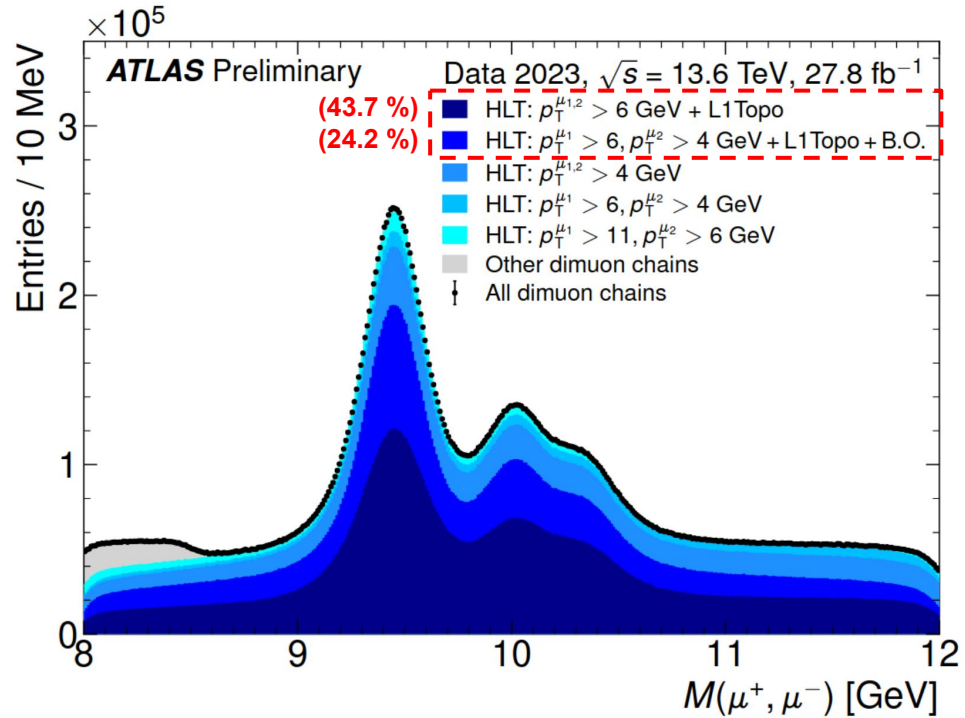
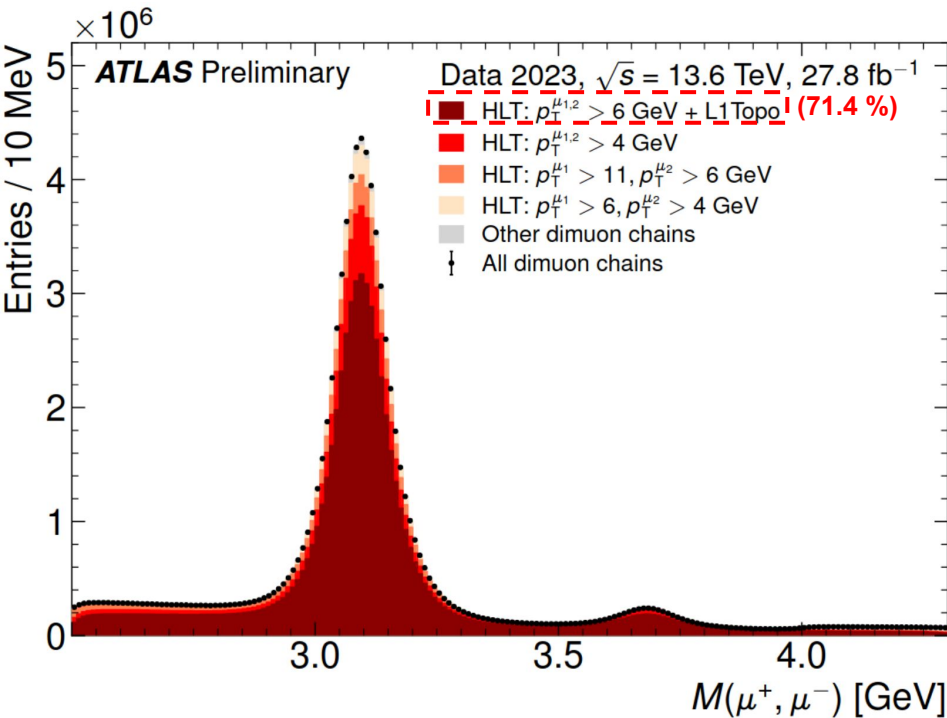
OR

trigger  
bit

## Highly parallelized:

- cost scales with #TOBs often quadratic (or cubic)
  - #TOBs reduced in Sort/Select stage
- implementation of example algorithm uses 31'732 LUTs
- algorithmic firmware occupies **2.5M LUTs** across 6 FPGAs (VU9p)

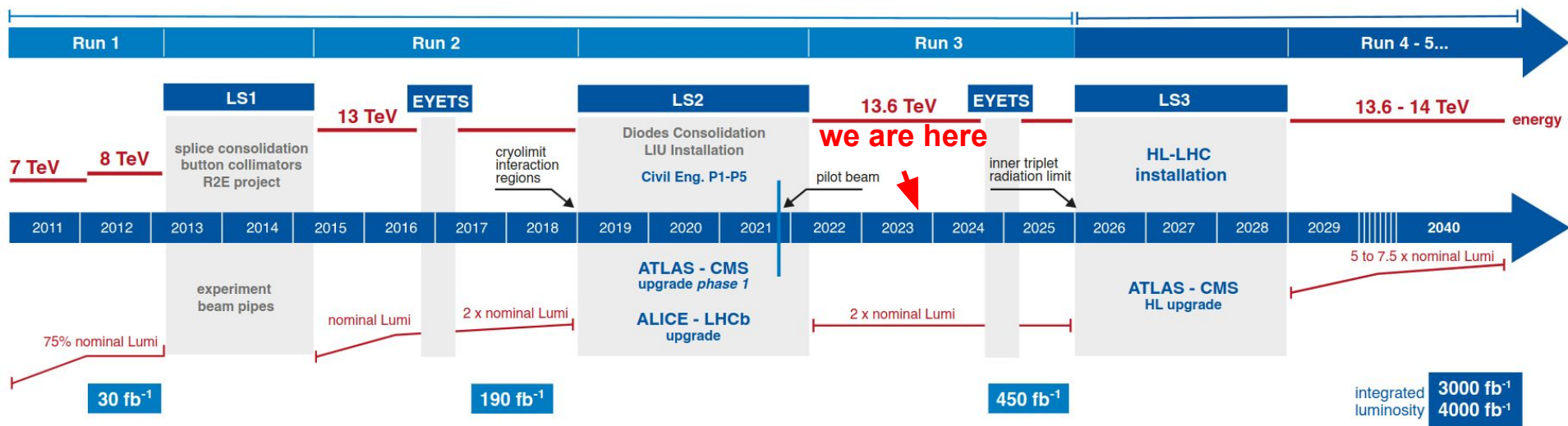
# Run 3 L1Topo - First performance results from Bphysics



**Run3-L1Topo chains provide ~ 70 % of unique rate for J/Ψ and Υ candidates!**



# LHC schedule - Towards Higher Luminosities

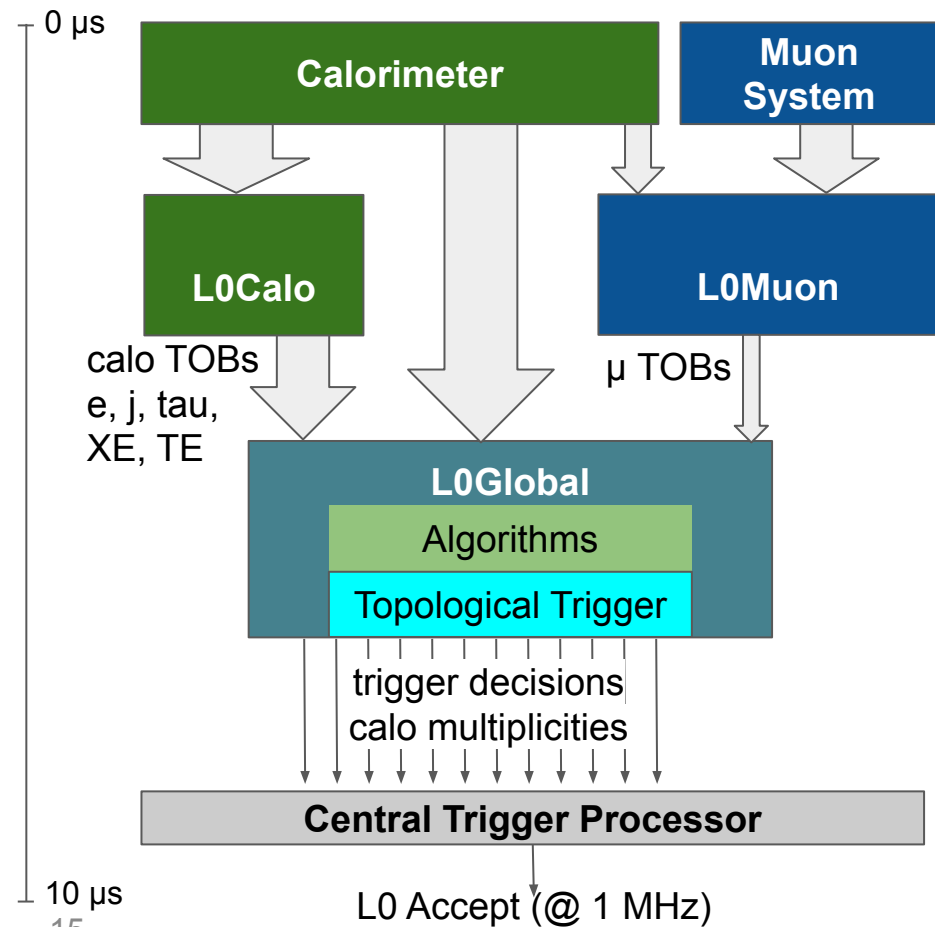


High Lumi - LHC brings challenges for the Trigger:

- Luminosity of up to  $7.5 \cdot 10^{34} \text{ cm}^{-1}\text{s}^{-1}$
- Pileup of up to 200 (60 in Run 3)

=> Adapt Trigger System for High-Lumi

# ATLAS Level-0 Trigger System - Run 4 and beyond

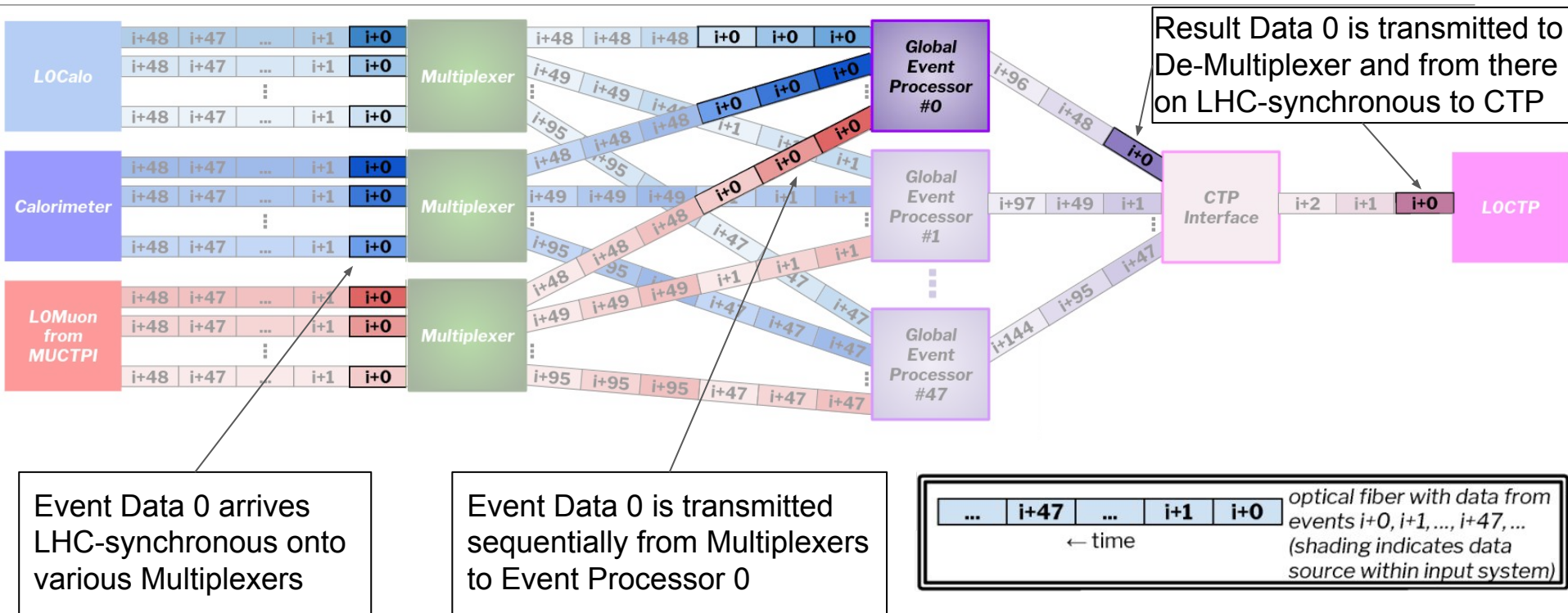


Changes for first level trigger for Run 4:

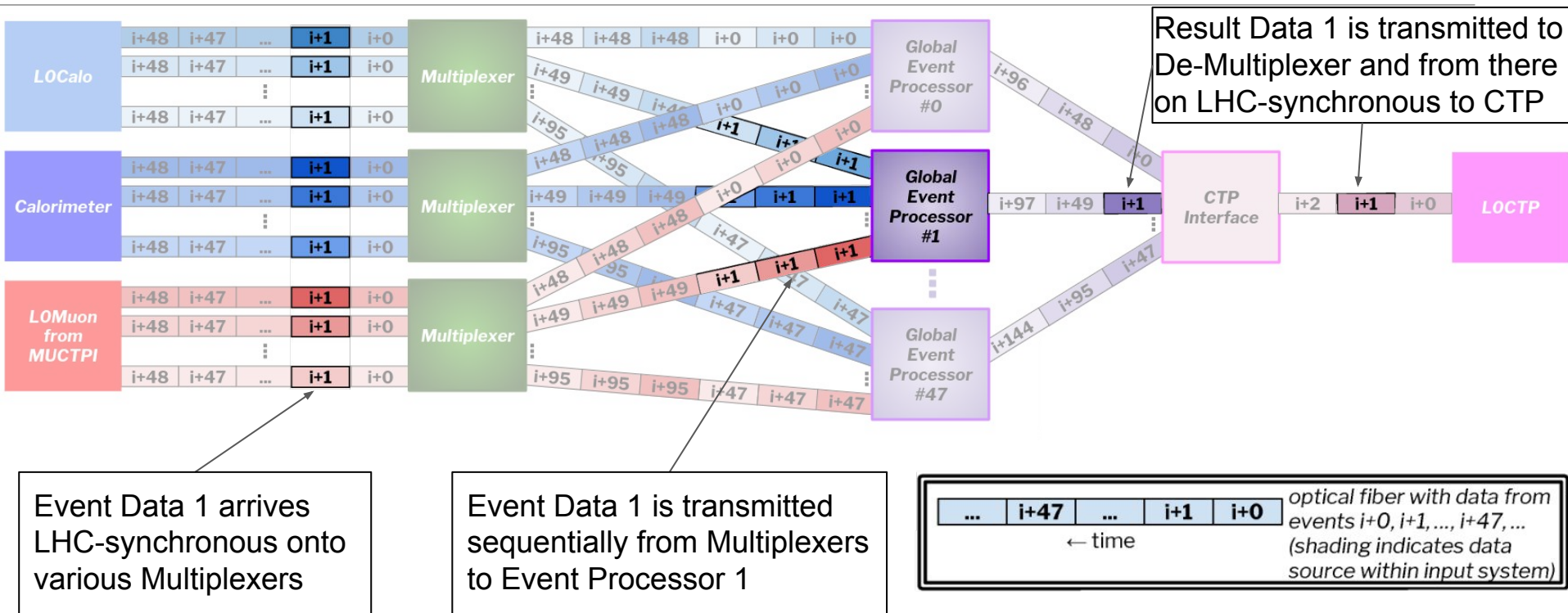
- Overall Latency for from 2.5  $\mu\text{s}$  to 10  $\mu\text{s}$
- Full cell-level granularity of whole detector combined on single FPGA of L0Global
  - TOBs from L0Calo and L0Muon
  - Run own e, j, tau, XE, TE algorithms to improve TOBs efficiencies
  - **Absorbs Topological Trigger**

=> Combins 1 event onto single FPGA at full granularity using time multiplexing

# L0Global - Time Multiplexing



# L0Global - Time Multiplexing



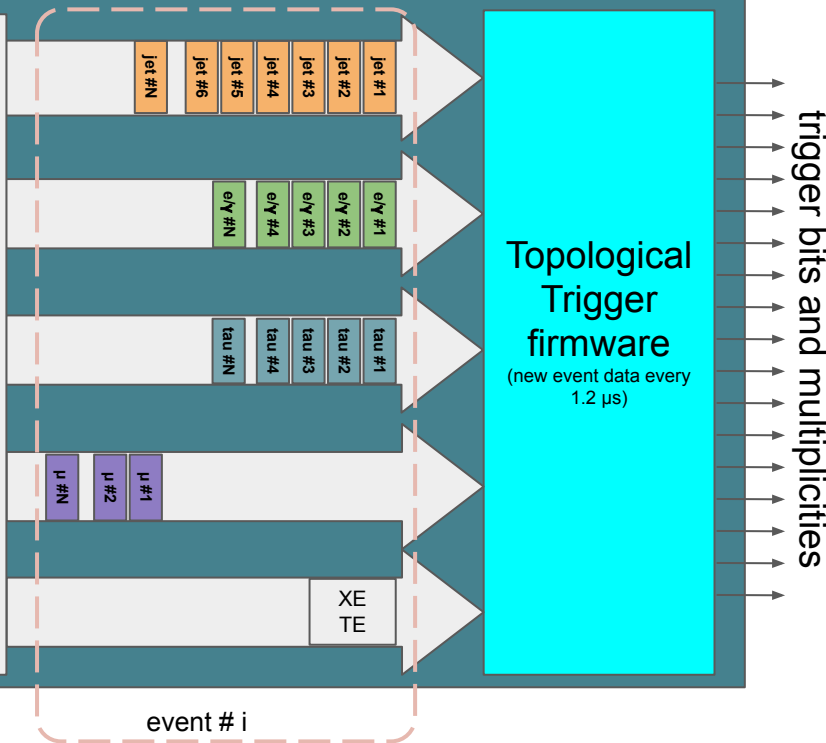
48 Event Processors  $\Rightarrow 48 * 25 \text{ ns} = 1.2 \mu\text{s}$  until next event on same Event Processor

# L0Global - time multiplexed topological firmware

## Algorithms:

- TopoClusters
- Jet algos
- Egamma
- Tau
- Muon Isolation
- Missing ET
- ...

L0Global



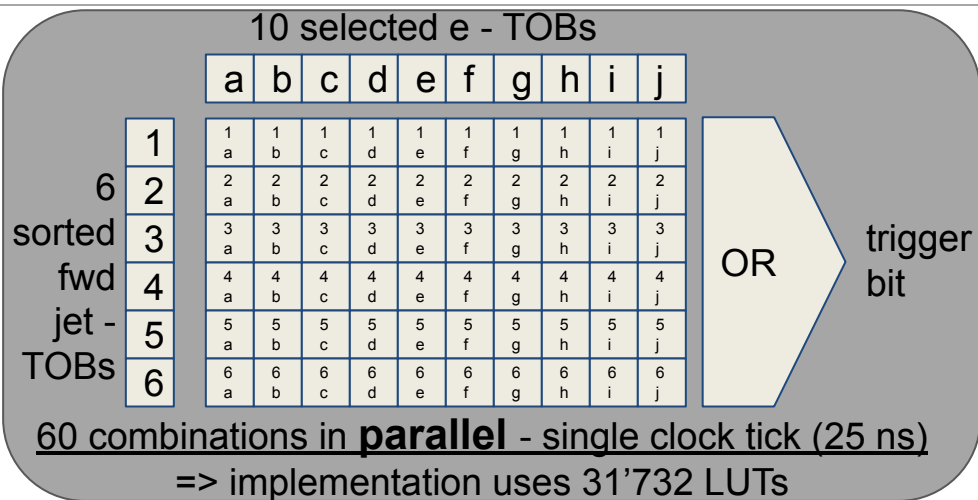
## L0Global ≠ L1Topo:

- Variety of algorithms running on L0Global
- Data moves serially through L0Global
- Long time until next event
- Tight resource budget: **100k LUTs** allocated for topological part (3.3M LUTs on VP1802)

=> Topological algorithms need to adapt



# L0Global - Minimization of Resources

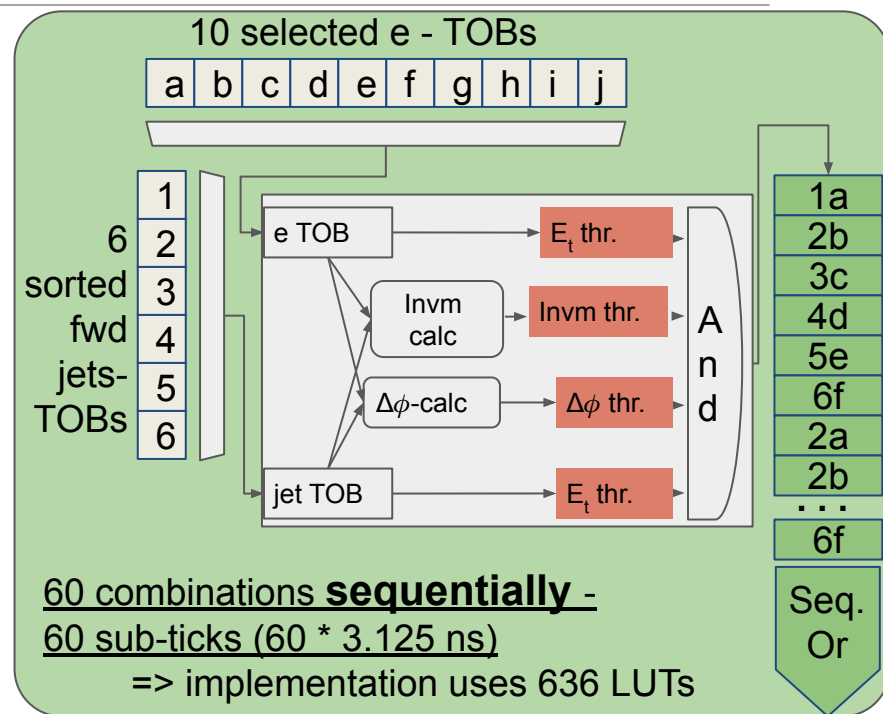


Resource minimization through serialization:

- **trade resource vs. time**
- process one combination per clock tick
- requires additional logic to provide all combinations

**For this example algorithm serialization reduces resource costs from 31'732 to 636 LUTs**

- 95 % already serialized - fits into 100k budget



# Conclusion

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- Low  $p_t$  physics data taking benefits from Topological Trigger immensely
- Run 3 Topo system was installed and is nearly fully commissioned
- First physics results from Run 3 show excellent performance!
- Run 4: Completely different boundary conditions for topological firmware
  - Serialized topological algorithms fit into 100k LUT budget