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The ATLAS Level-1 Topological Processor: Phase-I upgrade and Phase-II adaptation

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The instantaneous luminosity of the LHC in Run 3 is increased up to 3x10^34 cm^-2s^-1, bringing the need for the upgrade of the ATLAS detector, including the trigger system.

The new Phase-I L1Topo system, which replaces its Phase-0 predecessor, processes data from the jet, electromagnetic, and global Feature Extractors and the upgraded Muon to Central Trigger Processor Interface to perform topological and multiplicity triggers. The L1Topo system consists of three modules, each hosting two processor FPGAs (Xilinx Ultrascale+ 9P). High-speed optical transceiver modules are used for the modules' real-time data path to support data transmission at speeds up to 11.2 Gb/s per link.

The L1Topo firmware is composed of a large number of sort/select, decision, and multiplicity algorithms, that are automatically assembled and configured based on the provided trigger menu.

The fully synchronous, very low latency, parallel implementation of the Phase-I Topological firmware is inadequate for the new Phase-II operational environment, where a significantly higher latency budget with a substantially tighter resource budget is available. Therefore, all the developed algorithms, including the automatic menu-based firmware assembly functionality, are being adapted for use within the Global Trigger System, coming into play after the Phase-II upgrade of the ATLAS detector.

A detailed overview of the Phase-I L1Topo hardware and firmware will be provided. Phase-II related firmware adaptations will also be discussed.

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