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Cape Town, South Africa

Prototype validation for the CMS Inner Tracker Phase II upgrade

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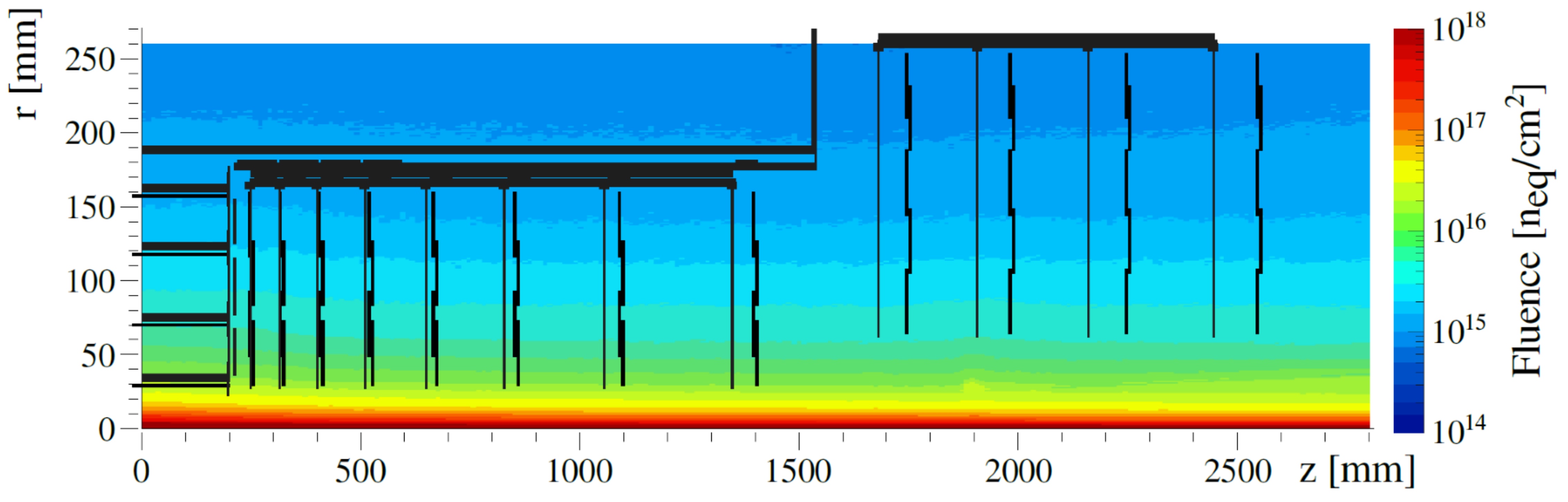
on behalf of the **Tracker group of the CMS Collaboration**

[a] INFN Torino *(Italy)* [b] CERN *(Switzerland)*

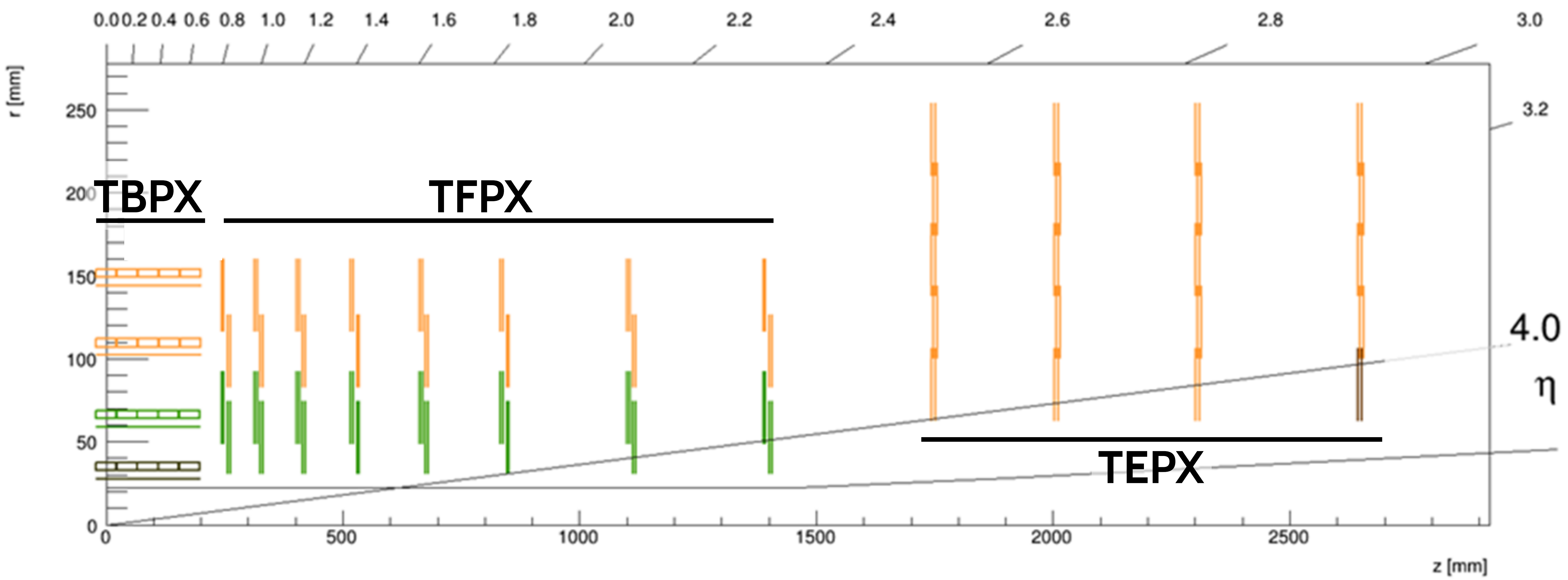
Inner Tracker of the CMS experiment will be fully replaced during the Phase 2 upgrade
to cope with the increased radiation levels and collision rates of the HL-LHC



Upgraded tracker will operate under harsh conditions:

- average 200 pp collisions/event every 25 ns
- up to 1.9×10^{16} n_{eq}/cm^2 fluence ▶
  and Total Ionising Dose (TID) of ~1 Grad

Substantially extended coverage in the forward region
from η ≤ 3.0 → **η ≤ 4.0**



2x2 modules (**planar** sensor)

1x2 modules (**planar** sensor)

1x2 modules (**3D** sensor)

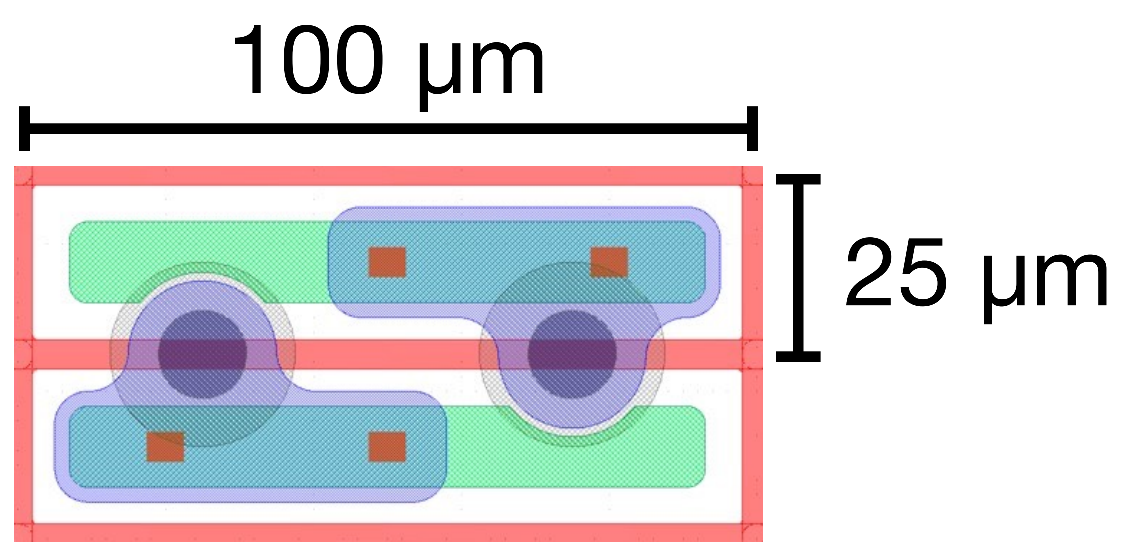
↳ higher radiation tolerance
+ better thermal performance

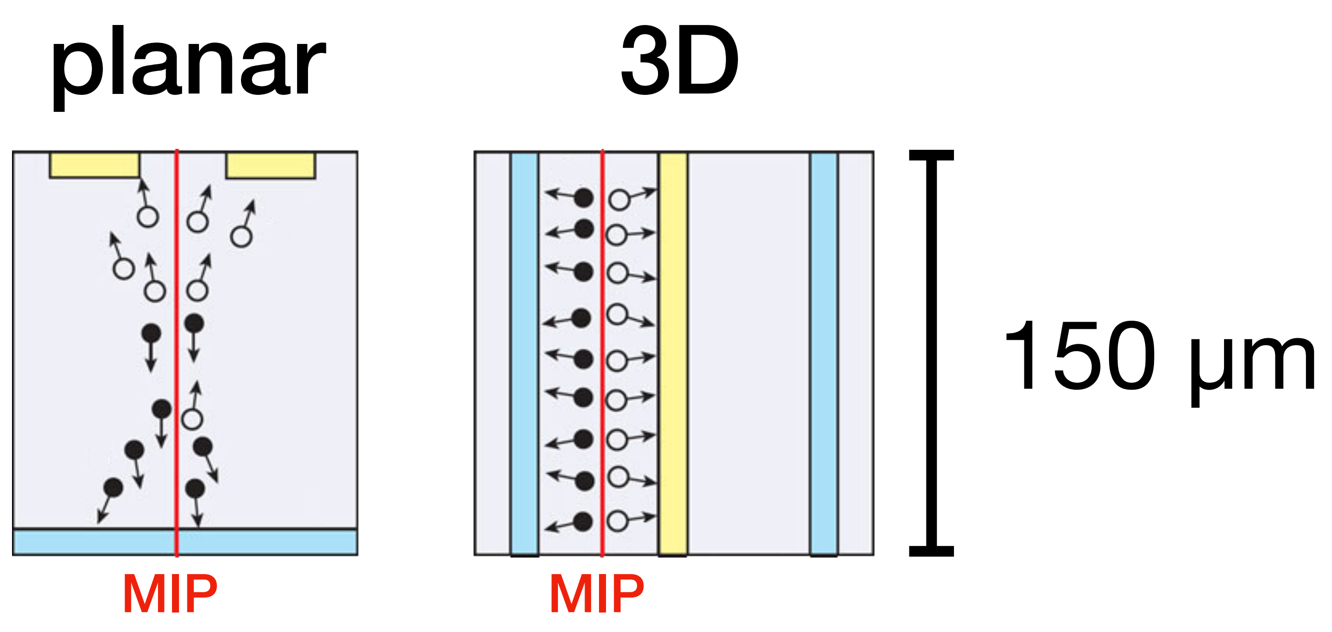
A complete Inner Tracker comprises of several core components: sensors, readout chips, mechanics

↳ each has to be validated at different stages of design, production and assembly

Sensor

- spatial resolution, efficiency
- radiation tolerance





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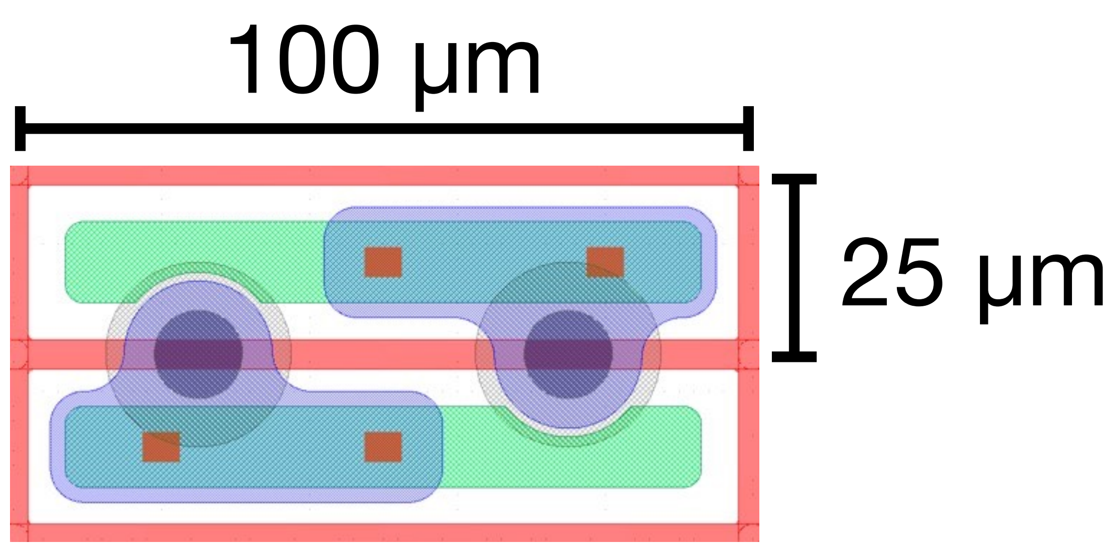
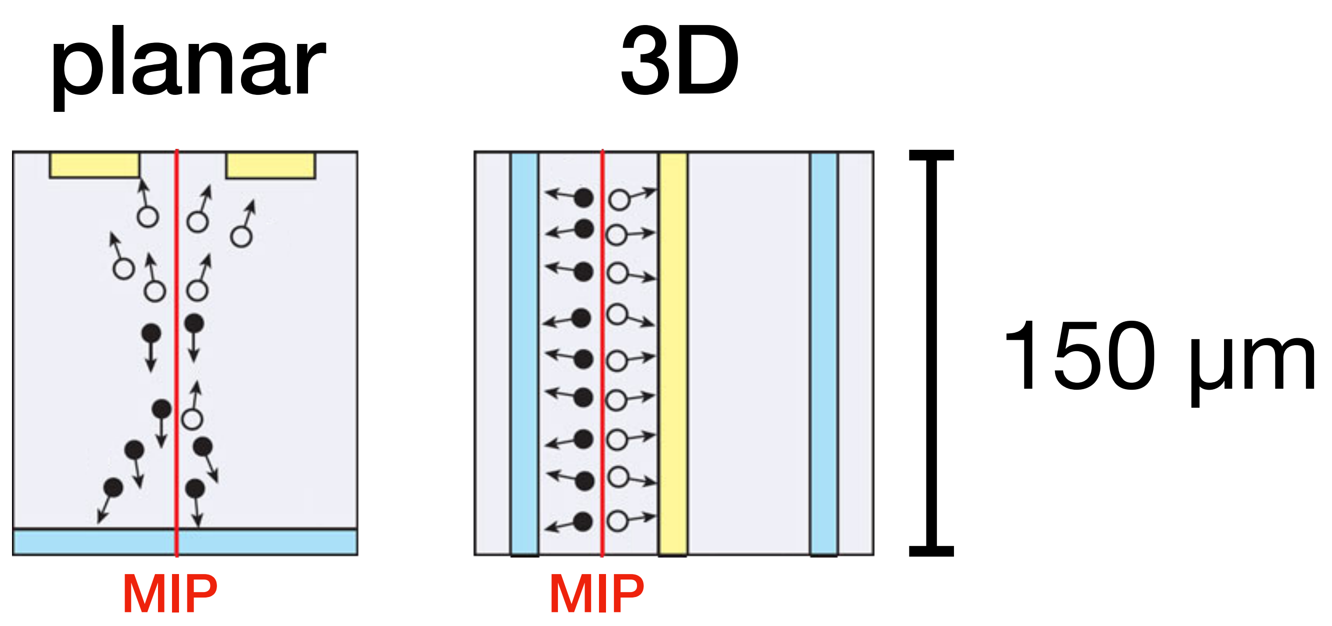
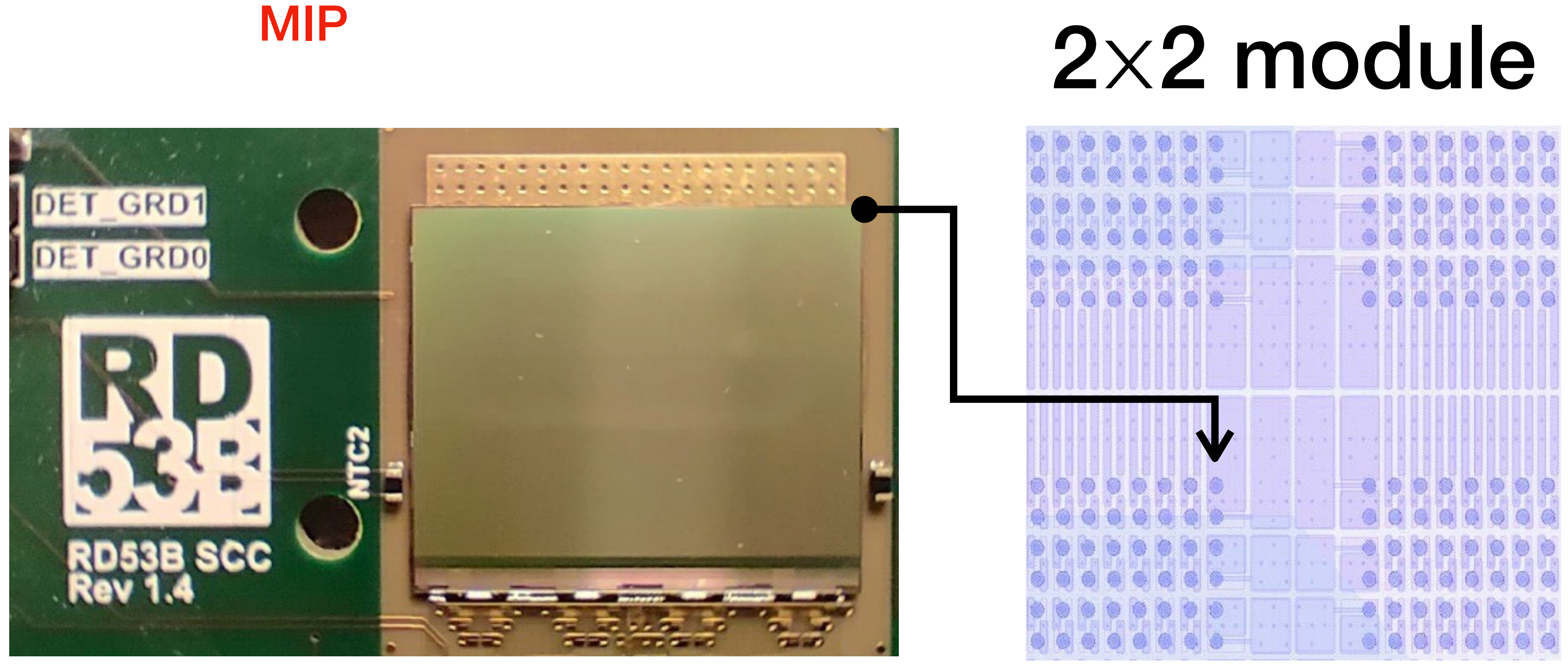




Readout chip → CROC - variation of RD53A design for CMS

- powering, noise, communication, cross-talk
- radiation tolerance



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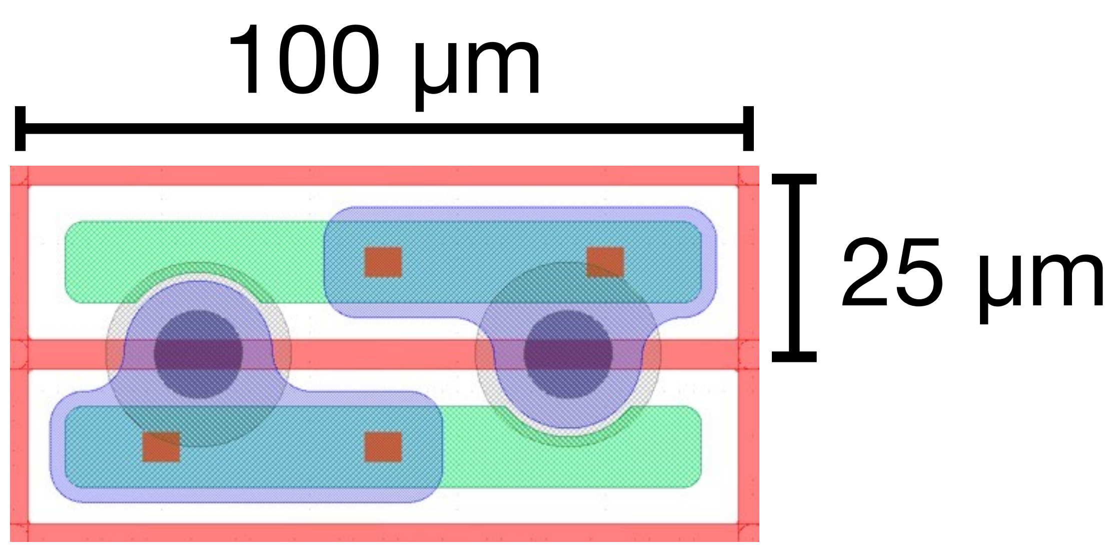

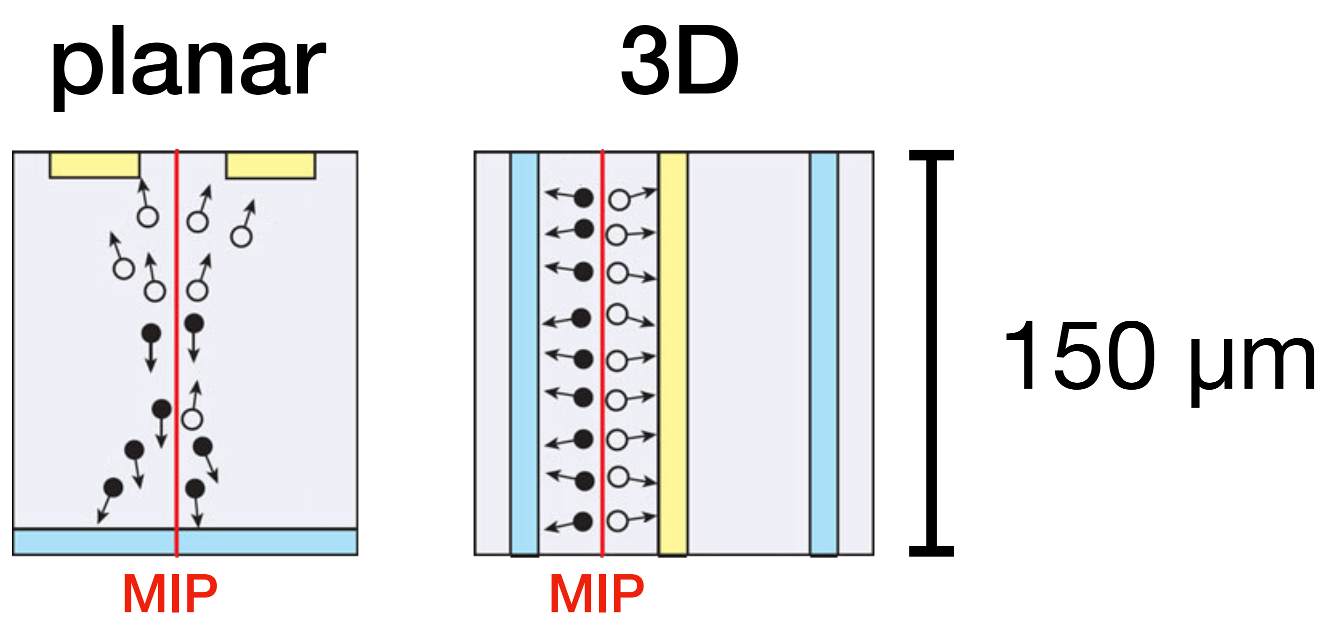

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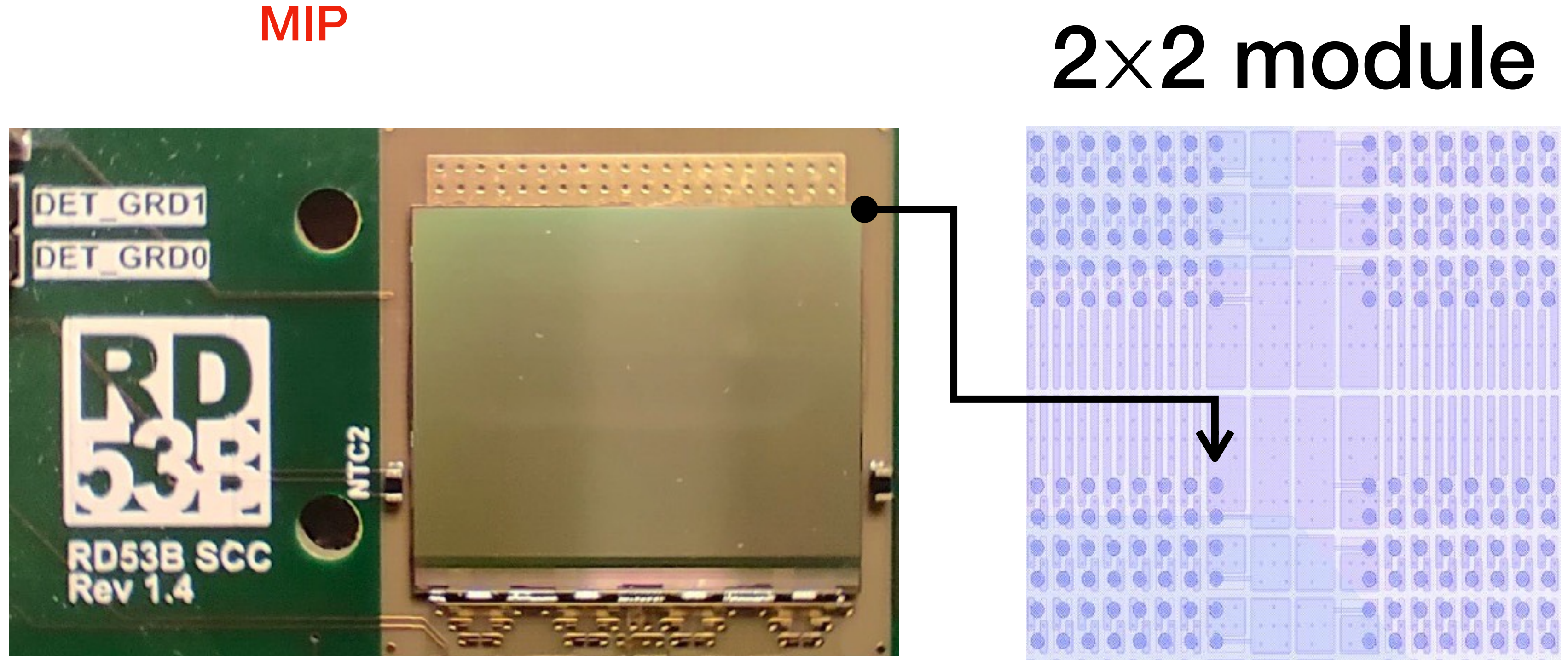
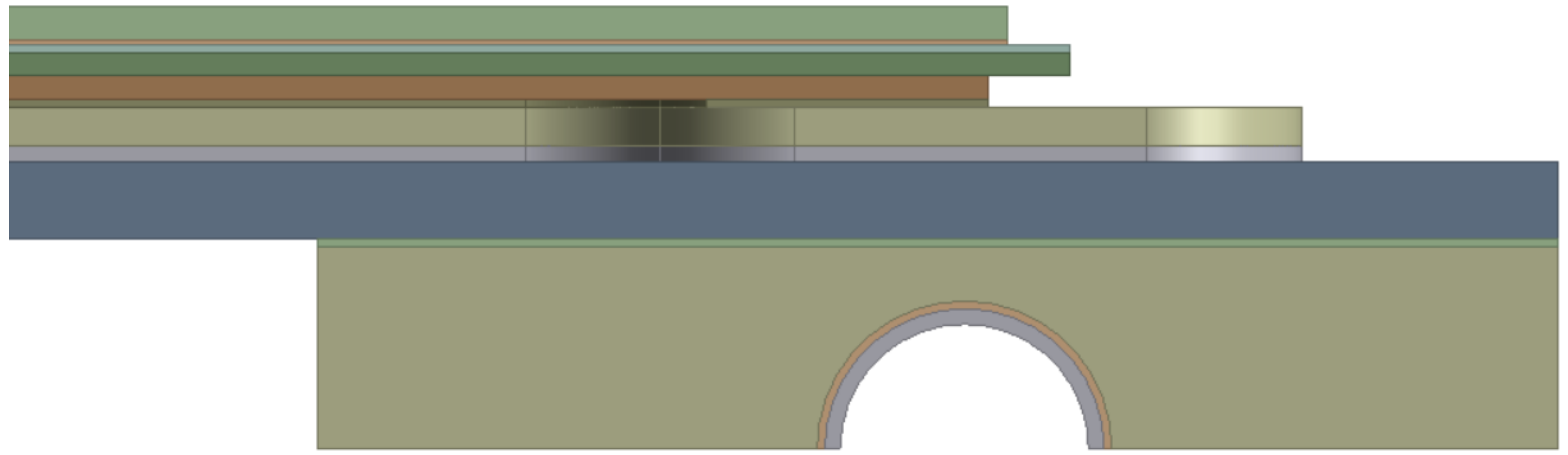


Module assembly

- hybridisation, wire-bonding
- mechanical qualities
- cooling performance

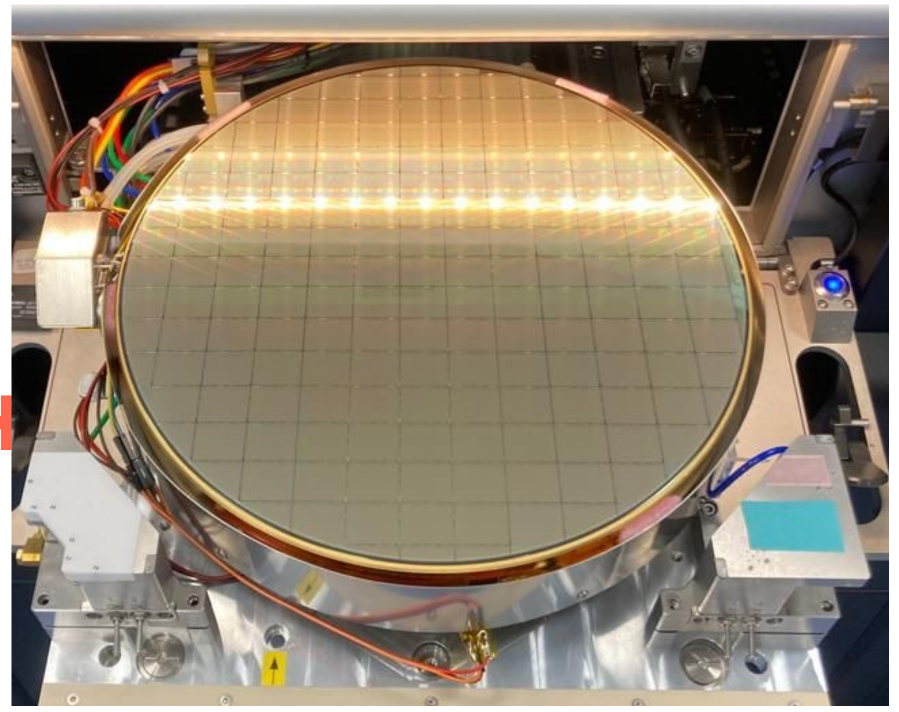


CROC readout chips arrive from the vendor as Si wafers: 138 chips/wafer

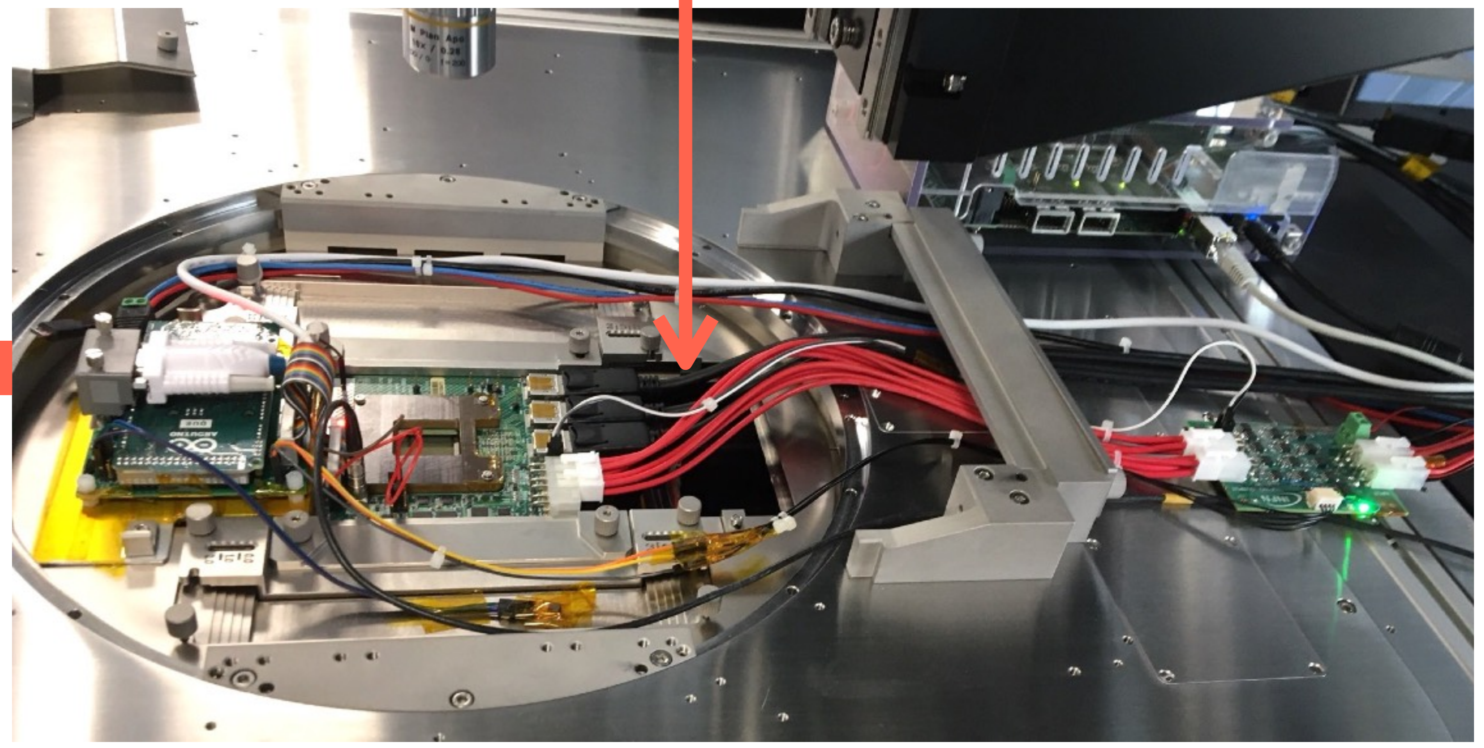
↳ very complex manufacturing process → a fraction of chips expected to have defects

All relevant functionality of each chip tested directly on the wafer on two sites: INFN Torino + KSU

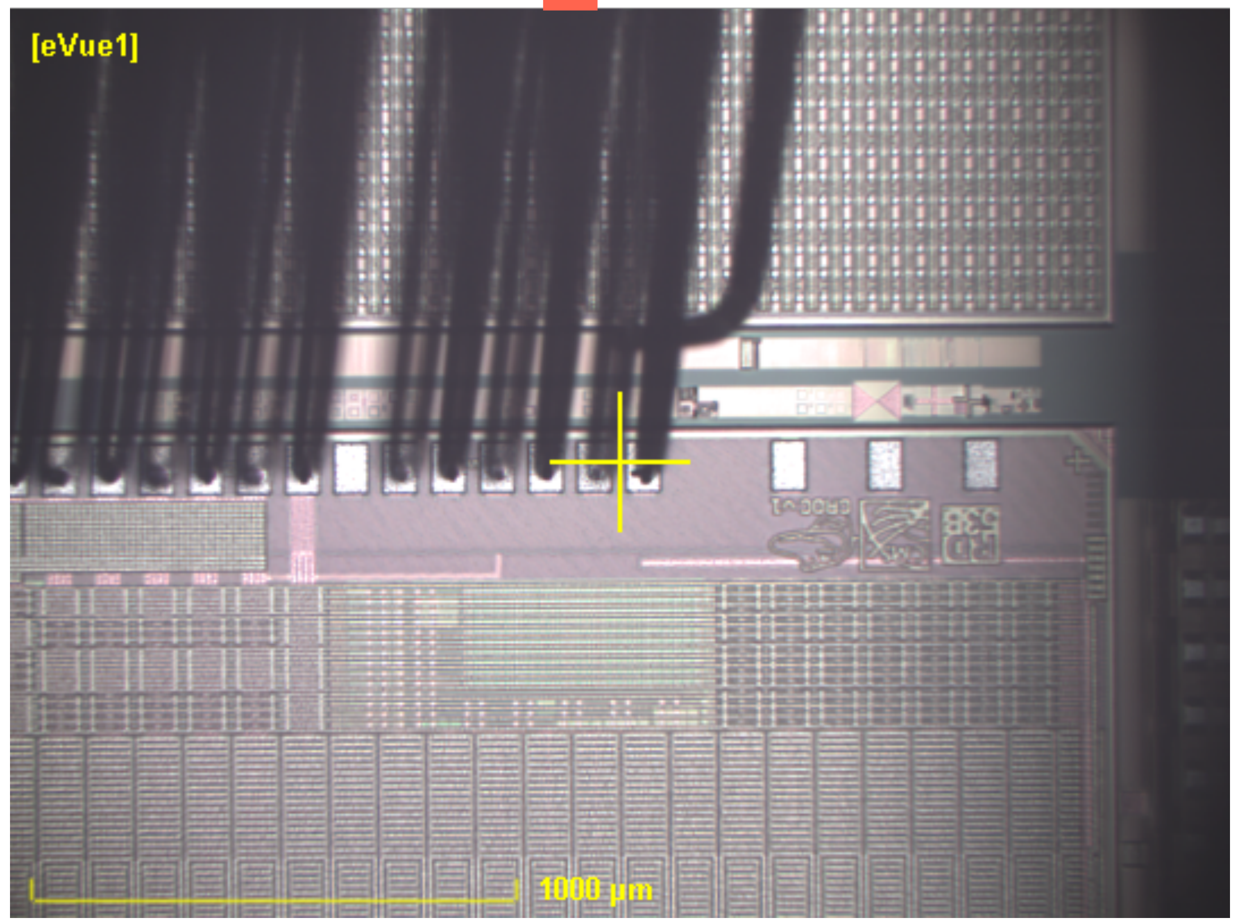
Probing station
semi-automated



Loaded wafer
non-thermal chuck



Probing card
- power board
- controller auxilliar board
  interfaced via Arduino Due
- PC with DAQ + UI
- power supplies, source meters, etc.



Probing needles
in contact with pads of the chip

Wafer-level CROC testing: tests

An extensive series of Wafer Level Tests (WLT) executed for every chip:

- powering schemes, power consumption, I-V curves
- chip configuration, communication, data transfer
- threshold tuning, analog/digital front-end readout
- ADC/DAC and temperature sensor calibrations

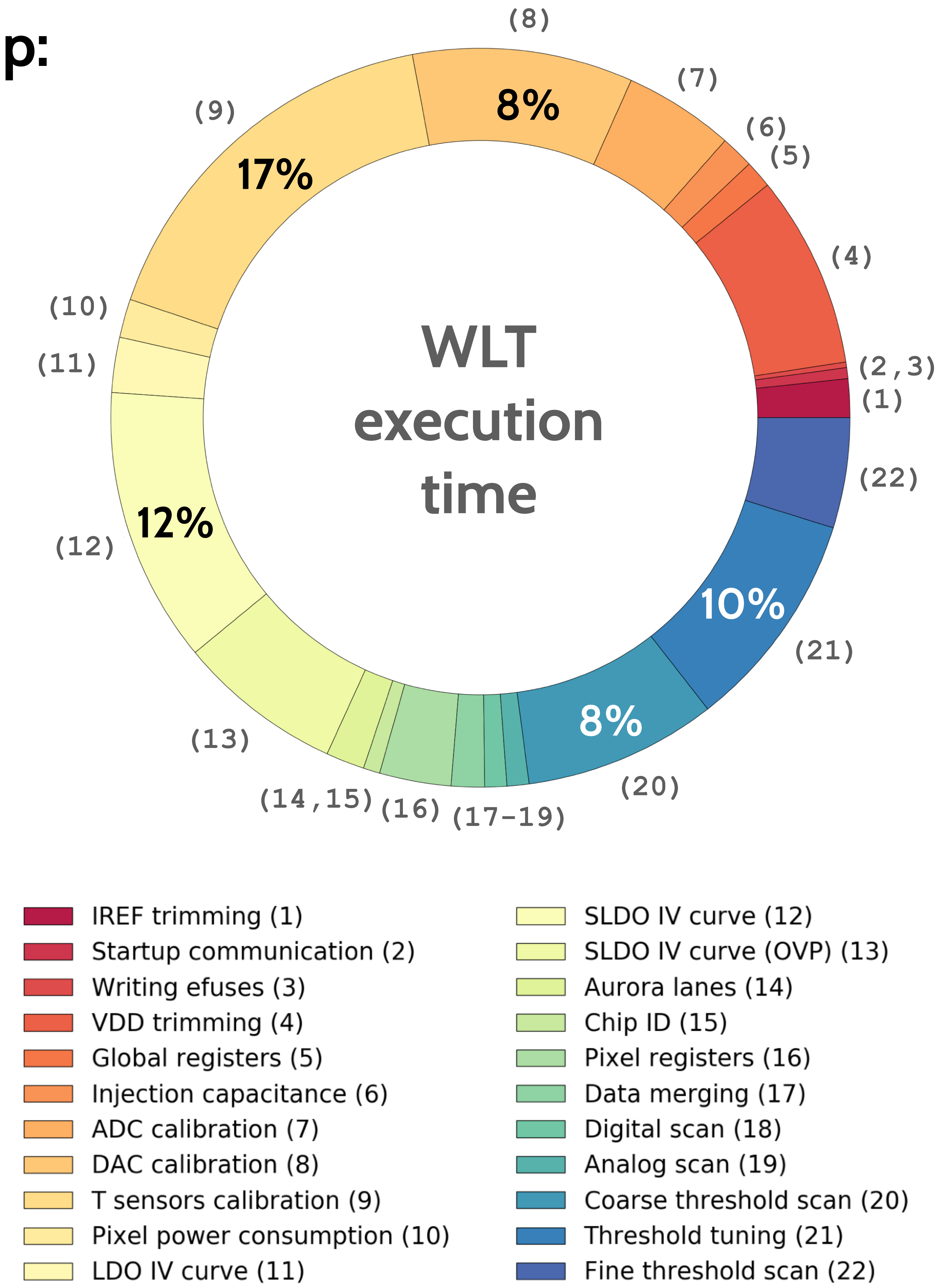
Execution time optimised to test 1 wafer/day → ~8 min. / chip

↳ crucial for daily wafer validation during large-scale production

Just a few tests take most of the time:

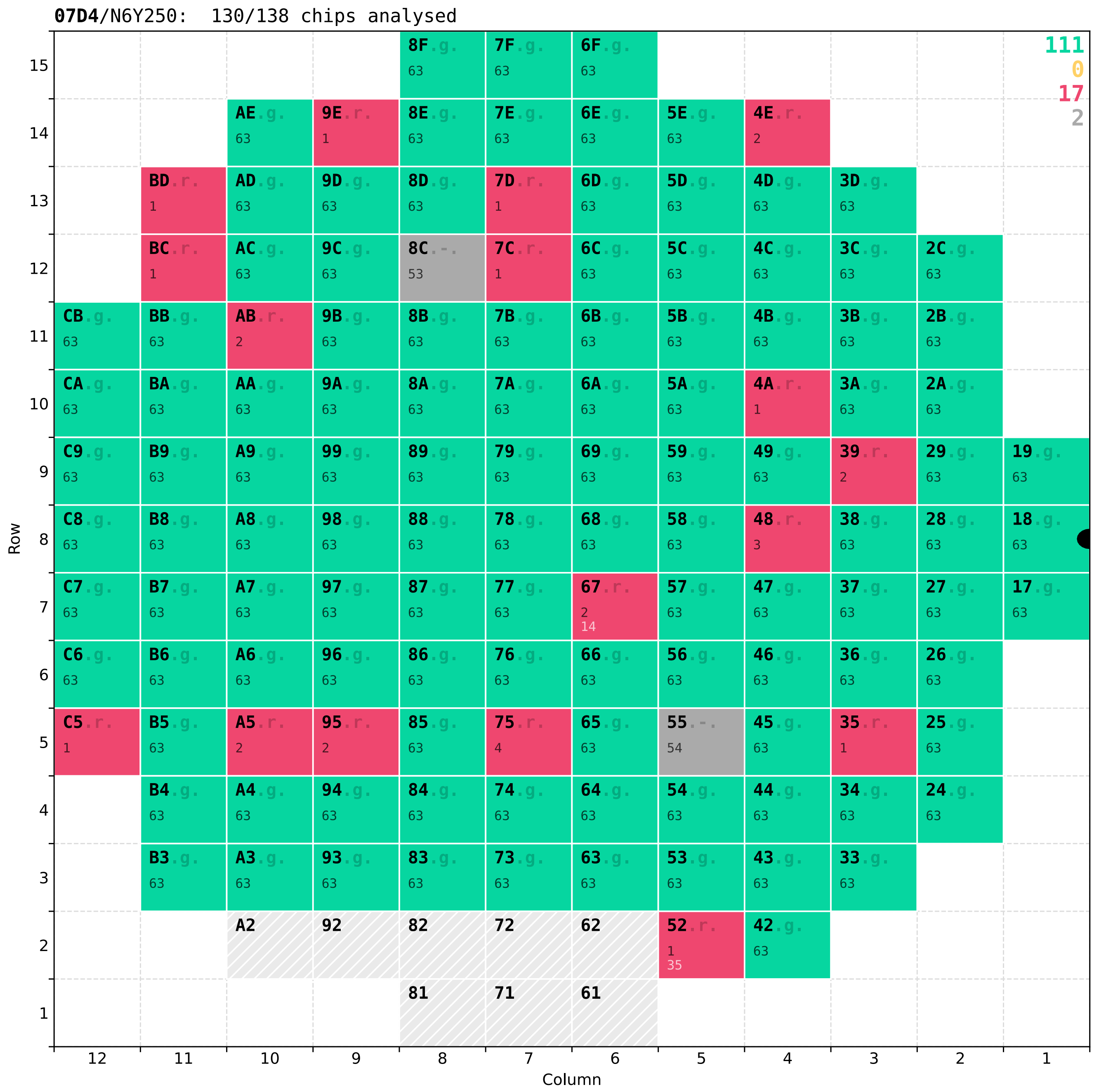
- tuning of pixel thresholds [8% + 10%]
- calibration of T sensors [17%]
- measurement of I-V curves in SLDO powering mode [12%] ↱ Shunt Low Drop-Out
- calibration of DACs [8%]

Several tests are still to be added, but there is enough time margin



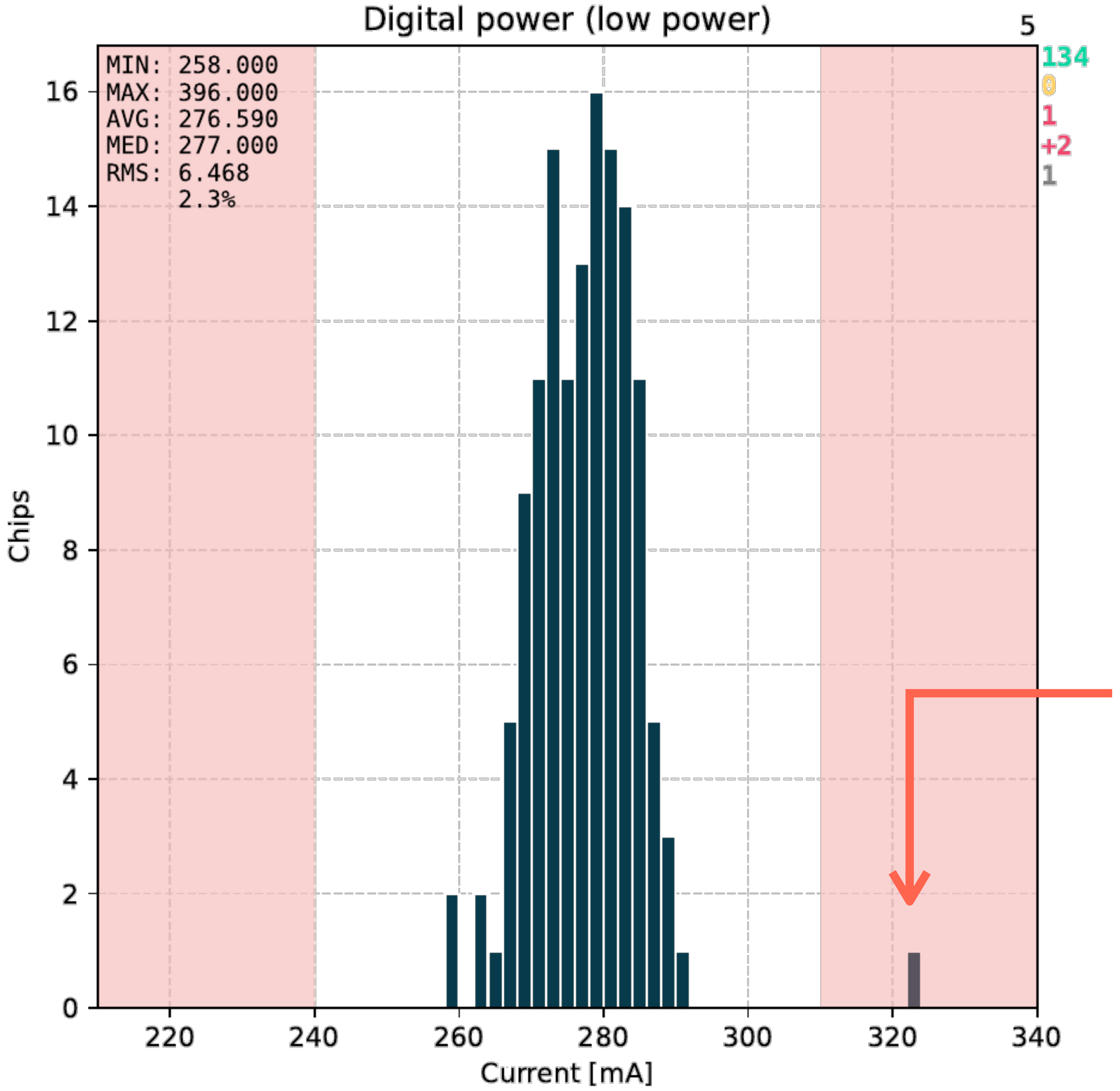
Wafer-level CROC testing: results

Data from each test and each chip processed using automated analysis procedure



Wafer map

used for selection of good chips during wafer dicing



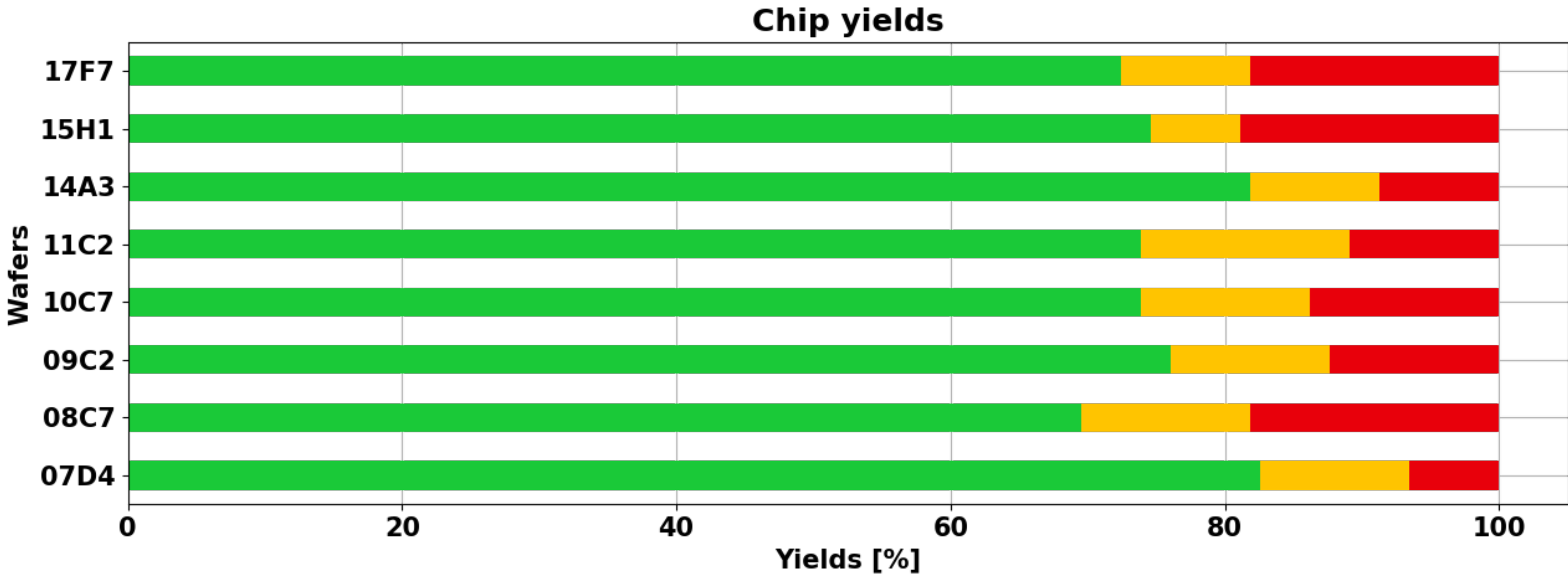
Test output

shows distribution of the measured quantity

- 1 entry/chip
- ≥1 histogram/test

Bad quality chip
↳ discarded

Average yield of good chips: 73% among 8 tested wafers



Part of the yellow chips are kept for internal use

↳ some production-critical functionality is broken, but can still be useful in laboratory

Wafer-level CROC testing: book-keeping

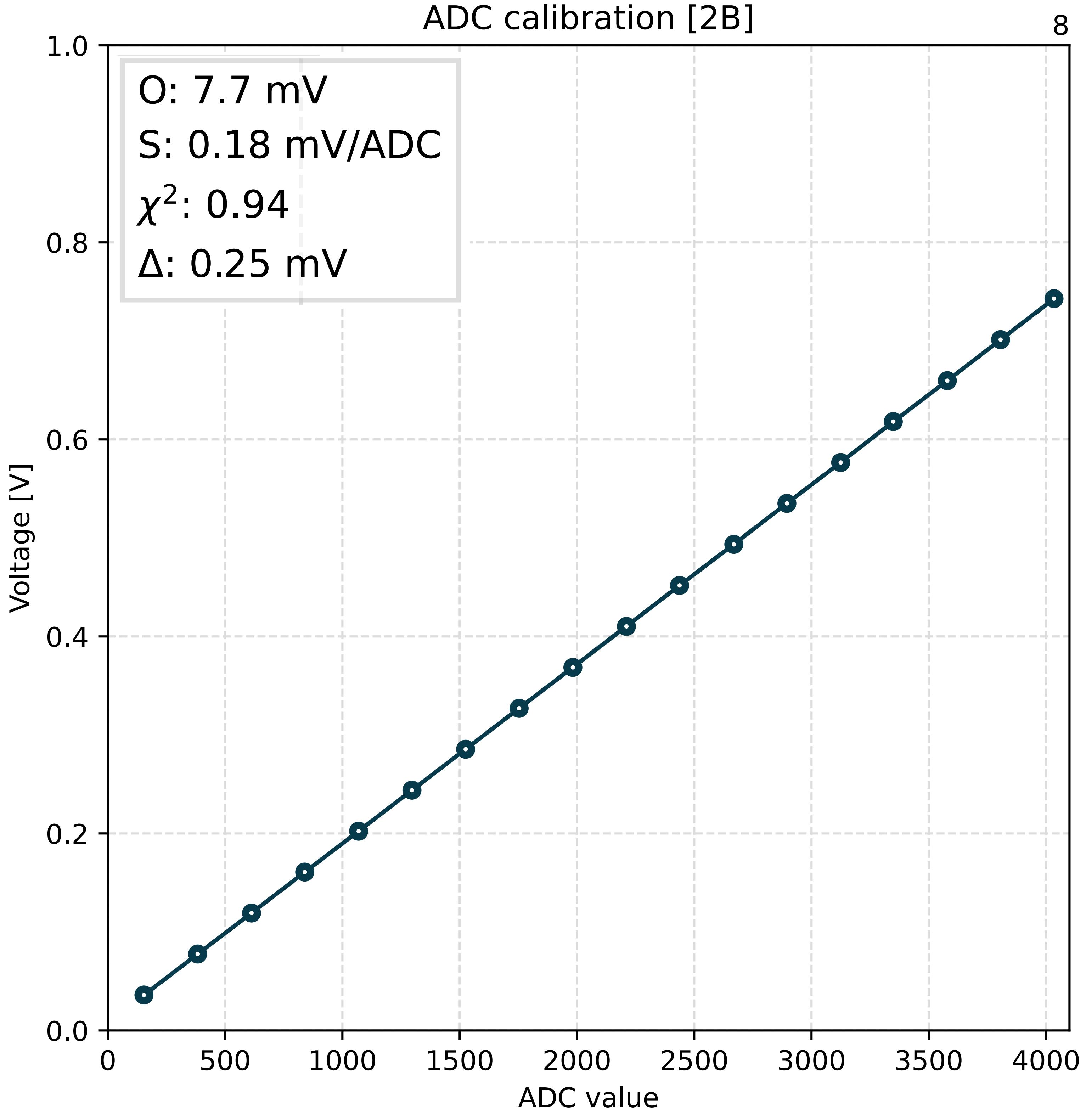
Extensive list of measured values stored in the Detector Construction Assembly database (DCA)

↳ necessary for module assembly and future detector operation

Examples of the stored values:

- **final chip quality** (green / yellow / red)
  ↳ used during selection of good chips for module assembly
- **IREF trim-bit value**
  ↳ defines physical pads on the chip to be wire-bonded
- **T-sensor calibration coefficients**
  ↳ used during detector operation for the local T measurement

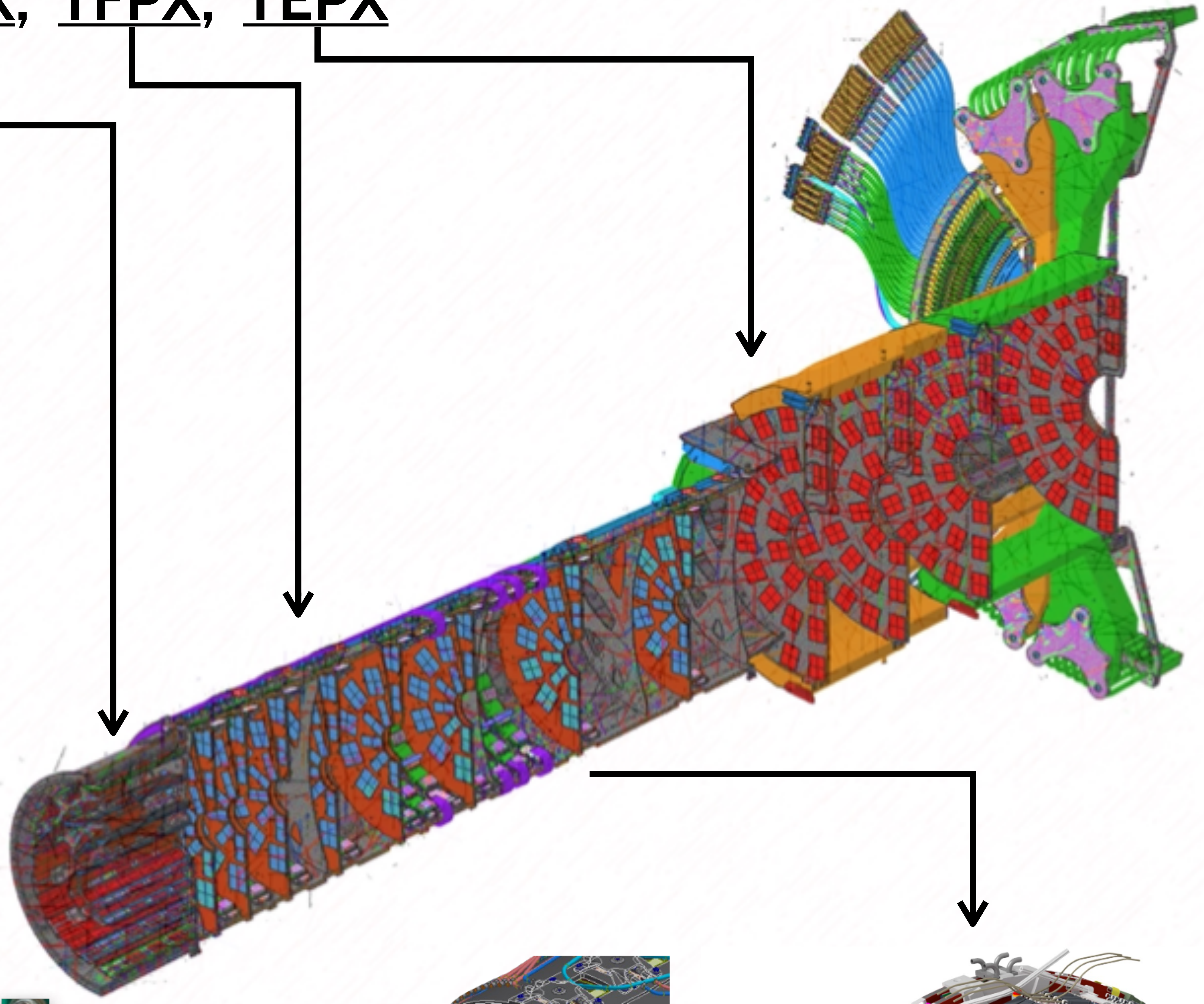
\+ **relevant book-keeping information**
chip/wafer serial numbers, test configurations, quality criteria, etc.



Some quality criteria determined empirically from the tested wafers

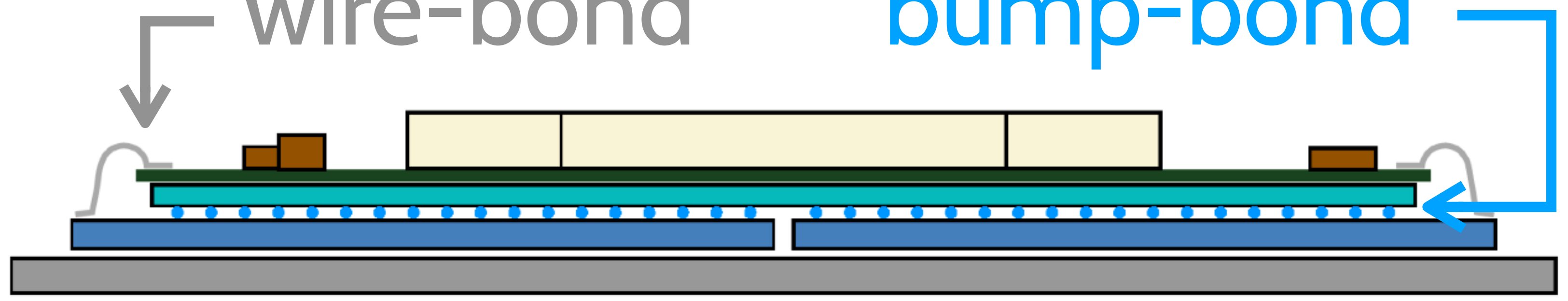
↳ evolution of distributions from wafer to wafers is monitored to keep yields as high as possible

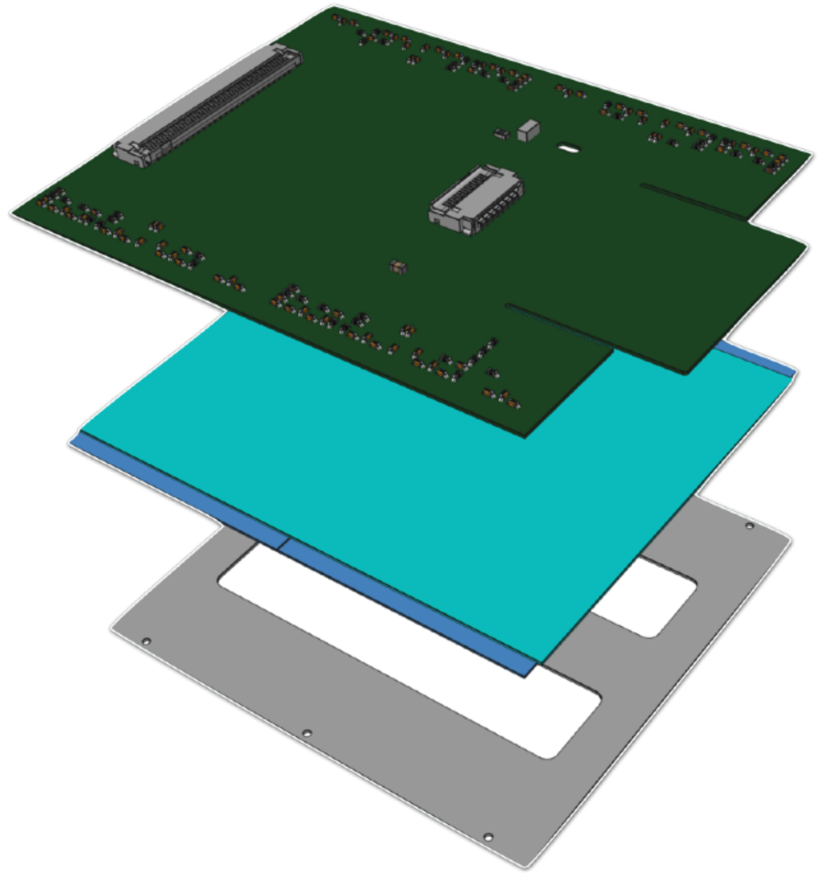
Inner Tracker will comprise of three separate partitions: TBPX, TFPX, TEPX
each having a different mechanical structure



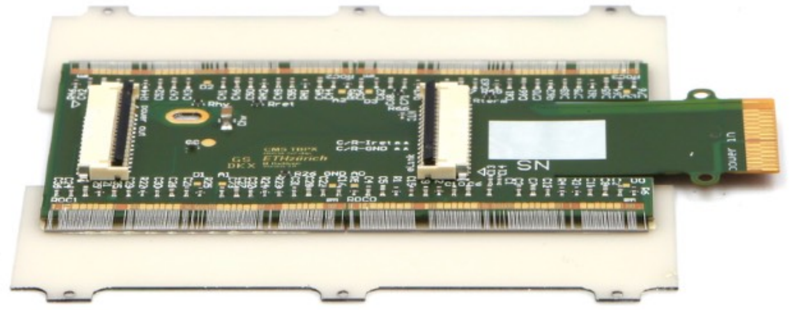
Conceptually the same module assembly in each partition

- HDI (High Density Interconnect)
- ROC + sensor assembly
- Si_3N_4 cooling plate (TBPX only)

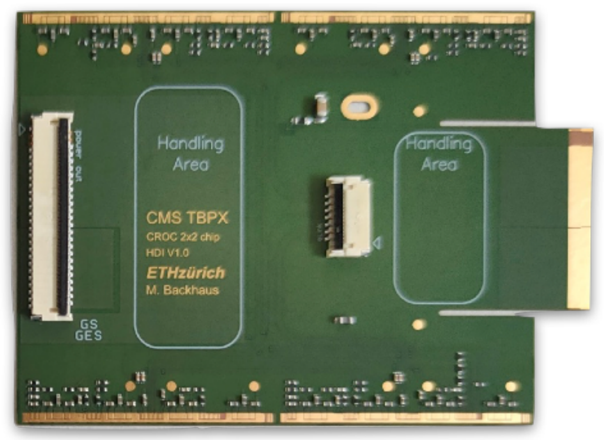




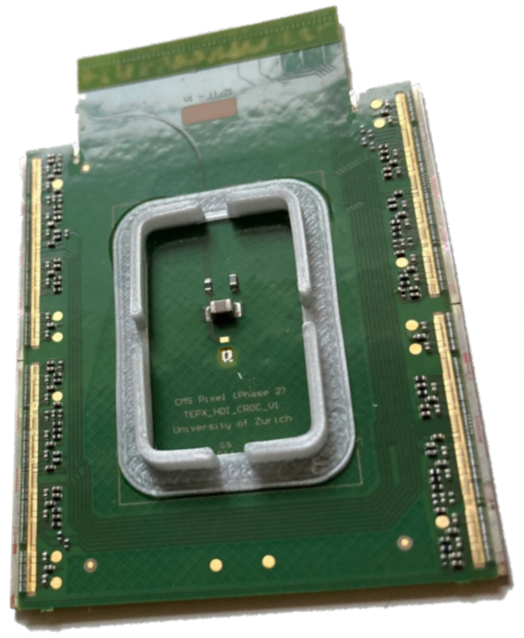
Multiple specific module designs of each type



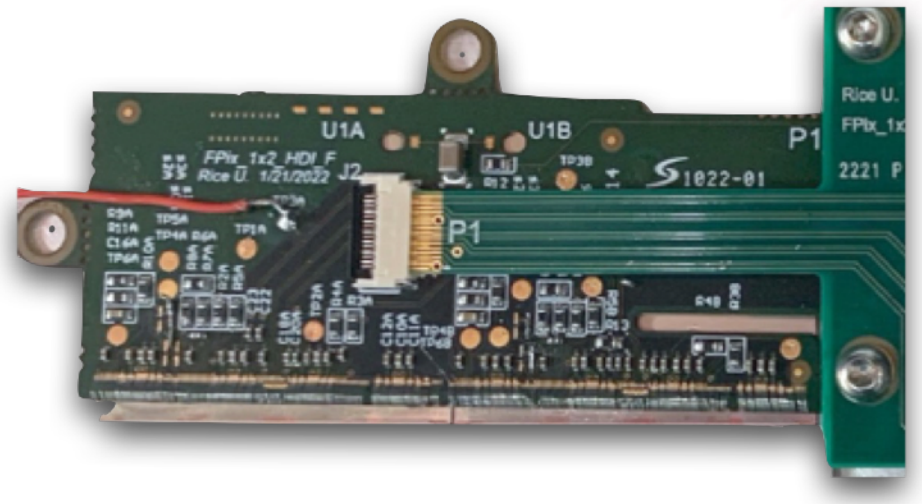
TBPX: 1x2



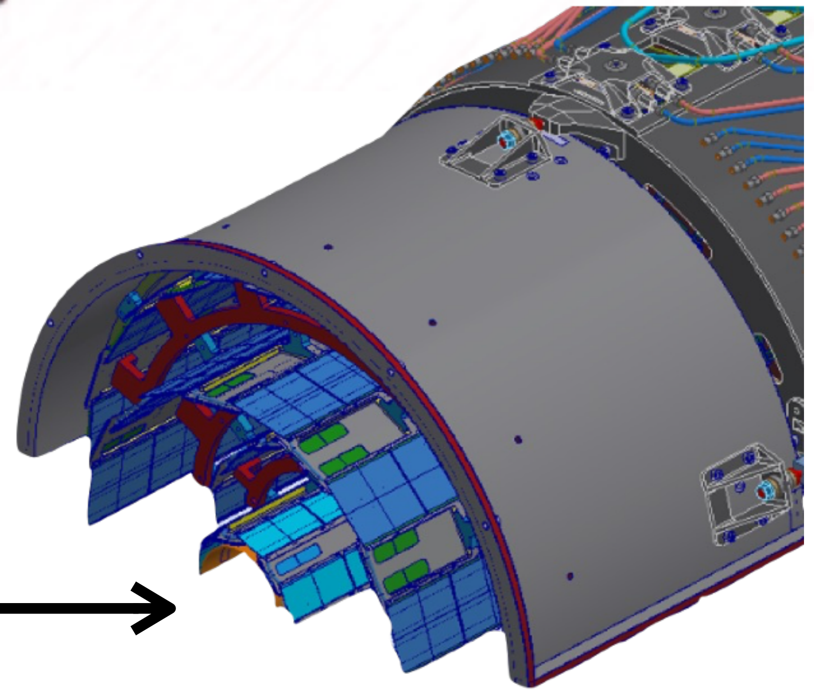
TBPX: 2x2

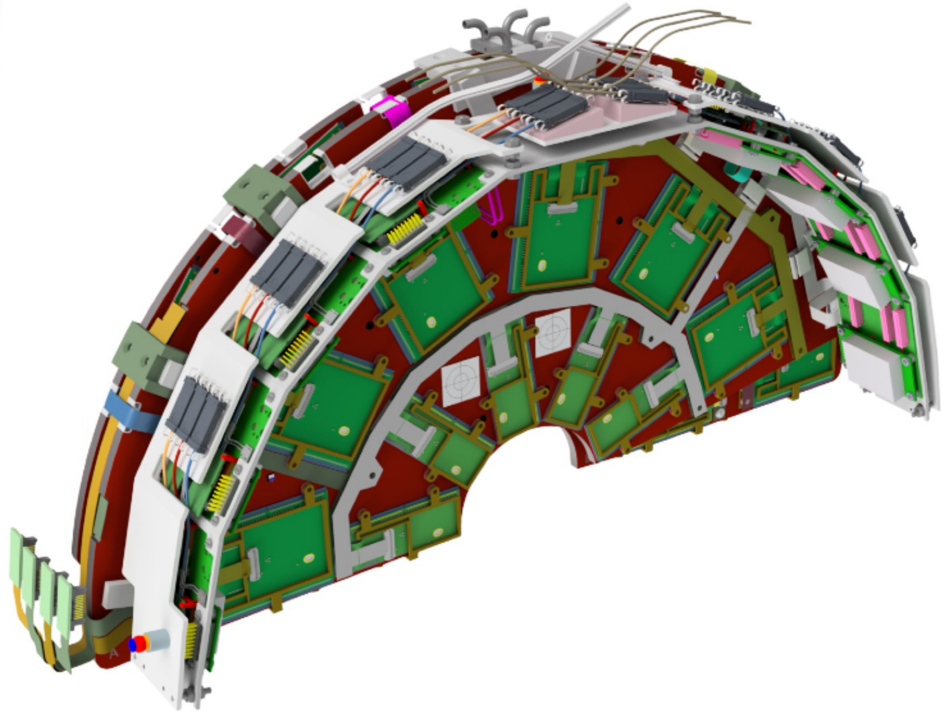


TEPX: 2x2



TFPX: 1x2





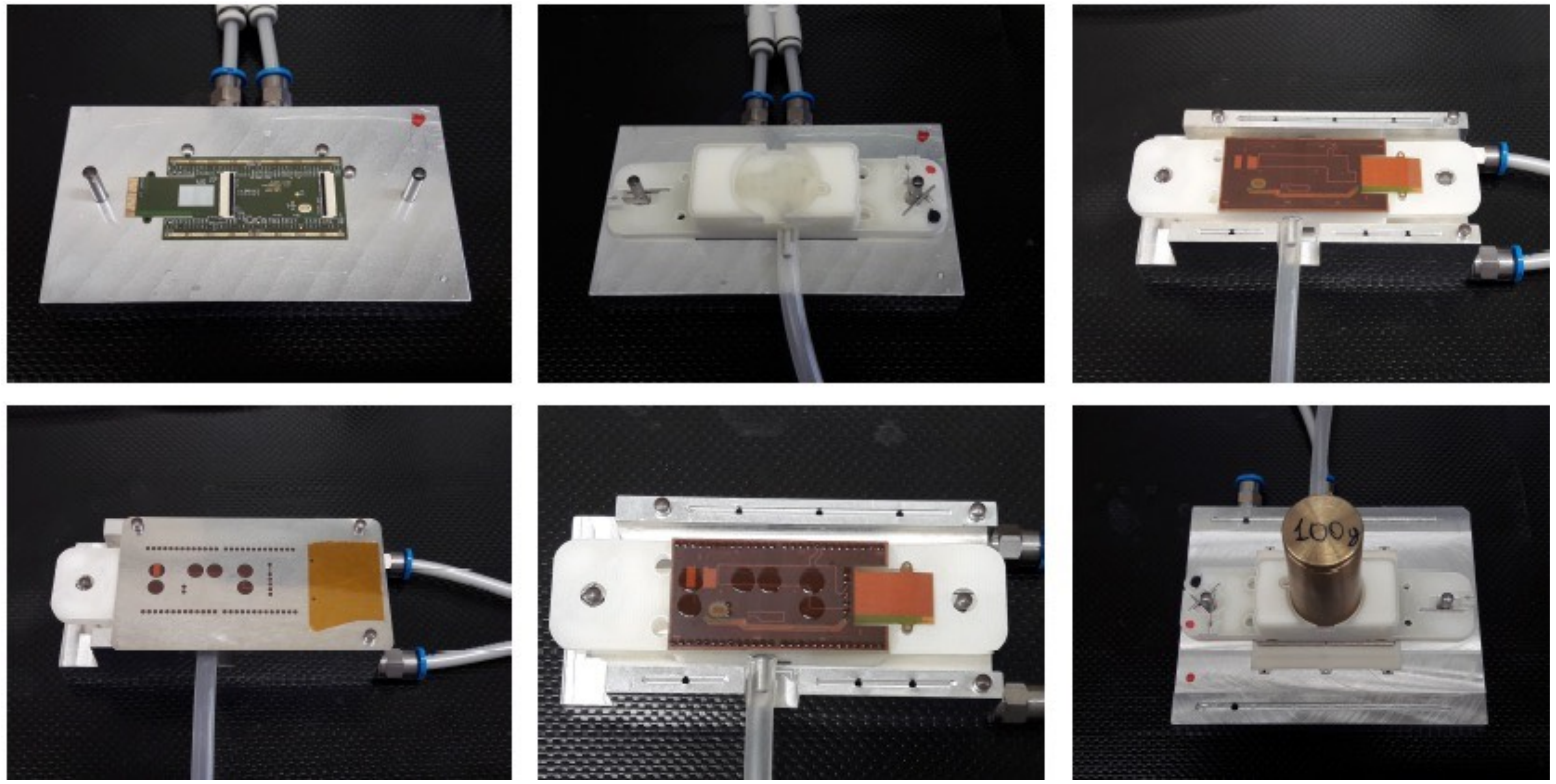
Module assembly: procedures

The two main operations during module assembly: glueing + wire bonding

↳ <u>ROC + sensor</u> arrive already assembled from the bumb-bonding facility

Glueing must be done with very good alignmend for proper wire-bonding

↳ **using high-precision jigs with pins dedicated for each part + stencils for precise glue deposition**



TBPX assembly

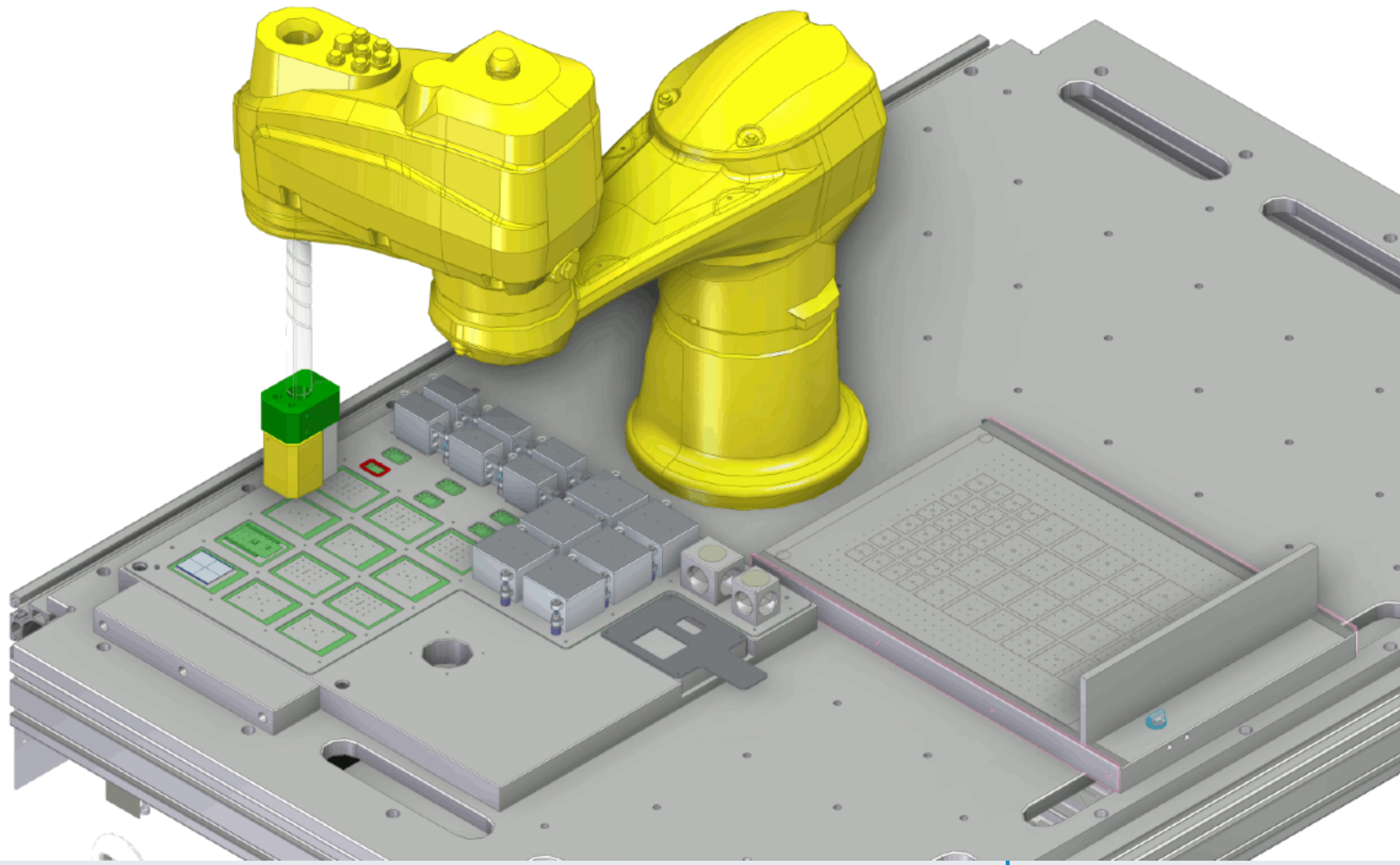
1. **sensor + ROC glued to the cooling plate**
2. **HDI glued on top**
3. **ROC wirebonded to the HDI**

Each step performed manually

↳ easy to parallelise with tool duplication

<u>TEPX assembly</u> is more automated → using a robotic arm ▶

↳ autonomous positioning of parts + glue deposition: ≤60 µm precision



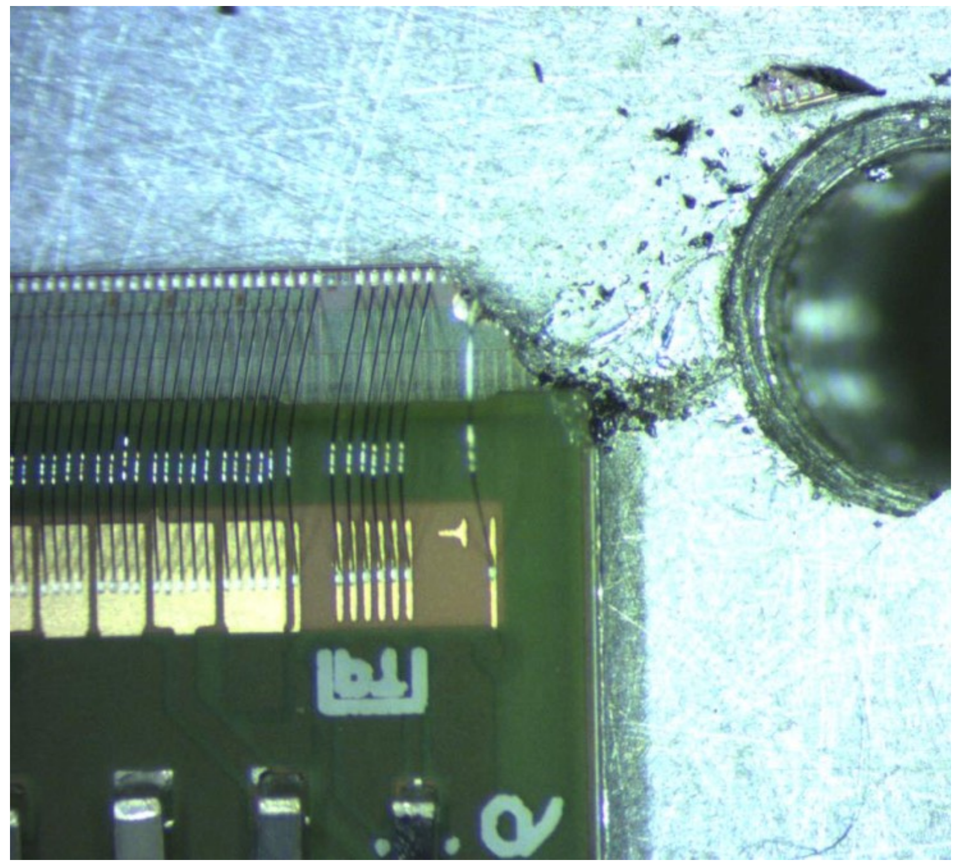
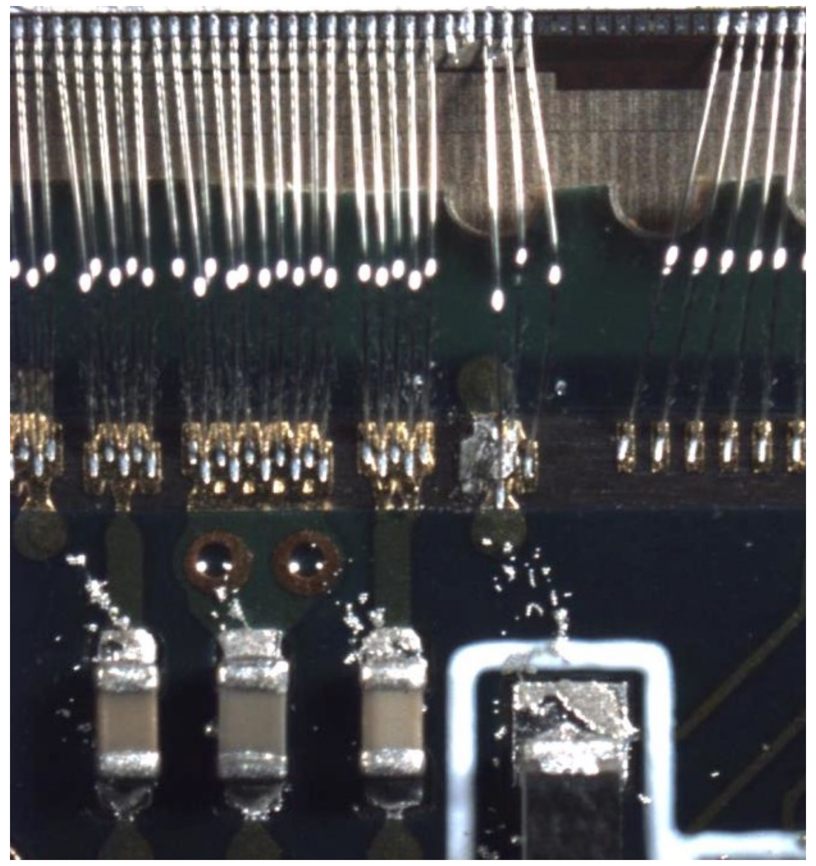
Module assembly: quality control

Assembly quality is assessed in two main stages:

1. Optical inspection

primarily under microscope

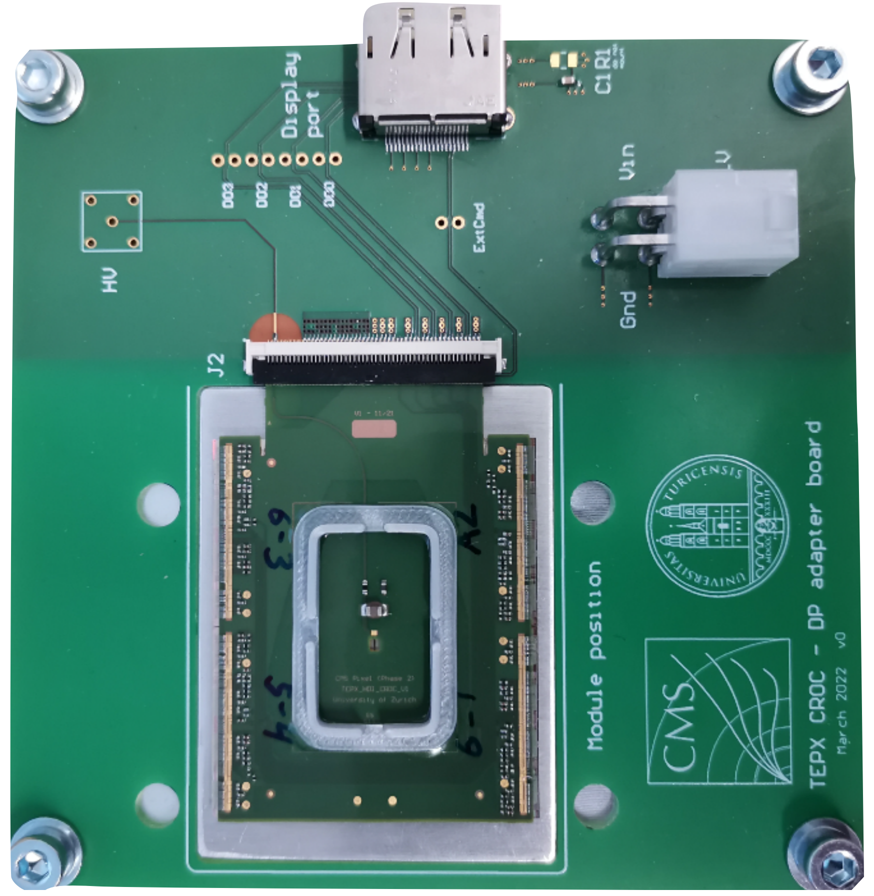
- alignment of parts, soldering quality
- absence of mechanical damage
- quality of wire bonds

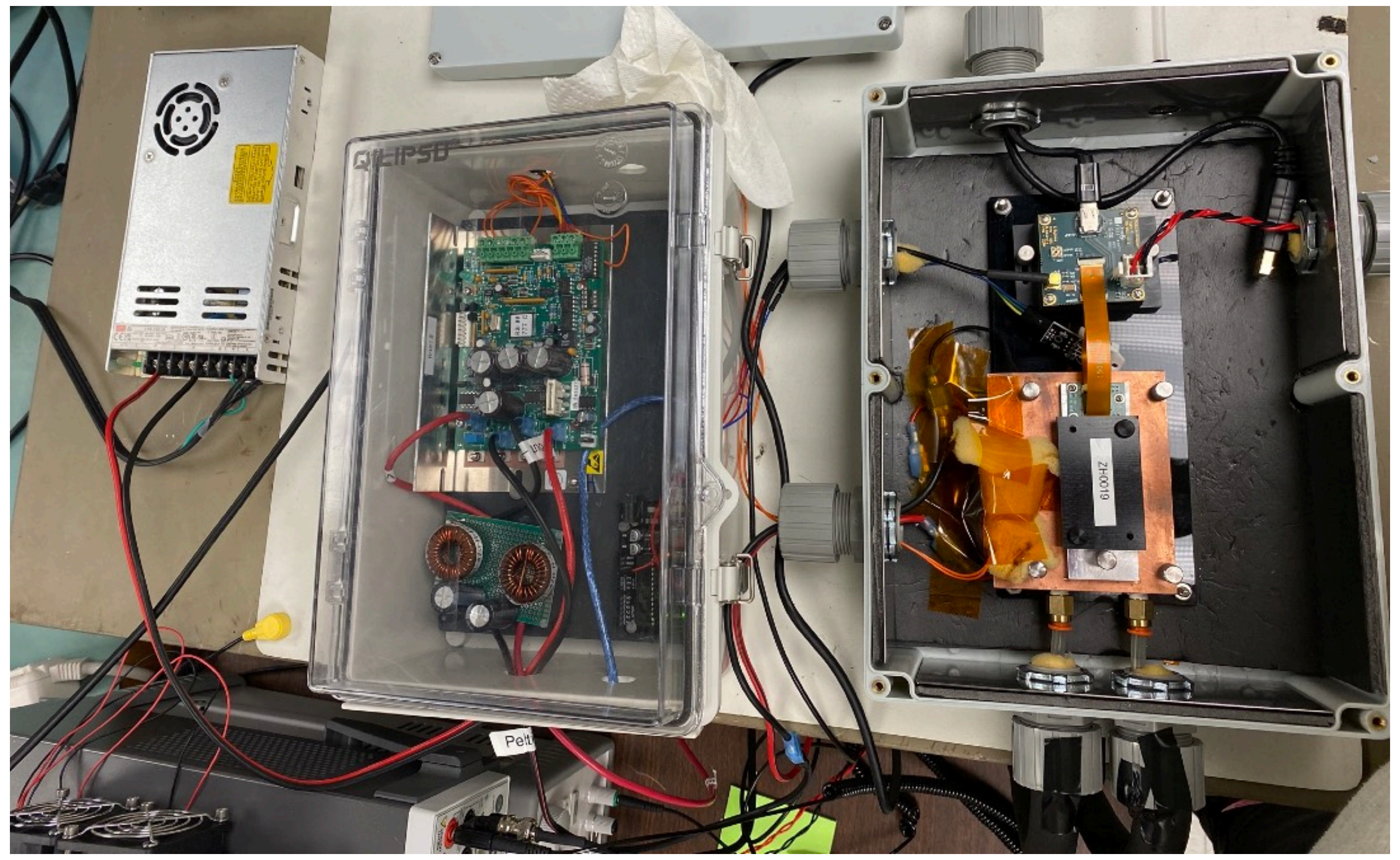



2. Functional tests

primarily using single-module adapters

- bump-bonding defects *(X-ray induced charge)*
- power consumption, communication
- threshold + noise distributions after tuning

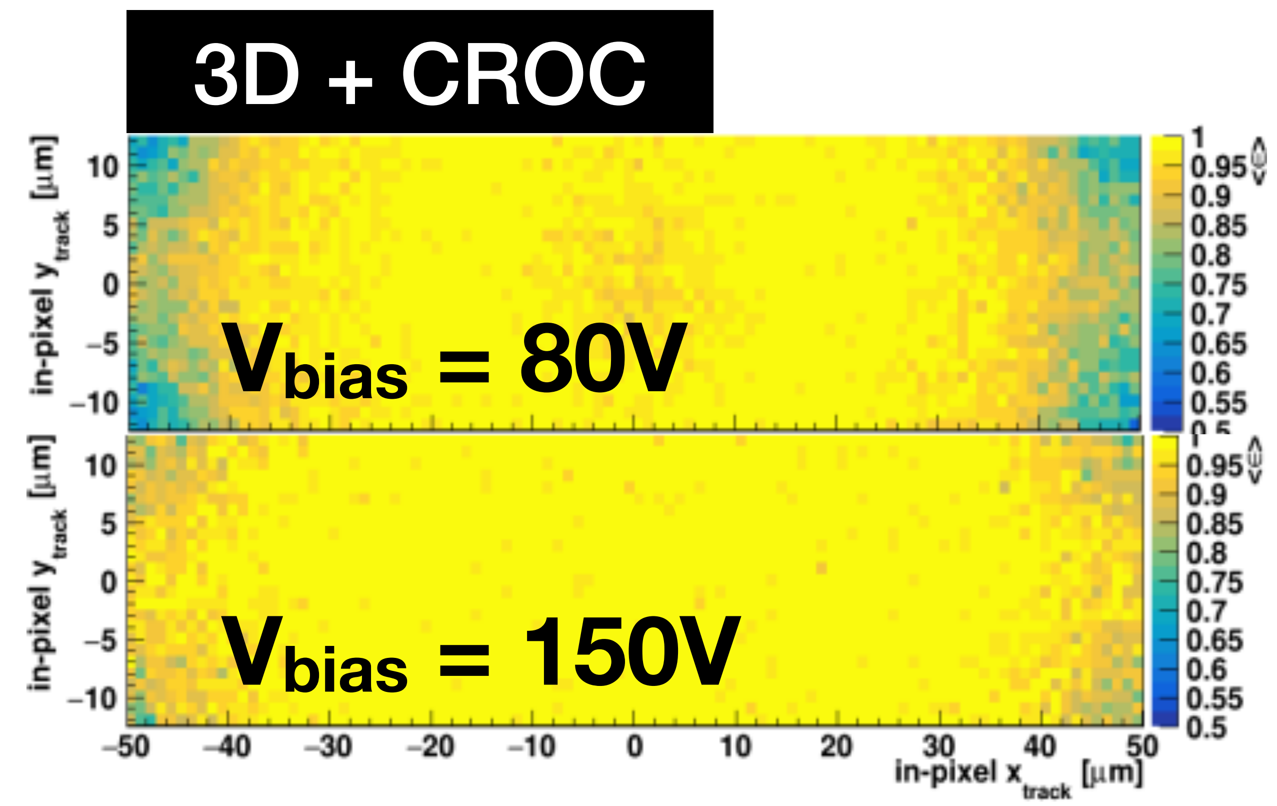


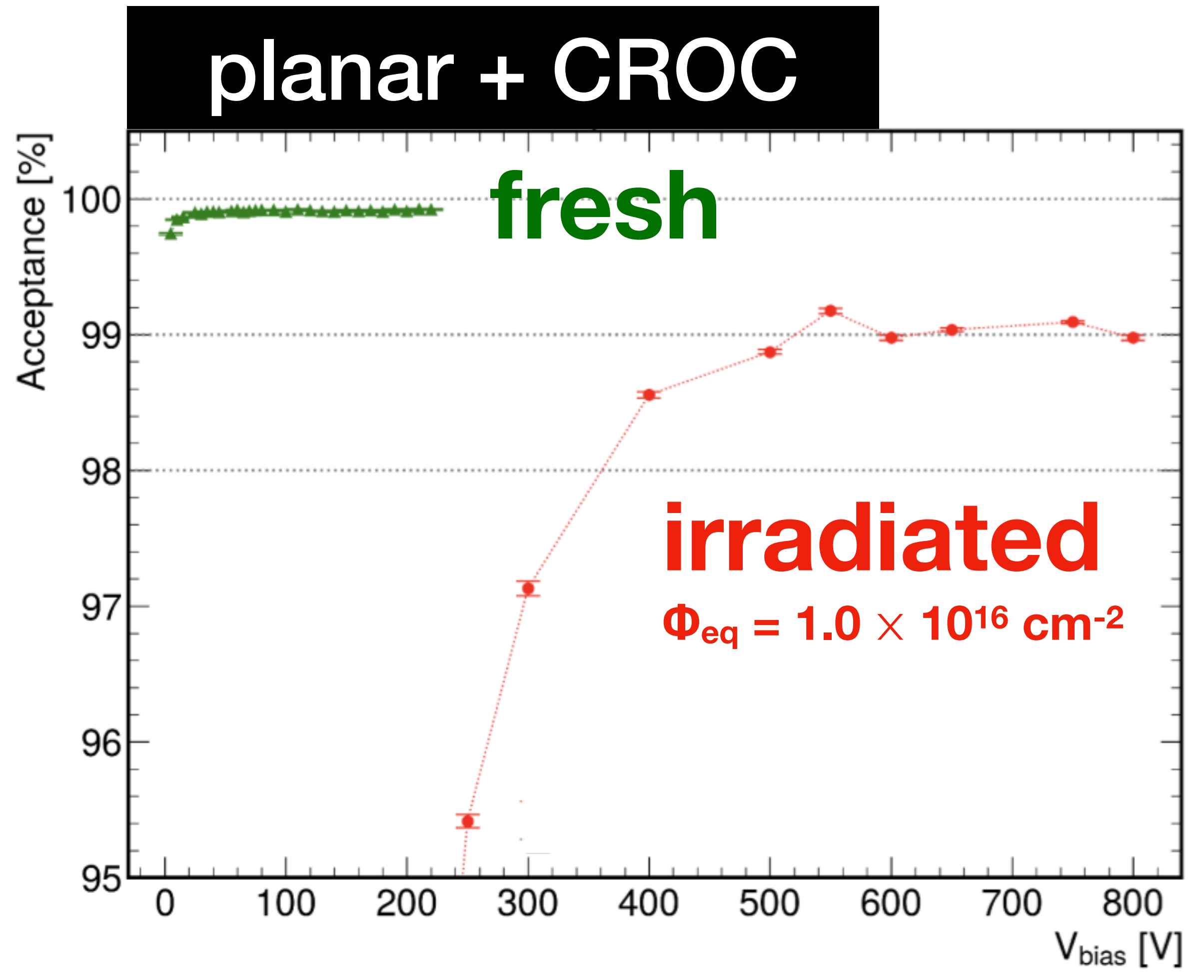


HDI vs ROC alignment measured after each assembly → stored in DCA database for future reference
+ assembled mass measurements, wire-bond pull-test results, module-tuning results, etc.

Si-sensor designs are already finalised after extensive beam-test campaigns
carried out at 3 sites: CERN, DESY, FNAL

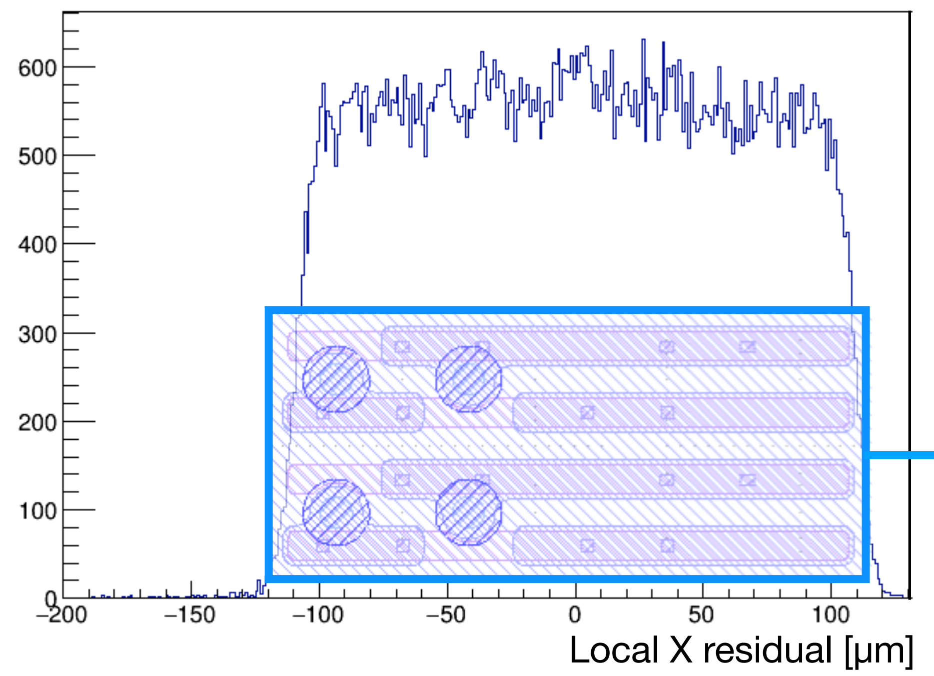
- **full characterisation of module prototypes ▶**
  ↳ planar + 3D sensors bump-bonded to RD53A chips
  + several modules tested with CROC prototypes
- **measuring efficiency, noise, spatial resolution, cross-talk**
  as a function of bias voltage, irradiation, temperature

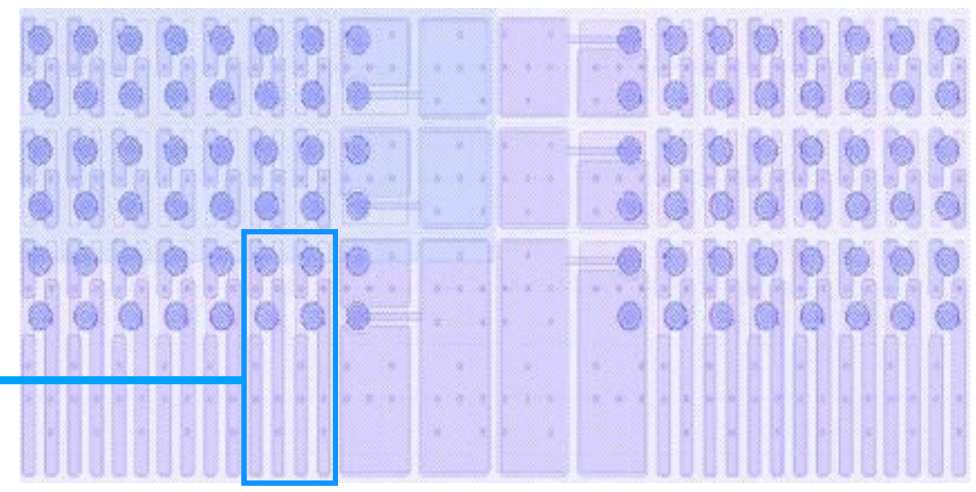




Overall sensor performance under control → specialised studies ongoing
focusing on detailed aspects of the module design and operations

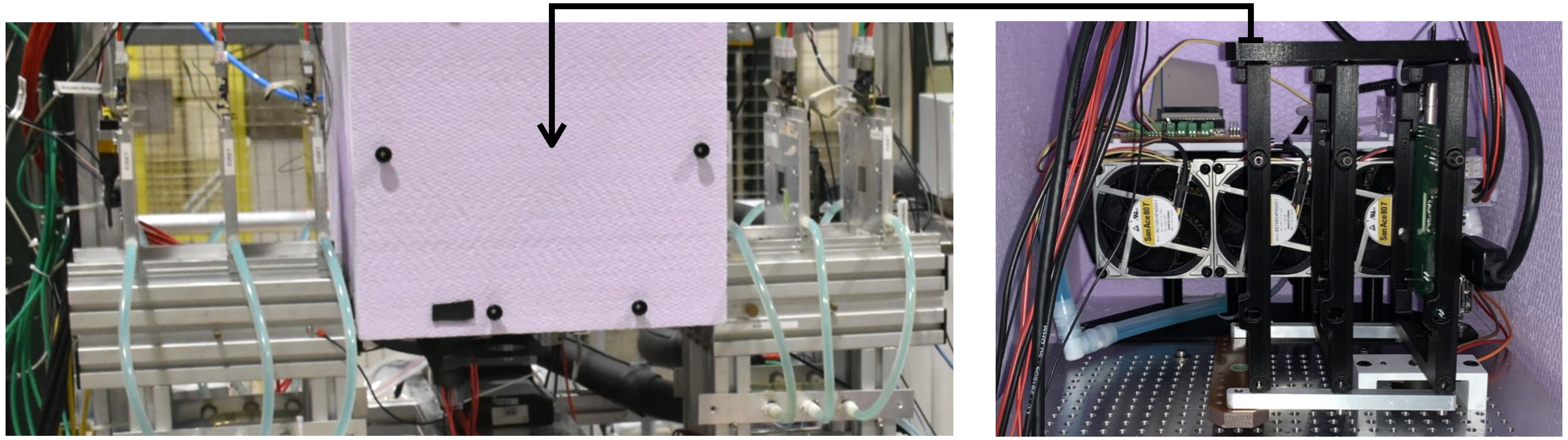
- **resolution dependence on the incidence angle**
- **operation synchronously with accelerator clock**
- **efficiency + resolution in the large pixels ▶**
  e.g. on the chip edges: 225 × 25 μm²





See more actual results in the talk by Georg Steinbruck tomorrow

Most of the beam tests use the EUDAQ data-acquisition system (CERN, DESY)
with 5 × MIMOSA-26 planes as a telescope: 18.4 × 18.4 μm² pitch **+** RD53 module as a refererence plane



DUT box **CERN SPS** (July/August 2022)

DUTs on a rotating stage
cooled down to -35°C

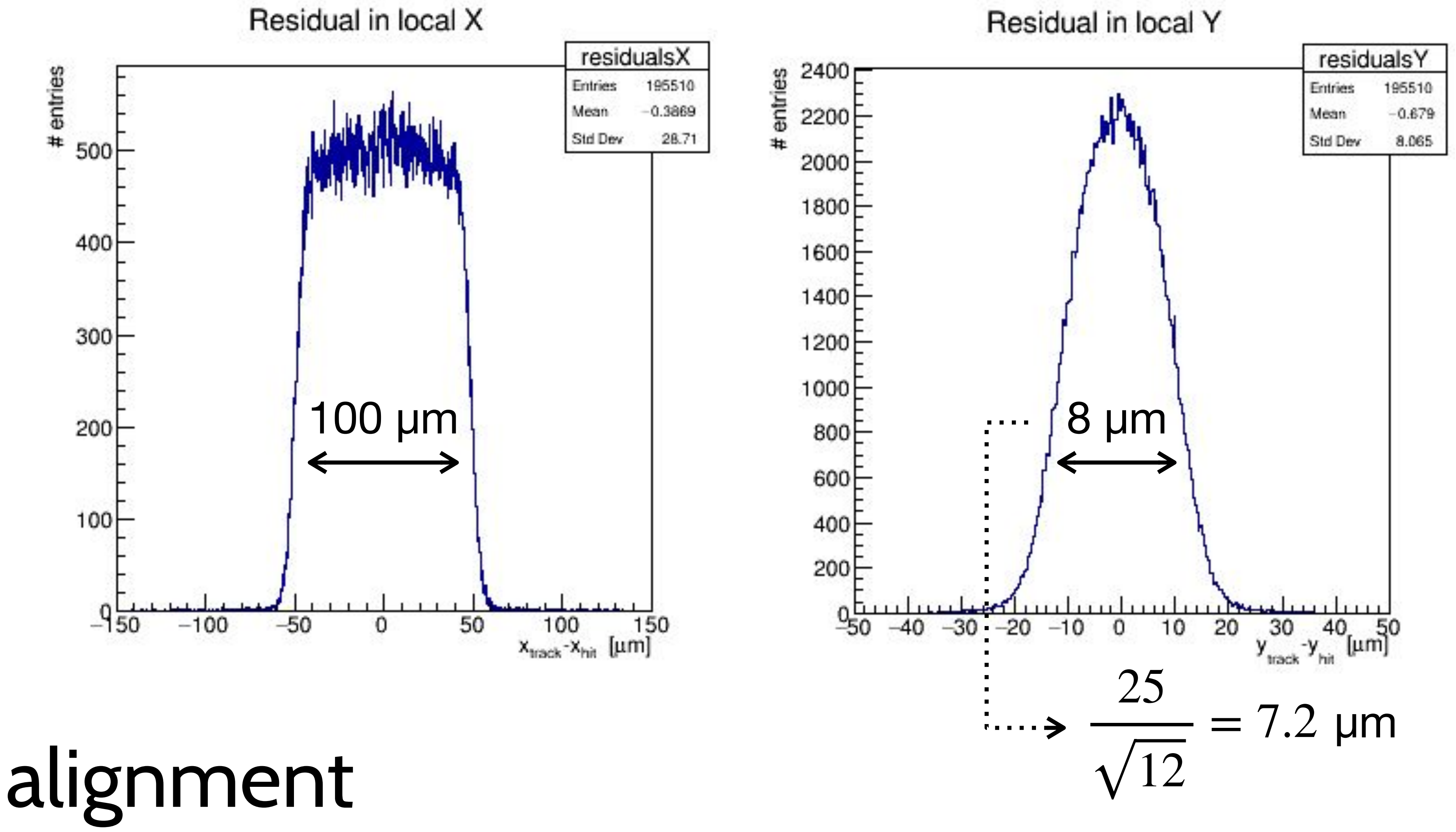
Corryvreckan **software framework used for data analysis**

- **modular structure with flexible configuration**
  ↳ pixel masking, clustering, tracking, alignment, DUT analysis
- **some modules modified for CROC-specific studies**
  maintained in the CMS fork of the repository

Telescope + DUT alignment: **one of the most critical steps** ▶

- **asymmetric pixels need careful treatment in the code**
  ↳ local vs global resolution during track reconstruction + DUT alignment

Properly aligned DUT



Summary

Inner Tracker of the CMS experiment will be fully replaced for HL-LHC
with a much more capable and sophisticated detector

Designs of all the major components are already or close to be finalised
approaching large-scale production and assembly

Several stages of testing are being implemented at different sites
from testing single chips to integrations tests of multiple assembled modules

A lot of lessons are being learnt in the process
to streamline the assembly and quality assurance when large-scale construction begins