The ATLAS ITk Strip End-of-Substructure Card - From design to production

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for the ATLAS ITk Strip EoS Team

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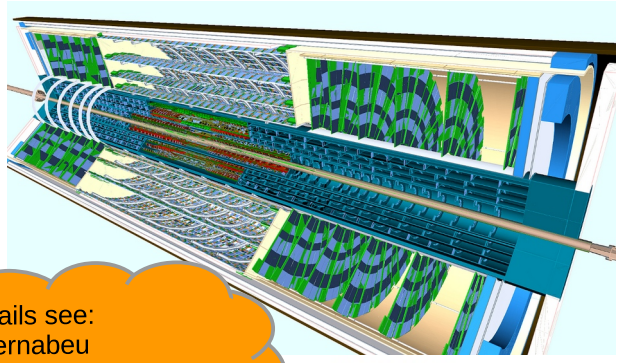
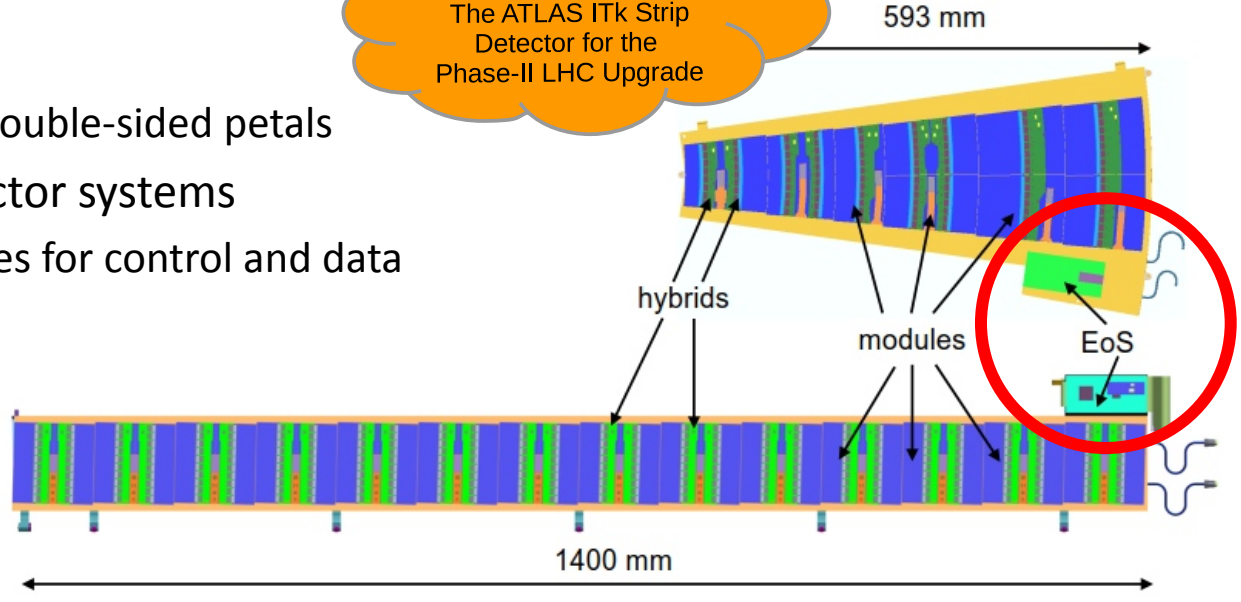
System Overview

- Upgrade of Inner tracker will be full Silicon based
  - Two Subsystems - ITk Pixel and ITk Strip
- ITk Strip consists of
  - A barrel with 4 layers of 392 double-sided staves
    - 256 with “long-strip” modules
    - 136 with “short-strip”modules
  - Two end-caps with 6 disks of 384 double-sided petals
- EoS is the interface to the OFF-detector systems
  - Multiplexer for the detector modules for control and data
  - Power distribution
  - Single Point-of-Failure
- Each stave/petal has two EoS PCBs
  - Main/Secondary

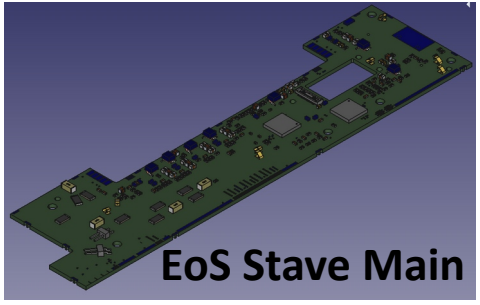


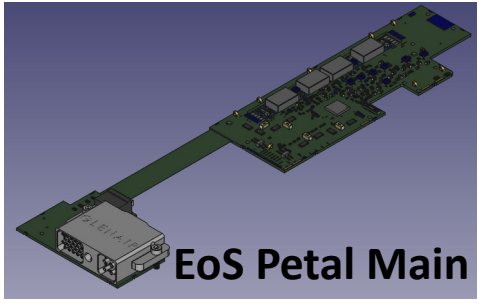
Details see:
J.Bernabeu
The ATLAS ITk Strip Detector for the Phase-II LHC Upgrade

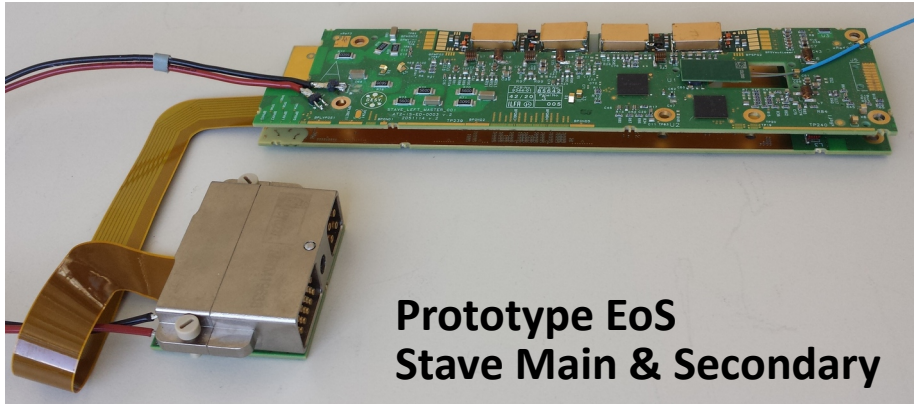


EoS Overview

- Each Petal/Stave needs a pair of EoS
  - Main EoS: with the DC-DC converters
  - Secondary EoS – no DC-DCs
  - Interconnected with connector at EoS edge
- One Pig tail with a flex cable for both
  - HV and Sense wires for the modules
  - Separate LV for both sides
- Tight mechanical constraints
  - Total height < 5 mm
  - 1.8 mm already taken by PCB
  - 3.2 mm available for all components

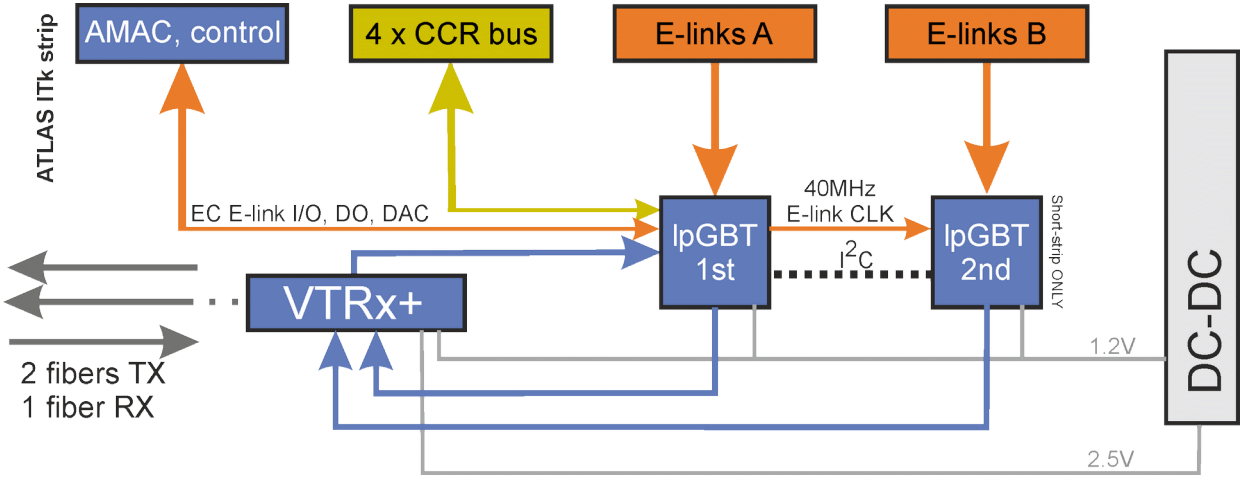

EoS Stave Main

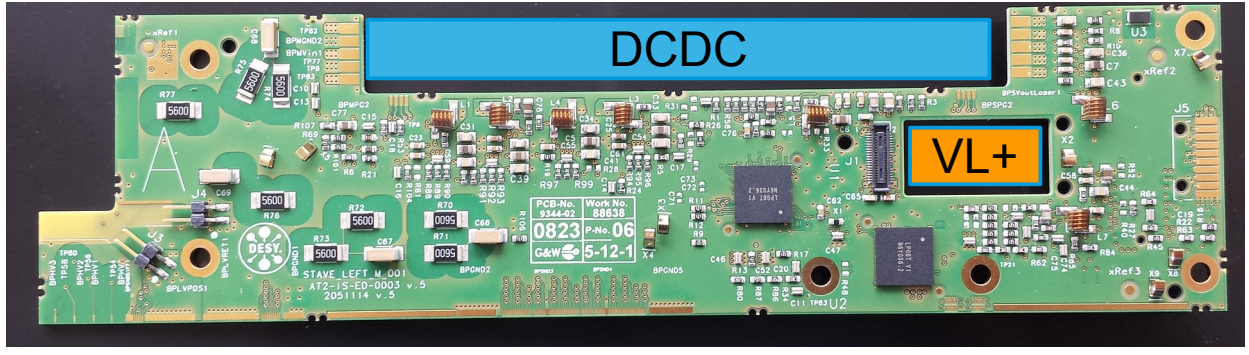

EoS Petal Main


Prototype EoS
Stave Main & Secondary

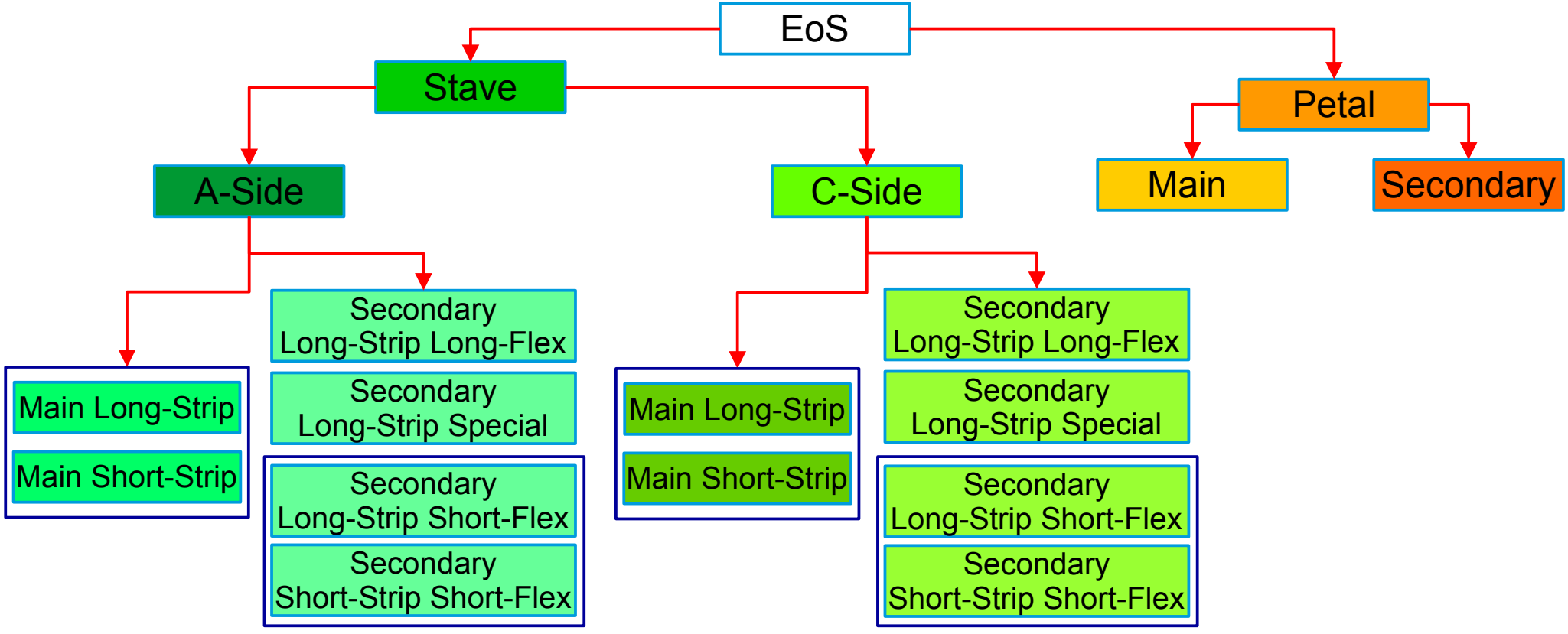
The EoS in Detail

- Based on the CERN ASICs for HL-LHC
  - bPOL's , lpGBT, VTRx+
- Up to 2 lpGBTs
  - lpGBT 1 acts as I²C Master for the second (only needs for a subset of EoS)
- Module Data (E-Links)
  - Up to 14/28 data links @ 640Mbit/s
- Clock, Control & Reset Bus
  - 4 fast control links to the modules @ 160 Mbit/s
- Optical Link
  - 2 TX fibers at 10.24 GBit/s each
  - 1 RX Fiber at 1.25 GBit/s
- Powering
  - Using dual-stage DC-DC





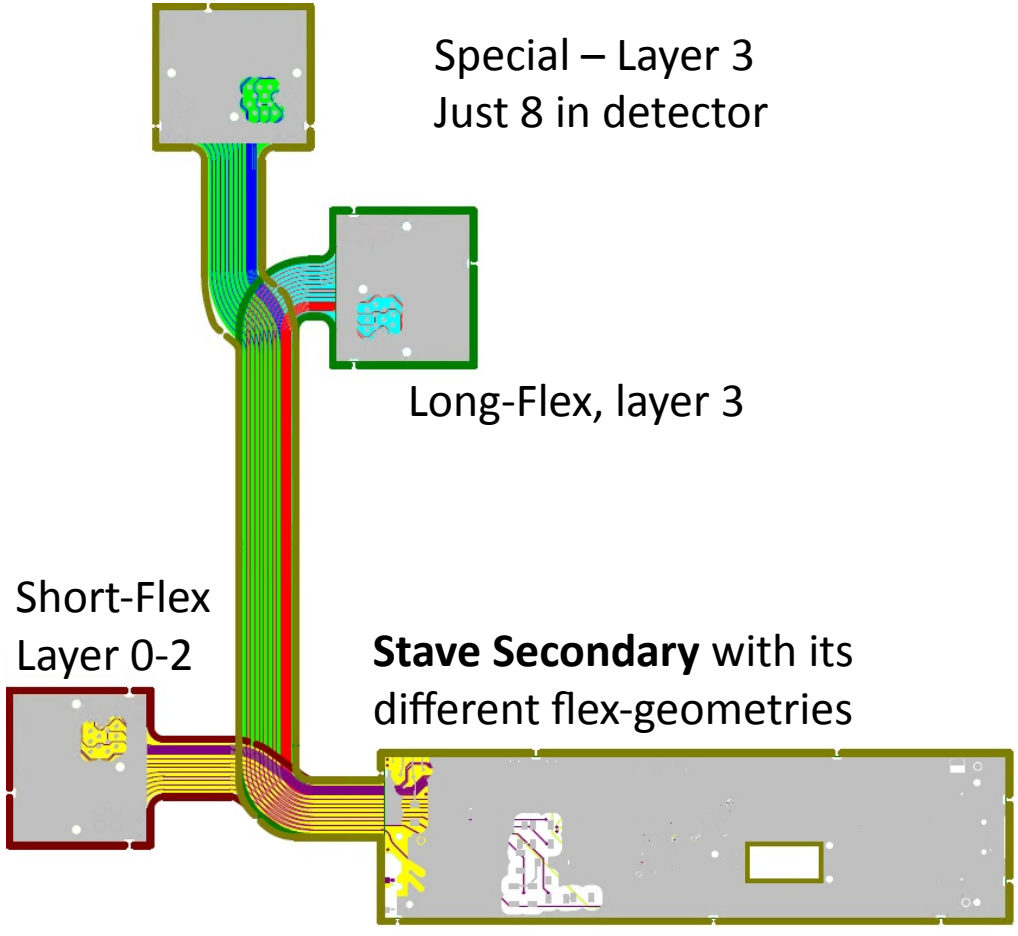
A Plethora of Variants



- Barrel - Requires **12** population variants with **8** different PCB layouts
- End-Cap - Two PCB layouts required – always the same population

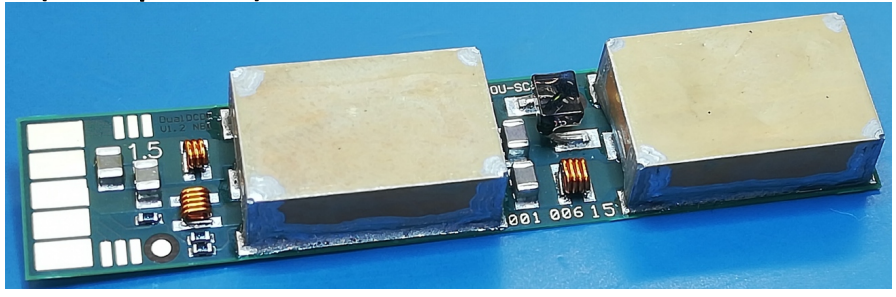
Some closer look

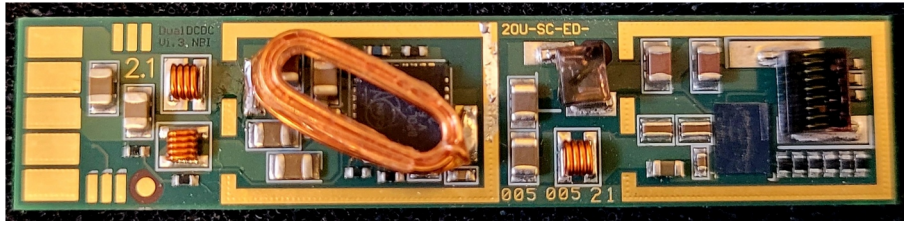
- Number of Barrel variants is driven by
  - Long-Strip vs Short-Strip
  - Different flex shapes due to integration constraints
- EoS PCB design for the barrel
  - Populate with 1 (Long-Strip) or 2 (Short-Strip) lpGBTs
- Separate designs for each flex …
- Altogether we need 1552 cards in the system
  - with approx. 10% spares we need to produce 1800 EoS cards



EoS Powering & DCDC package

- Everything starts with a dual stage DC-DC
  - Stage 1: bPOL12V from 11 V down to 2.5 V (for laser driver VTRx+)
  - Stage 2: bPOL2V5 from 2.5 V down to 1.2 V (for lpGBT)
- This feeds **7** power domains
  - 4 for lpGBT & 3 for VTRx+
  - Each power domain with its own filtering
- Driven by dedicated EoS DC-DC package
  - One Variant for all EoS

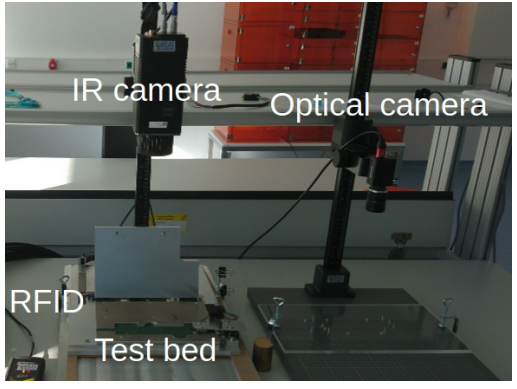


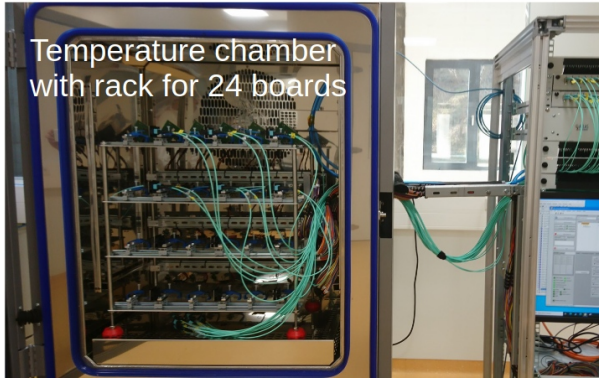


1st Stage 2nd Stage

Production Workflow -EoS

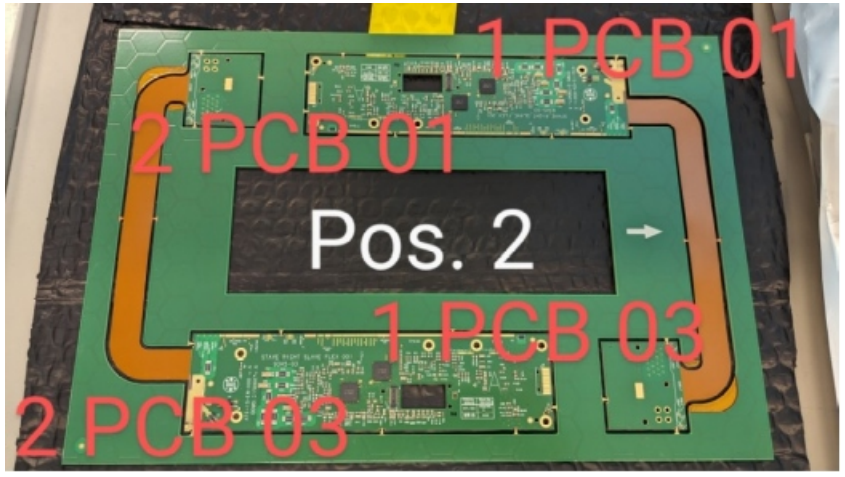
PCB Reception Test Coupon Testing → Population Population QC → 3D X-Ray → Basic Tests → Thermal Cycling → HV Tests → BER Test → Packing & Shipping

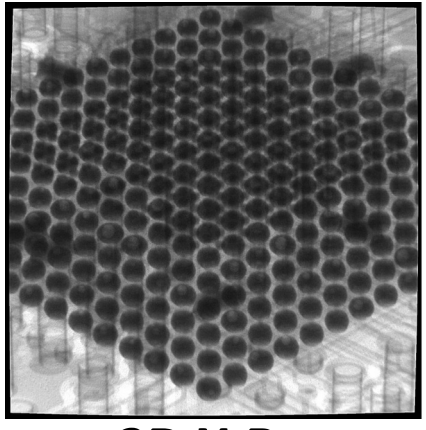




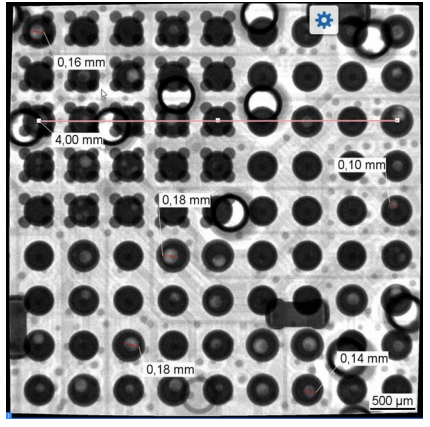
3D X-Raying

- Quality of the BGA soldering
  - Key for long-term operation
  - Difficult to do non-destructive
  - Solder balls neither visible nor accessible
- X-Ray of the BGA packages
  - Evaluate the BGA solder quality
  - 3D also allows to look at via quality
  - Like the images the outcome is gray, not a simple pass/fail
- Very powerful, but requires expert knowledge
  - One Advice: ”if you make a small pre-series of a few hundred boards you get good statistics” ….





3D X-Ray



BGA Cross-section

Keeping Track

Using the ITk production database to store and track components

1) Component Information

→ Retain component hierarchy

→ Identifiers:

- Unique EoS RFID & LpGBT ID

→ Component Type: petal/stave main/sec.

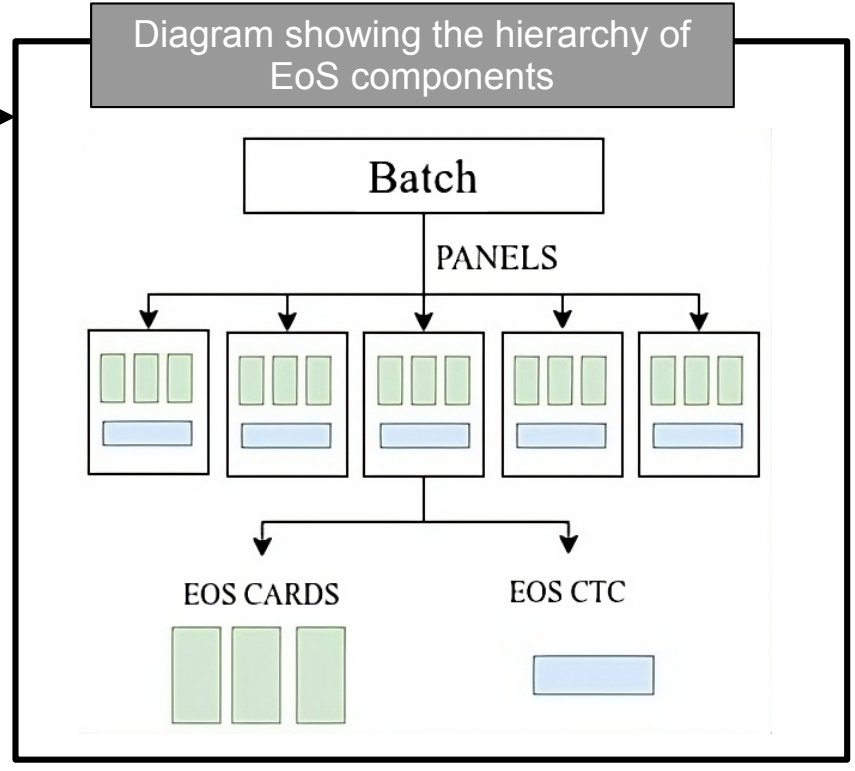
2) Assembly

→ Assemble components to EoS:

- DCDC, LpGBT

→ EoS assemble to:

- Staves & petals



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3) Quality control

Store results of QC process

→ Current component stage

→ Results of QC testing

- Pass/Fail

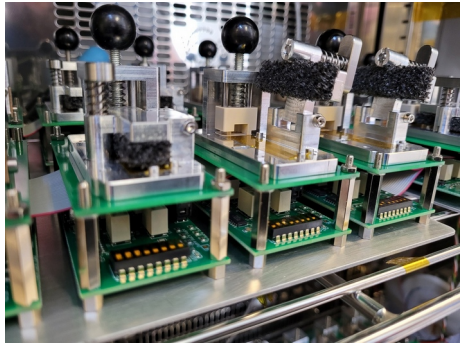
→ Test Data e.g. floats, lists or images

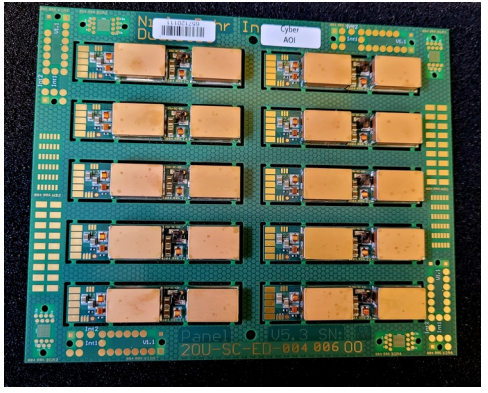
EoS DCDC Production

PCB Reception

Population
SMD + hand soldering of coils and shielding boxes

Breakout from panels



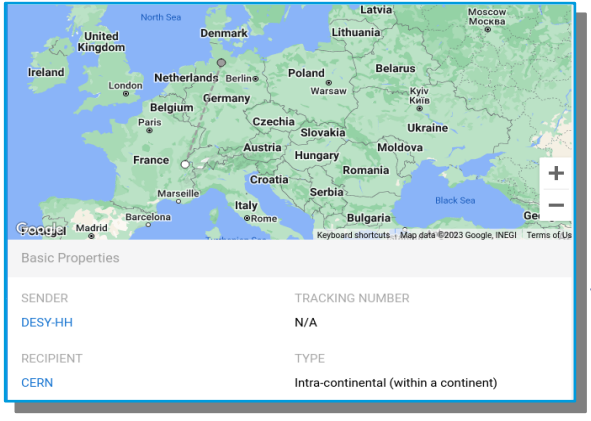


Test Coupon testing
Resistivity of traces + vias
Bonding tests

DCDC basic tests
Thermal cycling

Packing & Shipping

Shipping around the World



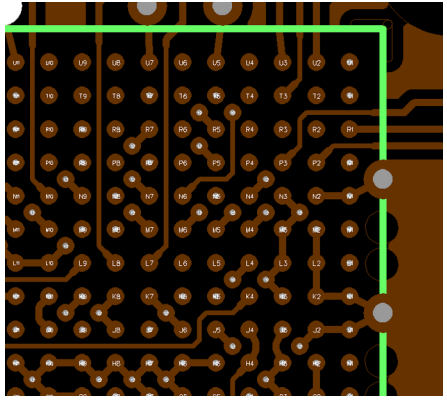
Everything tracked in the data base

A Decade of EoS – Lessons Learned

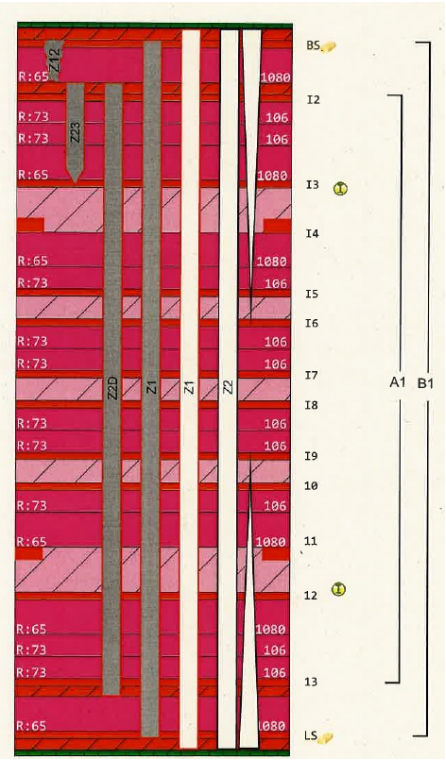
- Project has been evolving from 2012/13 to today
  - Moving from GBTx to lpGBT
  - Forking more and more variants
  - But basic approach remained relatively stable
- Status
  - Pre-Production has been completed - EoS being used at all Assembly sites
  - Production has just started – plan is to be done in summer 2024
- Good time to look back, what worked well (and what didn't)
- Skip most of the motherhood statements
  - Obviously less variants are a good thing….

PCB Complexity

- The combination of
  - Fine pitch BGA - (lpGBT: 0.5mm)
  - Via-in-pad
  - Board size
  - Number of layers and stack-up
  - Halogen-free requirements
  - Many variants with each low quantity
- Made each design vendor specific
  - Single-vendor issues – not easy to transfer design
- And reduced the selection of vendors willing to do it
  - Just because your design tool allows to design does not imply a vendor is willing to make it…
  - And viable does not mean economically attractive



Fine-pitch pads & vias

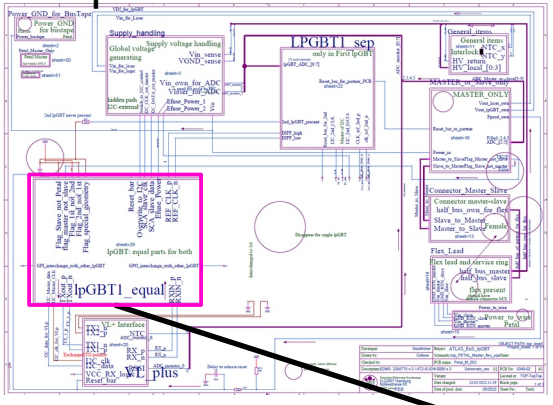


PCB Stack-Up

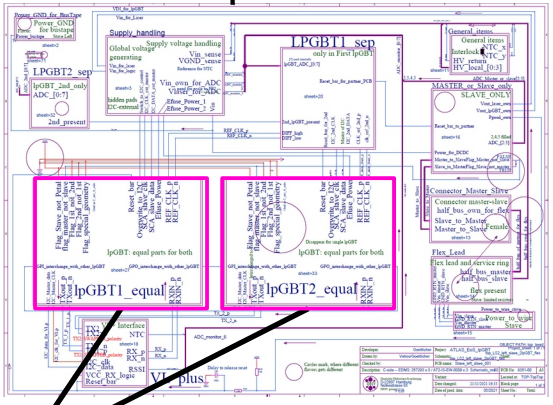
Hierarchical design

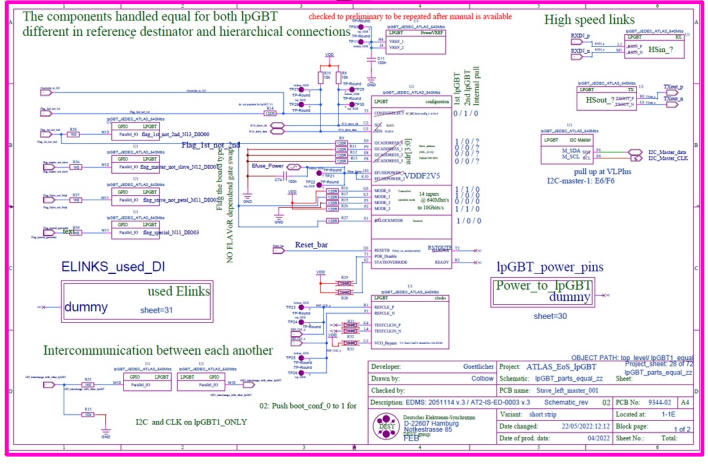
- Hierarchical design with reused configurable building blocks.
- Top-level is dependent on variant
  - Individual building blocks configurable per variant
- Advantages:
  - Blocks once proven in a single flavor are likely to be correct for all other designs → less prototyping
  - Changes to e.g. the lpGBT block are automatically propagated to all variants
  - Improves maintainability

Top level: Petal…



Top level: Stave





Chip U1 or U2

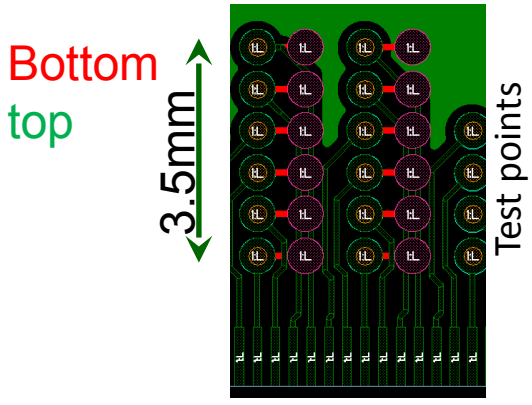
Pins

Leave unpopulated

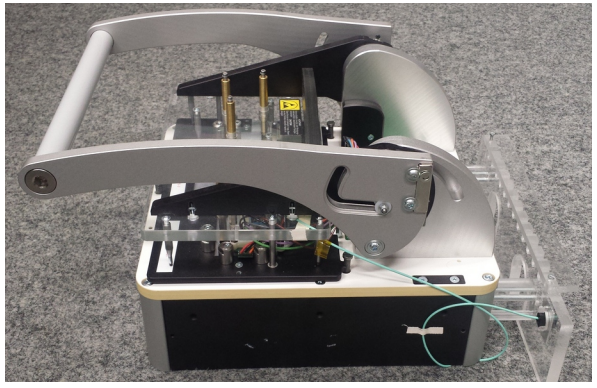
Values

Needle-Probe station

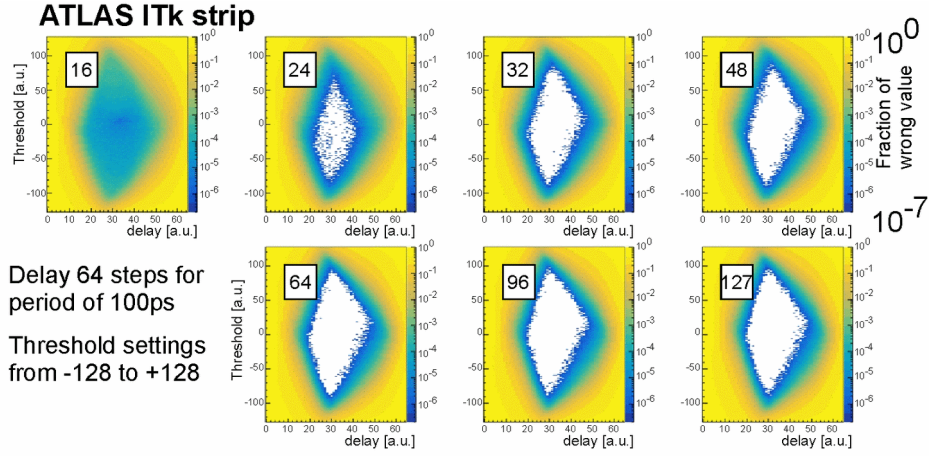
- We have to test connectivity of the PCB –
  - 28 Elinks & 4 CCR links
  - Can't touch the bond-pads
  - Do it 2000 times..
- Solution – Needle-Probe Station
  - Widely used in industry
  - Requires one per PCB variant
  - 640 Mbit/s through 300 µm thick needles
- Dedicated Firmware
  - Drives all links (via VL+ and lpGBT)
  - BER Tests of each PCB (> 10^{-12} is spec)
  - On-line Eye Diagrammes



Bond pads

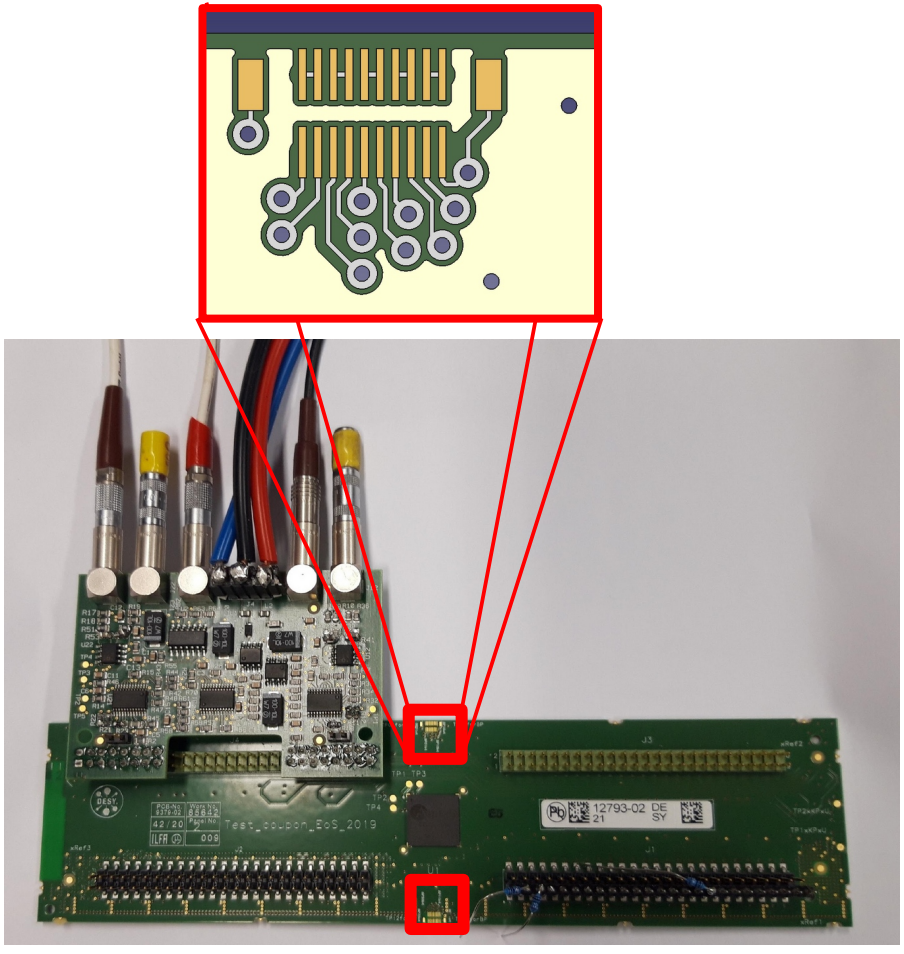


EoS Needle Prober



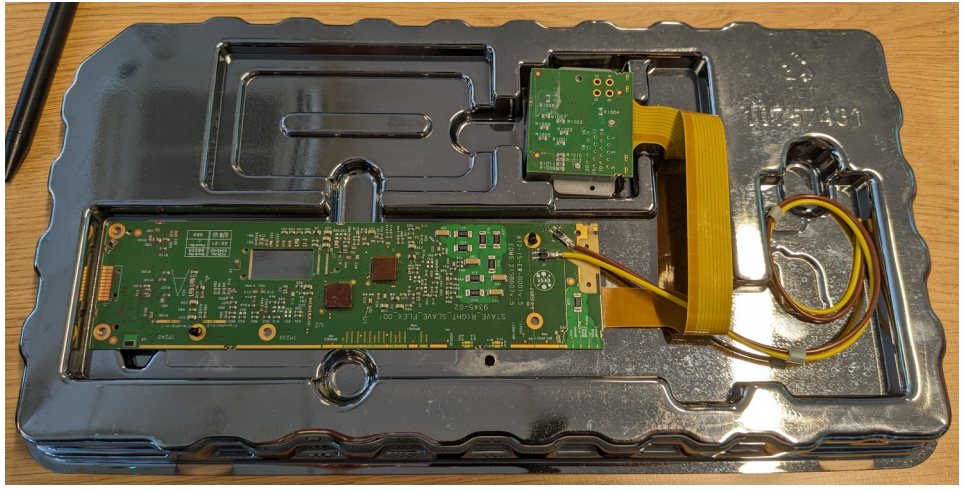
Test Coupon (CTC)

- Enables testing PCB panel quality before populating the EoS
- 1 m long traces on each layer to check resistance.
- 1 m long impedance trace to check the impedance of relevant layers.
- A dummy 0.5 mm BGA to check resistance after soldering.
- Long via chain of all via types:
  - 365 THT vias (1-14)
  - 200 Vias 1-2 (pad 275 µm)
  - 270 Vias 1-2 (pad 300 µm)
  - 223 Vias 2-3 with drill 0.3mm
  - 190 Vias 2-3 with drill 0.15mm
  - 190 Vias 2-13
- Bond pads with nearby vias to check bonding and pull-forces.



Some other points

- Using a “flex” for the LV
  - With up to 10 A, the flex turns into a spring
- Packaging is easy
  - Unless you want to have one box for all variants
- Aiming for concurrent engineering
  - Mechanical envelop definitions enabled concurrent electronics design and mechanical integration
- Thinking about QC
  - Each tests should be designed to identify a known problem
  - No random “let’s run for 100 hours”
- Try to get the most out of the reviews
  - We benefited a lot from a great review team – good points and a fresh look



EoS Stave A Secondary in package

Summary

- The EoS is the central interface between on-detector and off-detector for the ATLAS ITk-Strip Detector
- Entering production stage
  - Having to produce almost 2000 cards in twelve different variants
- Necessity to use new methods
  - Both for Design& Testing
- Many lessons learned – most importantly
  - K.I.S.S → Keep it simple, stupid !