Powering SiPMs and front-end electronics in HEP detectors

The ALDO2 ASIC

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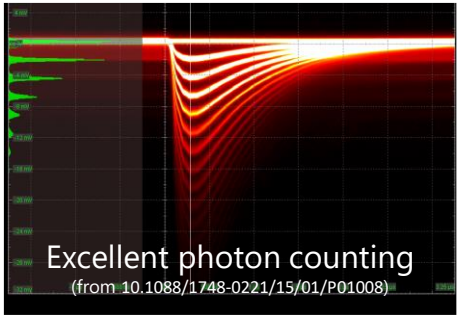
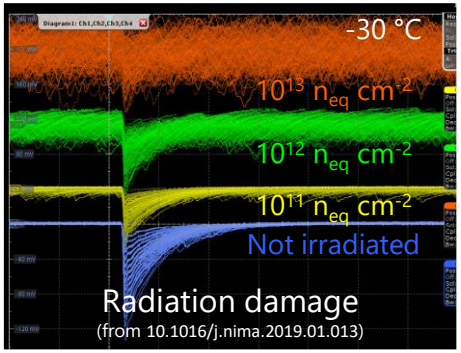
SiPMs in particle physics experiments

- Silicon photomultipliers (SiPMs, aka MPPCs) are becoming widely adopted in many particle physics experiments at accelerators
  - CALICE, T2K, Belle II, CMS, GlueX, KLOE-2, LHCb, MEG II, NA62, …
  - … and more experiments are considering them for upgrades
- SiPM advantages are many and widely known
  - Excellent photon counting performance, high detection efficiency, high gain, fast response, compactness, immunity to magnetic field, low bias voltage, decreasing cost per unit of area, …
- And so the drawbacks
  - High dark counts, moderate radiation hardness, performance strongly dependent on bias voltage and temperature, high capacitance per unit of area, crosstalk, after-pulses, …
- All the experiments mentioned above adopt similar strategies to mitigate drawbacks
  - Operation at low and stable temperature
  - Precise voltage and current control
  - (Periodic annealing)

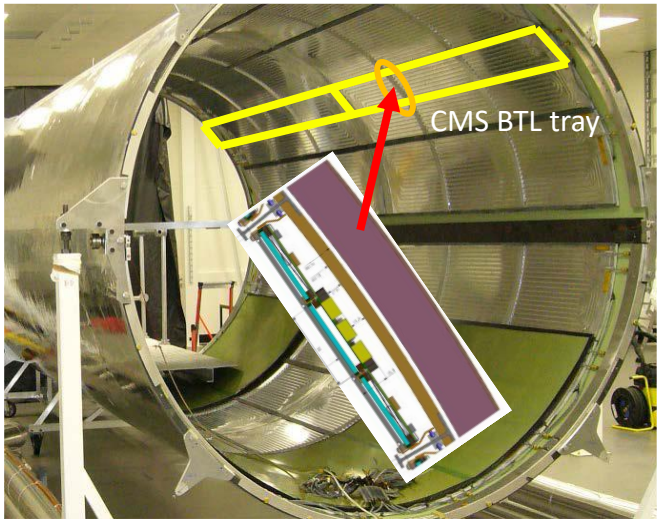




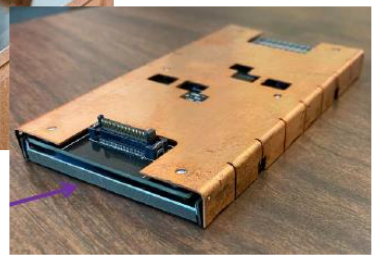
Powering SiPMs at HL-LHC

- At HL-LHC challenges with SiPMs will further increase
- Use case 1: CMS Barrel Timing Layer (LYSO bars + SiPMs)
  - 768 SiPMs per tray (with shared bias supply)
  - About 1 mA/SiPM at EOL irradiation level → 0.8 A total
  - Up to 40 m distance between bias PSU and SiPMs
  - No access to the detector after the tracker is mounted
  - Limited power budget, bias voltage decreased as dark current increases
- Use case 2: CMS High-Granularity Calorimeter (plastic scintillator tiles + SiPMs)
  - Similar needs

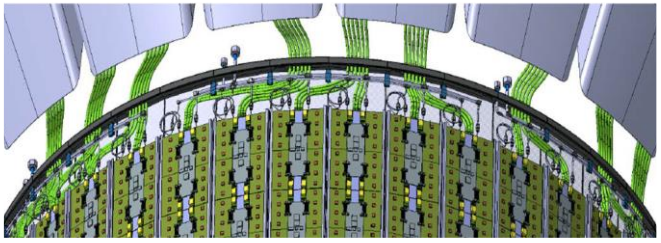
Point-of-load (POL) regulation of SiPM bias supplies and on-detector monitoring of SiPM current



CMS BTL module



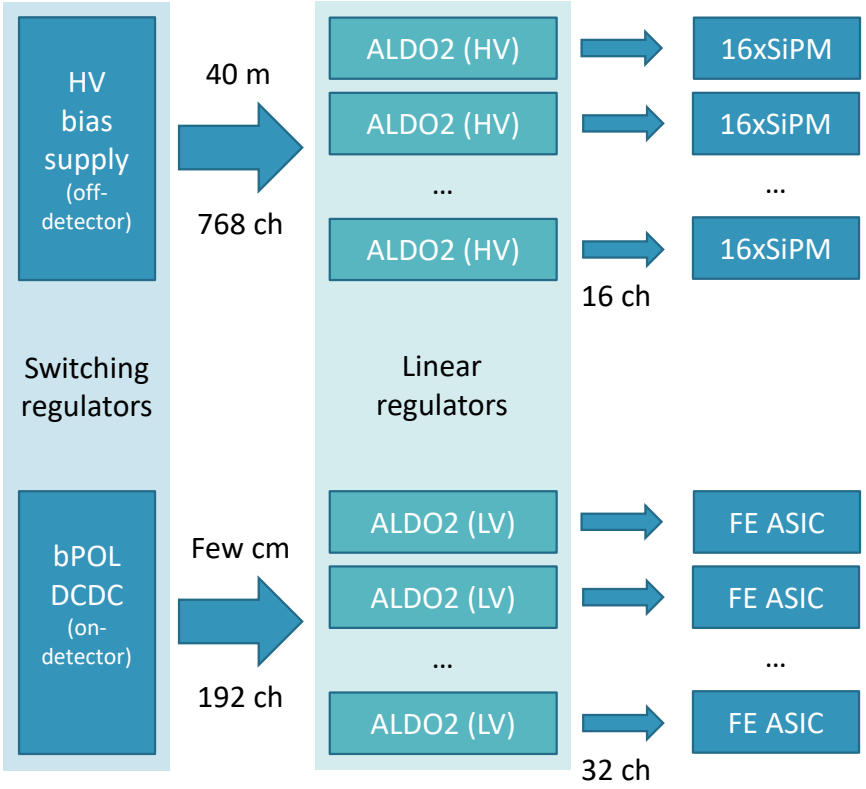
CMS BTL interfaces



ALDO2 ASIC = Adjustable Low Drop-Out linear regulator with 2 functions

- SiPM bias voltage regulation, protection, and monitoring
  - Fine segmentation
    - 768 channels for each HV bias supply → 16 channels for ALDO HV channel
  - Independent setting and switch-off of each SiPM group
    - ~Few V bias voltage adjustment with ~tens mV resolution
  - Dark current measurement for each group
- FE ASIC power supply regulation
  - Filter noise and transients on the power supply
  - Enhance thermal and load stability
  - Fine segmentation
    - 6 FE ASIC for each bPOL DCDC → 1 FE ASIC for each ALDO
  - Generate aux voltages (e.g. GBT-SCA 1.5V)

SiPM bias voltage regulation and protection (HV)



FE ASIC power supply regulation (LV)

Specs

LV part

- Input voltage: 1.6 V to 3.3 V
- Output voltage: **adjustable** (min 0.6 V)
- Output current: **0.6 A**
- Minimum dropout: 0.4 V
- PSRR/line regulation: **-40 dB** (10 µV/mV) **at max load**
- Noise: 30 µV RMS (10 Hz – 100 MHz)
- Thermal stability: 50 ppm/°C
- Thermal overload and over-current protection (0.9 A limit)
- Shutdown capability

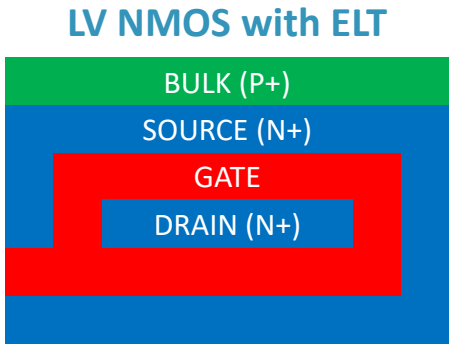
HV part

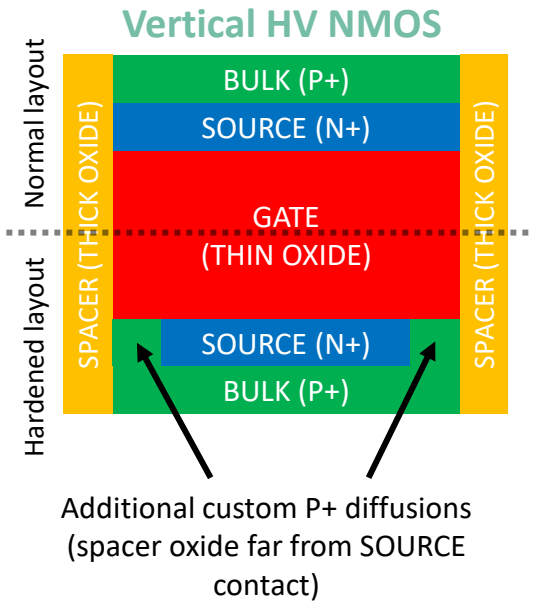
- 2 independent channels
- Output voltage: **adjustable**, 10-60 V
- Output current: **32 mA**
- Minimum dropout: 1 V at full load
- PSRR/line regulation: **-40 dB** (10 mV/V) **at max load**
- Noise: 350 µV RMS (10 Hz – 100 MHz)
- Thermal overload and over-current protection (50 mA limit)
- Shutdown capability
- **Output current measurement**

Technology choice

- onsemi 0.35 µm I3T80 CMOS technology
  - Qualified for radiation hardness by CERN DCDC group (F. Faccio et al., DOI: 10.1109/TNS.2010.2049584), used by FEAST DCDC and some bPOL DCDCs
  - Has all the devices needed (70 V N- and P-channel DMOSFETs, standard LV MOSFETs, etc.)

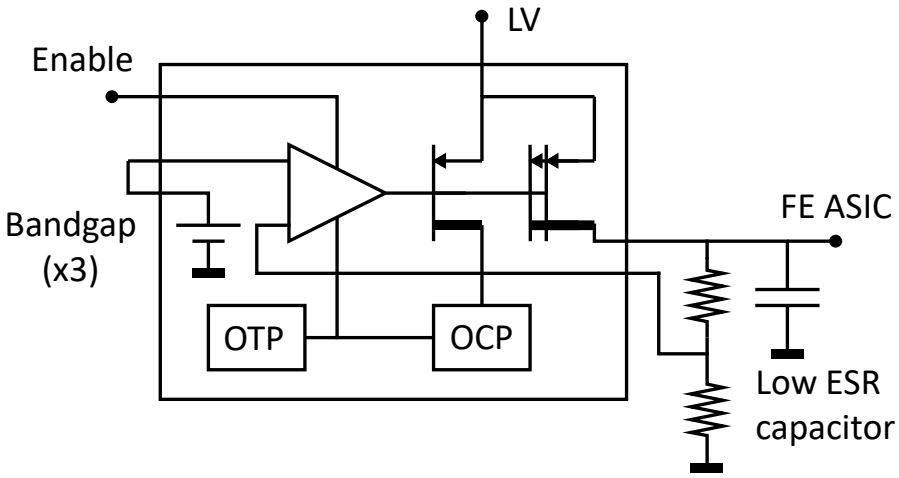
- Still some critical points for our application
  - ELT required for **LV NMOS**
  - **HV NMOS** requires custom layout to reduce leakage above 100 krad
  - On resistance of HV MOSFETs increases with displacement damage
    - Not super critical for our application, use much larger transistors
  - Use all the standard RHBD techniques (guard rings, spacing, etc.)
  - HV transistors have thin-oxide gates, max V_{gs} limited to 3.6 V

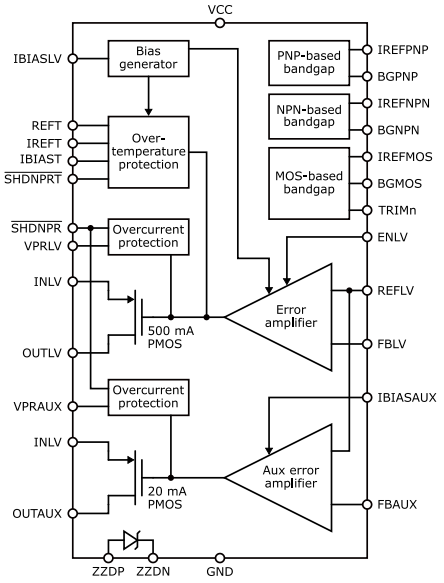




LV part

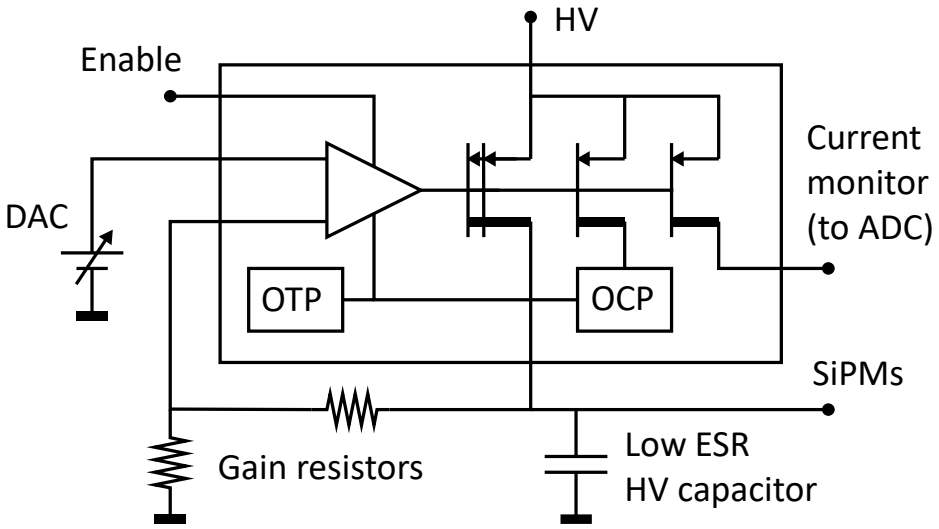
- Standard LDO topology (PMOS output MOS)
  - >500 mA output current, very large output MOS
  - Adjustable gain with external resistors
  - External compensation with low ESR capacitor
- Embedded bandgap
  - 3 bandgaps included (MOS, PNP, NPN based)
  - MOS-based selected due to best radiation hardness
- Output can be disabled to power cycle the load
- Overcurrent protection (OCP) and overtemperature protection (OTP) protect the device in case of load issues (shorts, etc.)





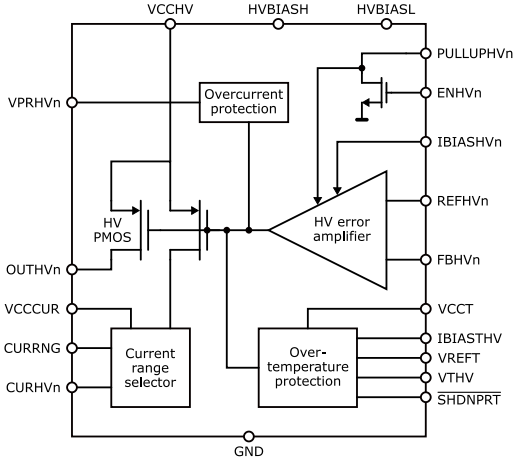
HV part

- LDO topology (HV PMOS output MOS), driven by requirements
  - Improve stability and noise of bias supply → active feedback
  - Capability to disable each channel independently in case of issues in one SiPM array → series switch required
  - Avoid parasitics on FE ASIC input node → high-side regulation
  - Output current measurement → current mirroring
  - High efficiency → PMOS output HV MOS for low dropout (e.g. 45 V input, 42 V output, 93% efficiency)
- Output voltage adjustable in two ways
  - Gain resistors to match SiPM model needs
  - Voltage reference using a DAC outside of the chip (FE ASIC in BTL or GBT-SCA in HGCAL)



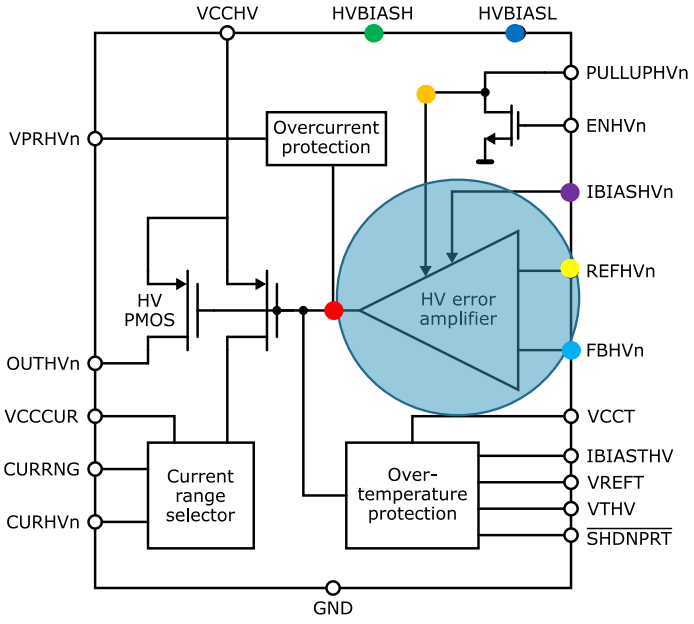
Main challenges of this architecture

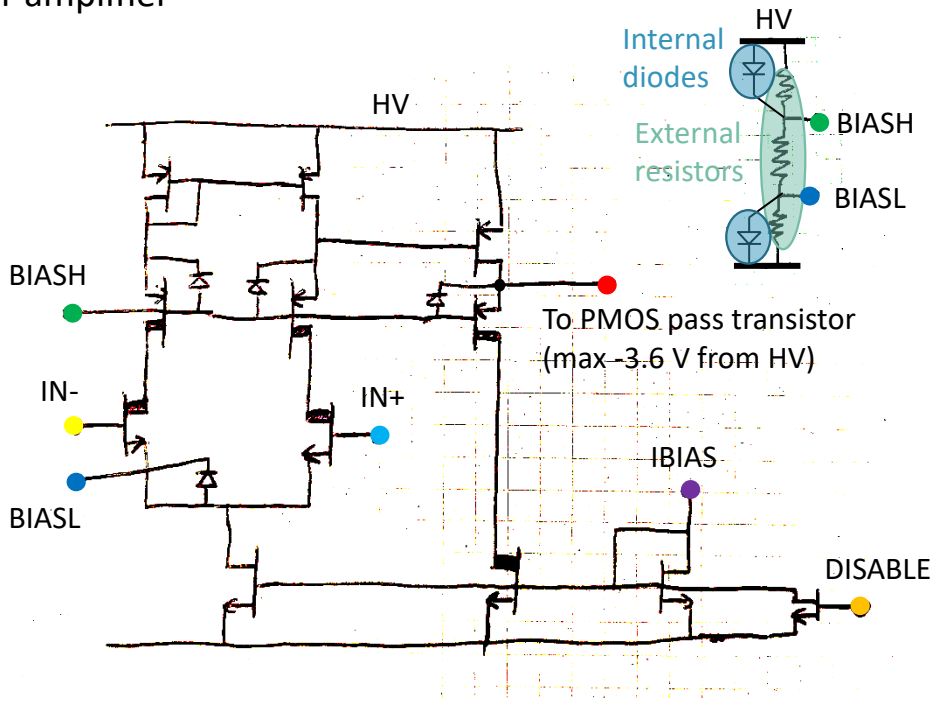
- Driving LV (thin-oxide) gate of HV MOS
- Gain is high (30-50 V/V)
  - DAC noise and input offsets must be minimized
- External compensation with low ESR tantalum capacitors
  - Few options rated 50 V, rather bulky (7.3x4.3x1.8 mm^3)



HV part – Error amplifier

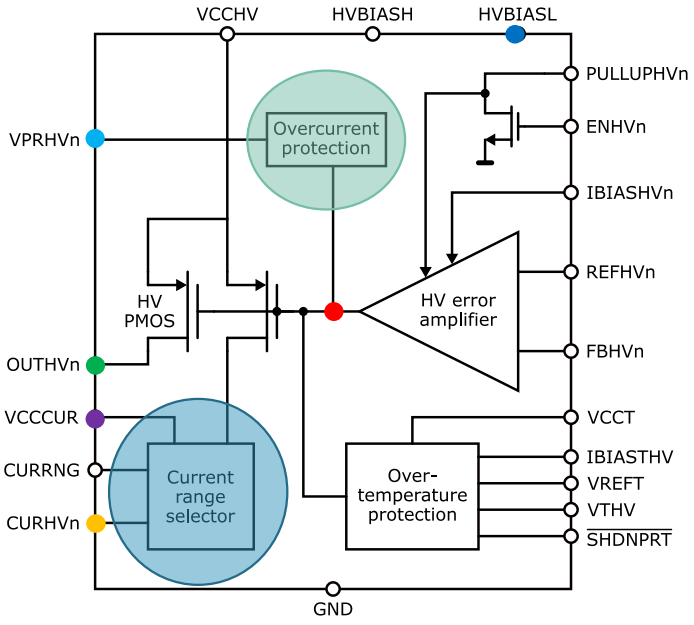
- The error amplifier has to operate between HV rail (up to 60 V) and GND
  - Mix of HV and LV transistors + bias lines to limit DC voltage excursion within LV MOS max ratings
    - Bias lines (BIASH and BIASL) are provided externally (ALDO2v0-v1) or generated internally (ALDO2v2)
- High loop gain (70 dB) to minimize regulation errors
- The regulator is disabled by acting on the error amplifier

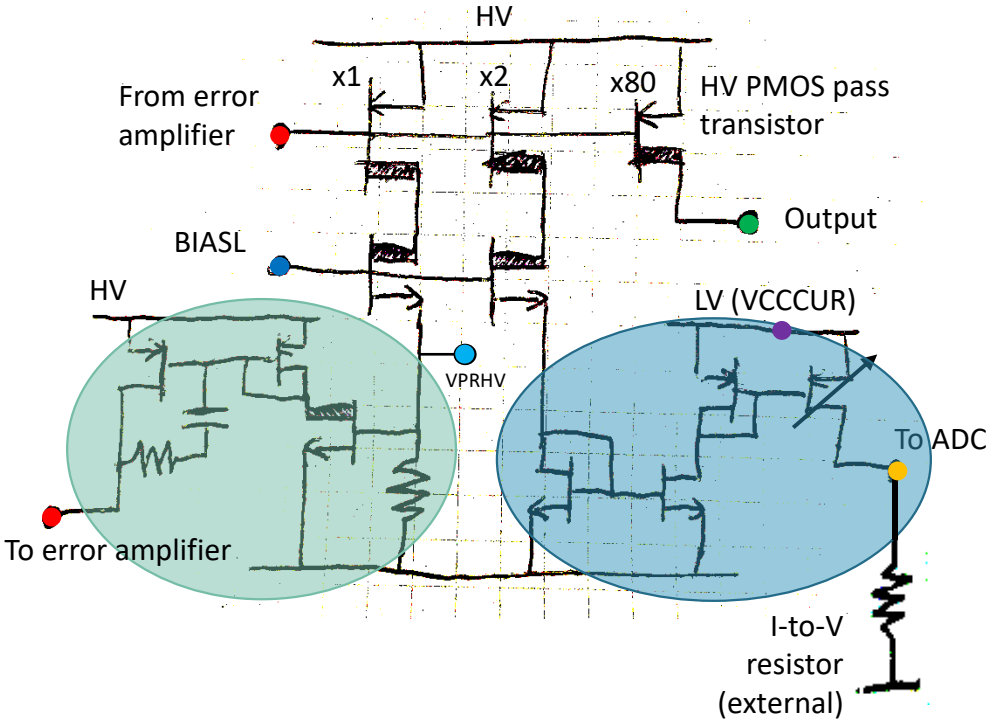




HV part – Output current protection and monitoring

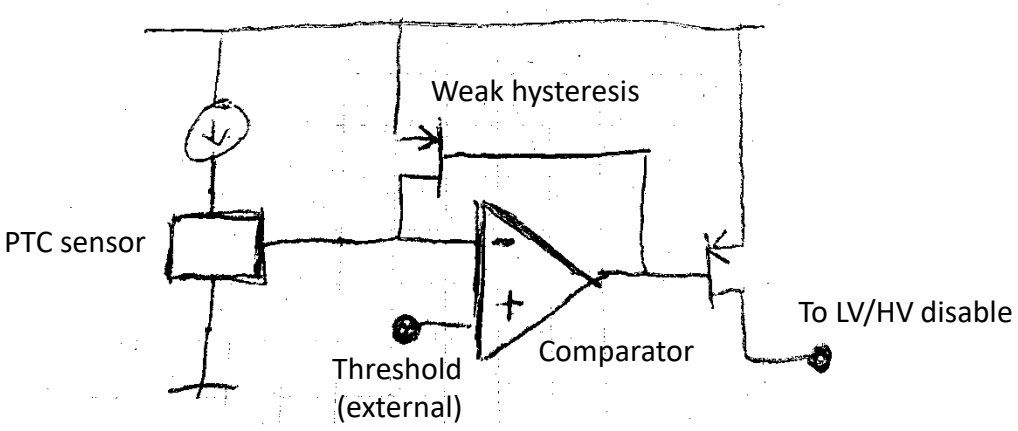
- The over-current protection and output current measurement use a similar strategy
  - A fraction of the output current is mirrored in the two circuits
  - The over-current circuit has a constant current limit (no foldback)
  - The current measurement circuit further mirrors the output current with tunable ratio (1/40 and 1/800)
    - An external resistor converts the output current to a voltage, matching the ADC full-range and SiPM specs

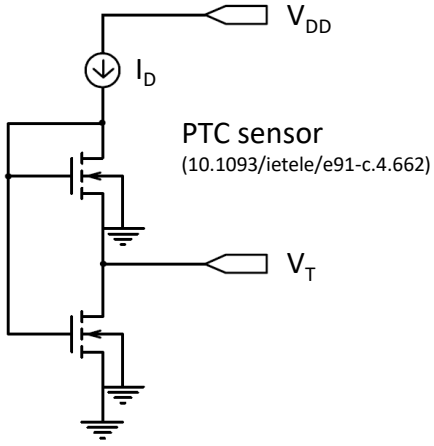




Over-temperature protection

- The over-temperature protection acts both on HV and LV part
- Internal PTC voltage compared to an external threshold
- PTC element based on weak-inversion composite MOS transistor (10.1093/ietele/e91-c.4.662, 10.5772/39231 and 10.1049/el.2010.1346)

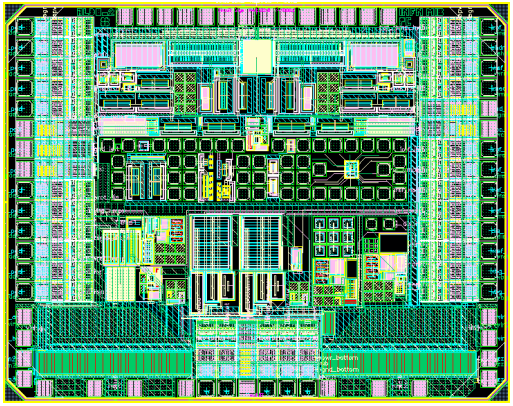




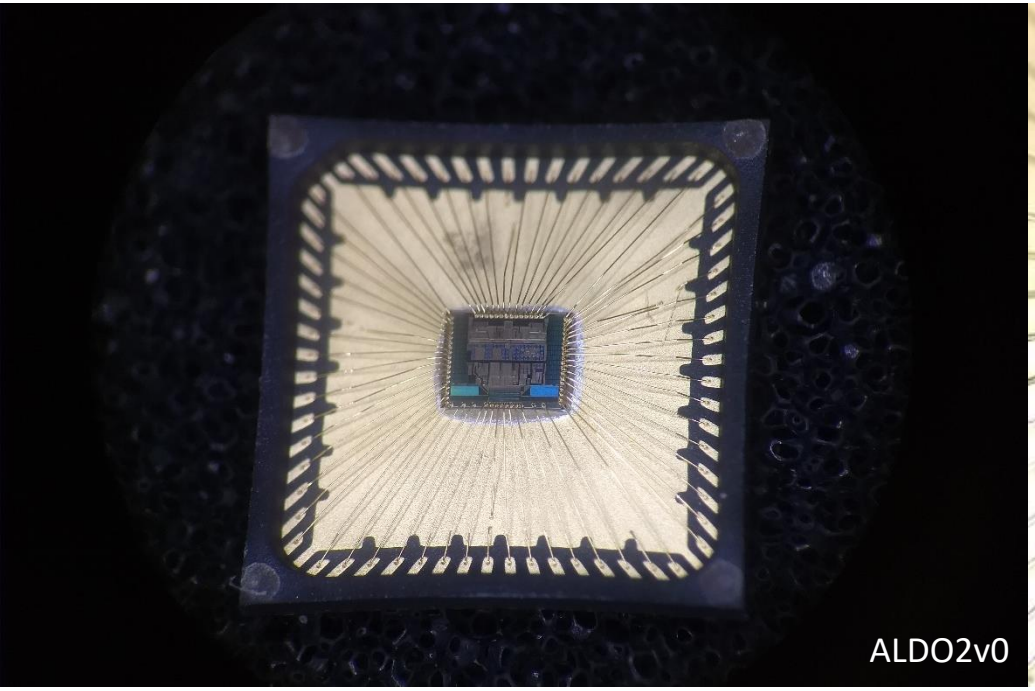
Parameter		Test Conditions	Min	Typ	Max	Unit
V_T	Temperature sensor voltage	Temp. = 27 °C	163.9	166.4	168.7	mV
$\%V_T$	Relative error		-1.5		1.4	%
dV_T/dT	Thermal coefficient		0.411	0.424	0.437	mV/°C
dV_T/dV_{DD}	Power supply coefficient			6.8		mV/V
dV_T/dI_D	Bias current coefficient	Linearized around 6 µA		1		mV/µA

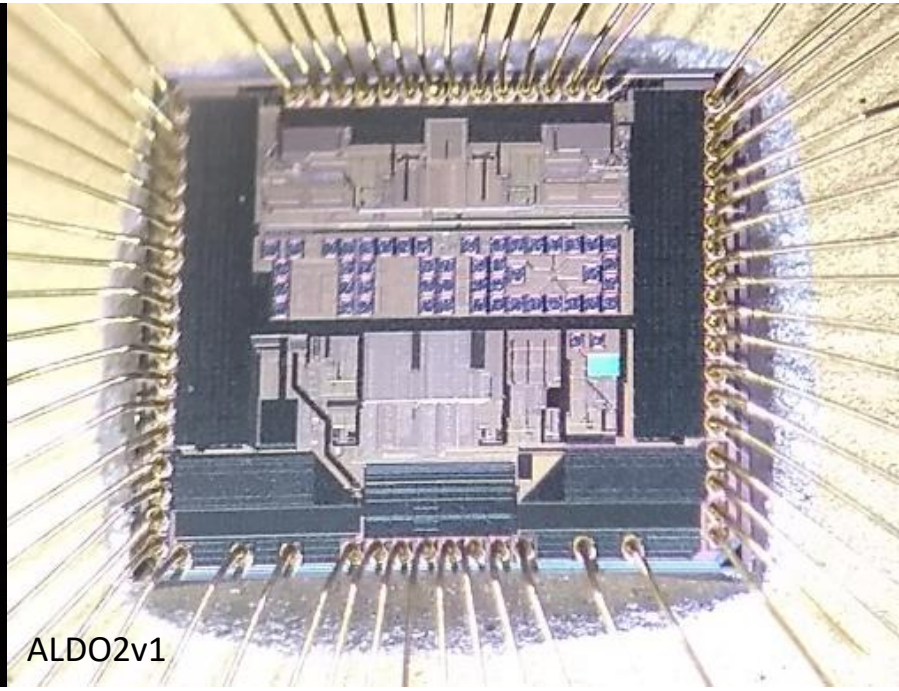
Prototyping

- 2019: ALDO2v0
- 2021: ALDO2v1
  - Re-centered bandgap trimming, higher default current limits
- 2022: ALDO2v2 (final production)
  - Self-bias, extend input voltage range
  - 45k chips produced



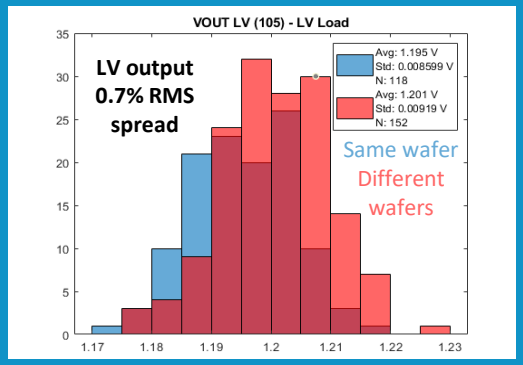
Die area 2.47 x 1.95 mm^2
Package QFN64

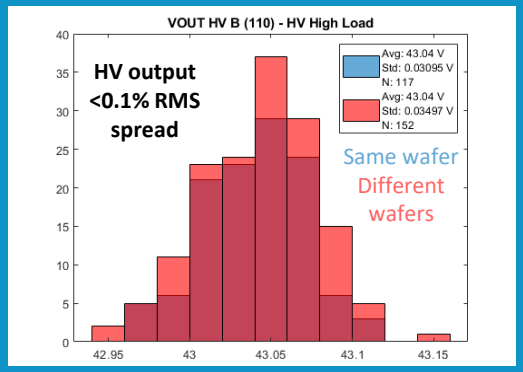




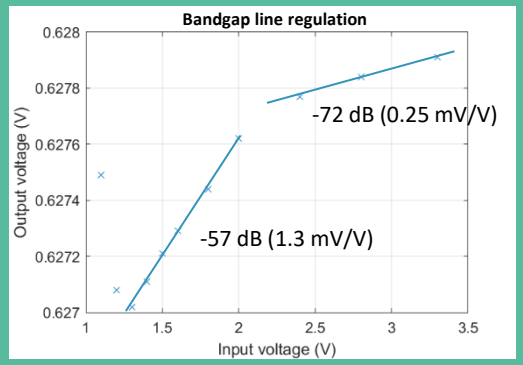
Selected measurements

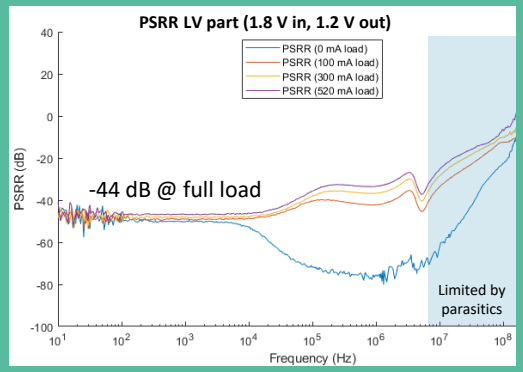
Output voltage spread of ALDO2v2



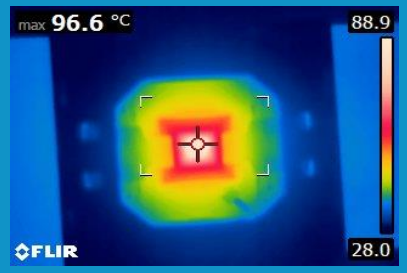


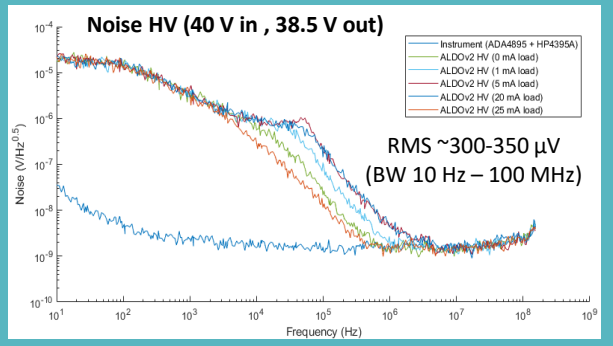
Line regulation and PSRR – LV part



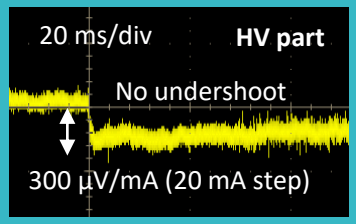


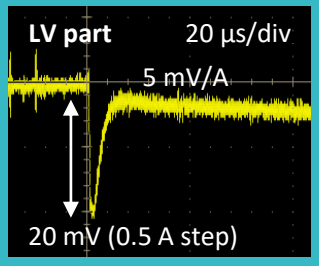
Over-temperature protection (shorts on all outputs)

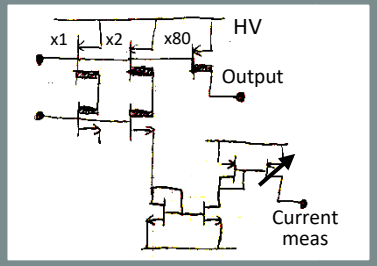


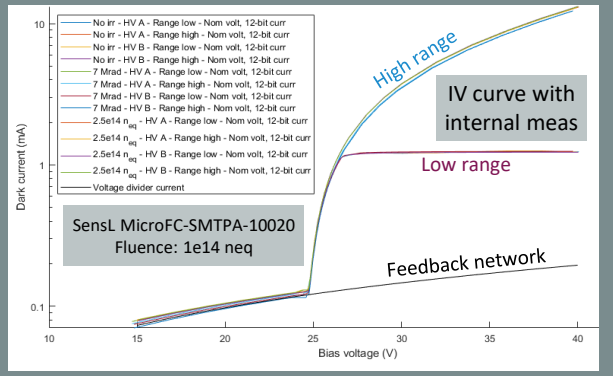


Load regulation









Radiation hardness

Irradiation performed in several facilities

- TID: KIT (ambient T) and CERN (cold T)
- Neutrons: LENA and JSI
- Heavy ions: LNL

Radiation levels at 3000 fb^{-1} in CMS BTL		
TID	Neutron fluence	Ch. hadron fluence
3.2 Mrad	1.9e14 n_{eq} cm^{-2}	1.5e13 cm^{-2}

Radiation hardness – TID

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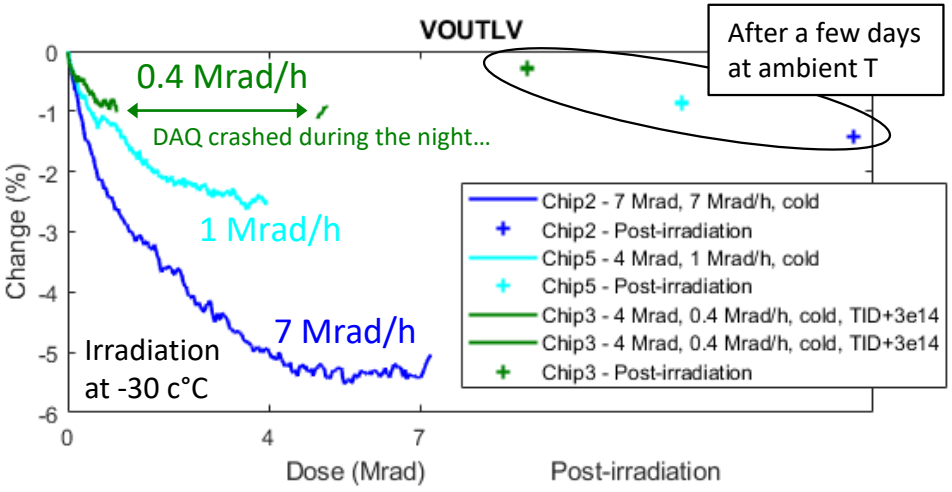
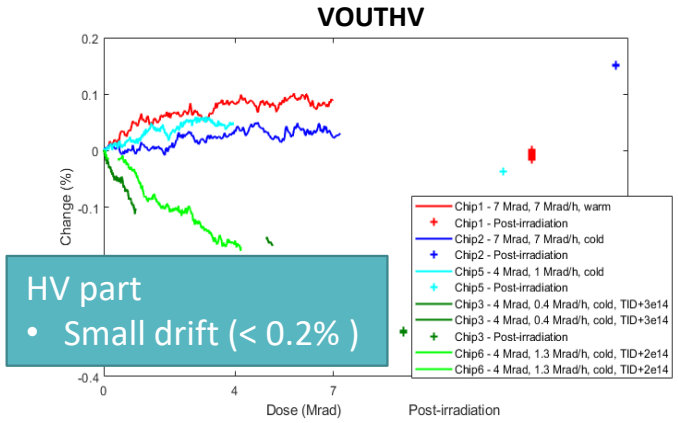
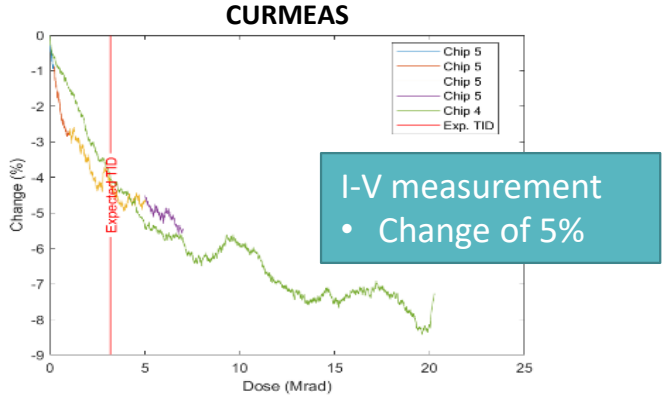
LV part
- Small drift (~ 1%)
- Clear effect of dose rate and annealing





HV part
- Small drift (< 0.2%)



I-V measurement
- Change of 5%

Radiation hardness – TID

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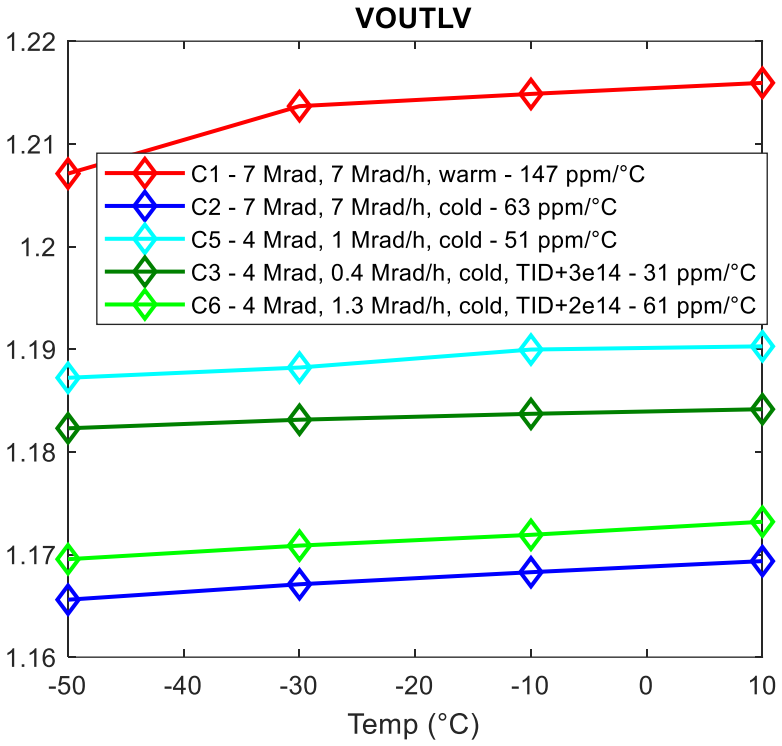

- Typical thermal stability before irradiation 50 ppm/°C
- Irradiation does not significantly affect thermal stability

Radiation hardness – Heavy ions

Irradiation performed in several facilities

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Radiation levels at 3000 fb^{-1} in CMS BTL		
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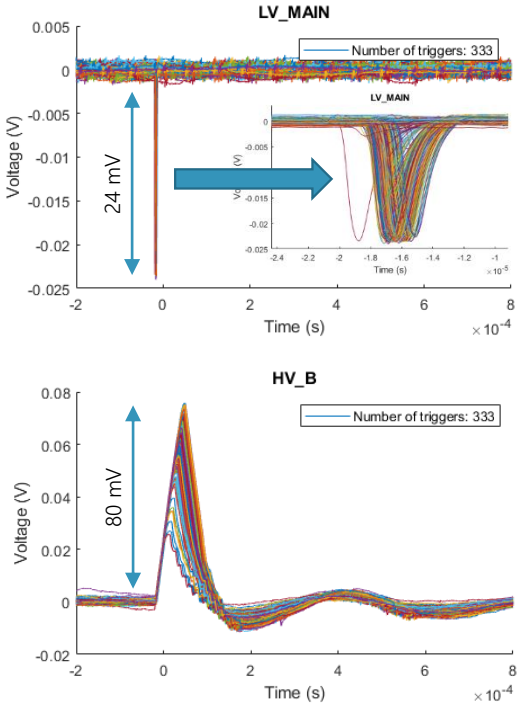
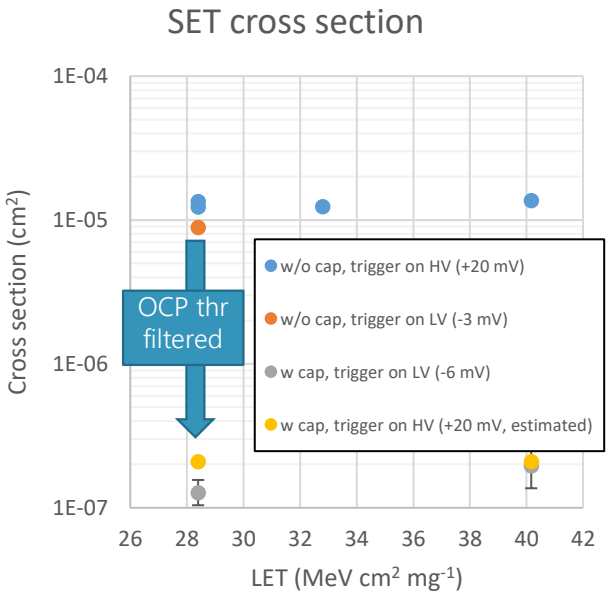


- Single event transients (SET) observed
- Cause: OTP circuitry (comparator)
- Mitigation: more filtering of OTP threshold
- Extrapolation with conservatively low threshold LET (1 MeV cm^2 mg^{-1}) gives a SET rate of 10 mHz in whole BTL
- Further mitigation: FE ASIC can disable OTP circuitry by software

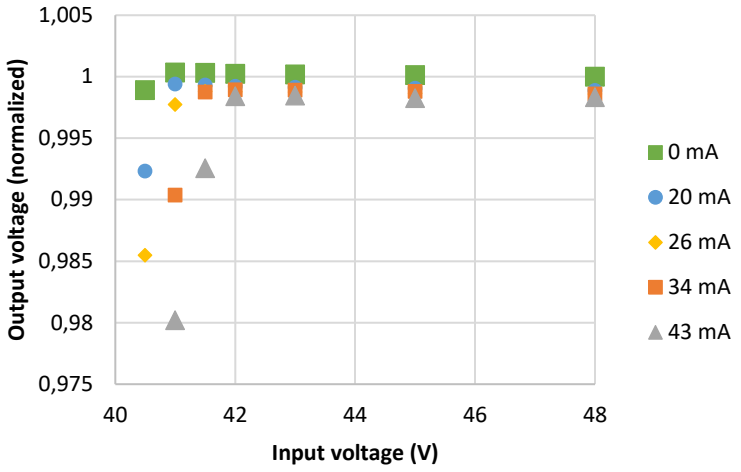
Take-home-message with SET: Be careful with high-gain, high-bandwidth and open-loop circuits



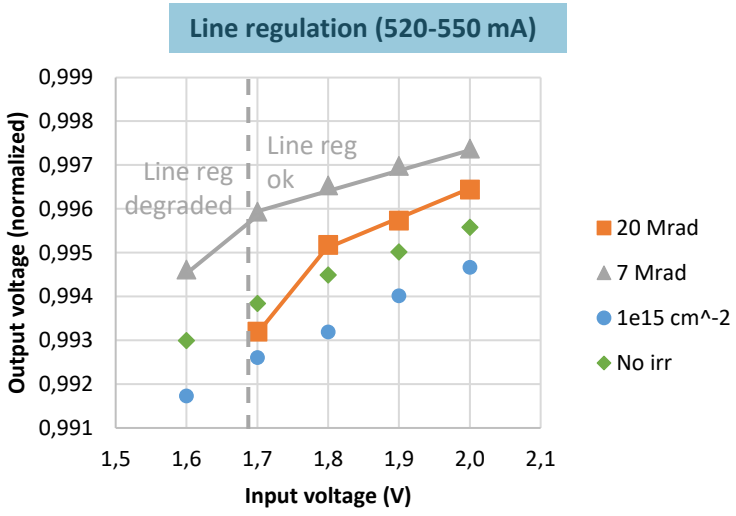
Line regulation – post-irradiation

- Radiation damage **degrades line regulation**
- LV part
  - Most critical because bPOL output is fixed during operation
  - At 7 Mrad and full load (520 mA), line regulation starts degrading when input voltage gets below 1.7 V (500 mV dropout)
  - Final choice for BTL: **600 mV dropout (1.8 V ALDO input voltage)**
- HV part
  - Less critical because dropout can be adjusted on PSU
  - Min dropout: **2-3 V at detector EOL, >90-95% efficiency**
  - Large **degradation** in HV PMOS R_{on} **at 1e15 n_{eq} cm^{-2}** (x5 above EOL level)

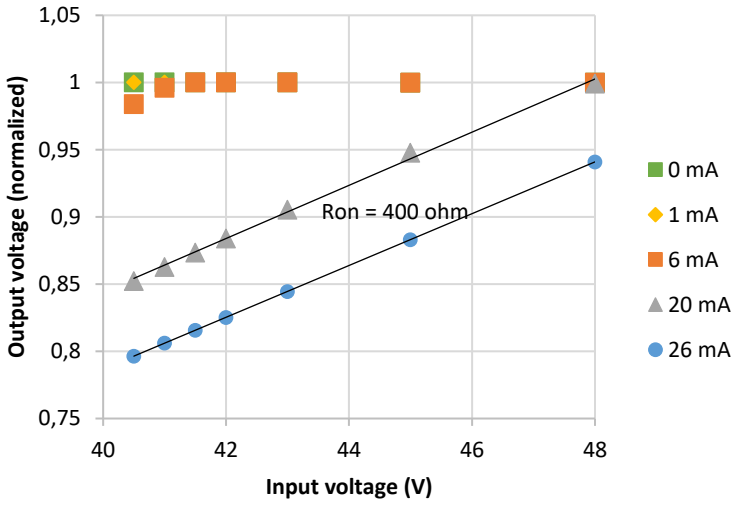
Line regulation (40 V, 2.5e14 neq cm-2)



Line regulation (520-550 mA)



Line regulation (40 V, 1e15 neq cm-2)



Yield and testing

- 552 ALDO2v2 measured in a test socket
  - Samples picked randomly from the full production
- LV part: 100% yield
- HV part:
  - 99.5% yield when counting partially working chips (e.g. with one channel that is always enabled)
  - 99.1% yield when counting only fully working chips
- Final decision: no individual chip testing, chips tested on FE PCB (with 2 ALDOs, exp yield >98%)

Testboard with QFN64 socket

Summary

- We have developed ALDO2, a multi-function rad-hard ASIC for the power management of SiPM-based HEP experiments
- Performance was validated over the course of 4 years of development, laboratory measurements and detector integration
- Radiation hardness was fully qualified up to 20 Mrad, 1e15 n_{eq} cm^{-2} and heavy ions
- Full production has been completed, 45k chips produced
- ALDO2 is ready to be installed in two CMS detectors, BTL and HGCAL

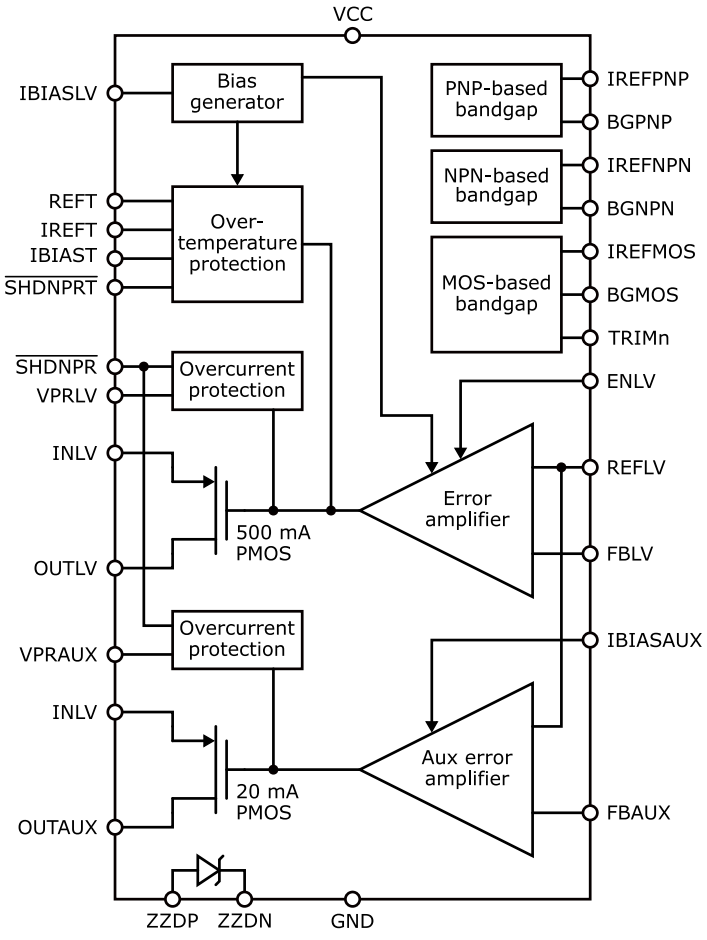
Future prospects

- A possible ALDO3 would likely include DAC for bias adjustment, ADC for monitoring, and digital logic
- onsemi I3T80 fab2 (used for ALDO2) closed in 2022
  - I3T80 still available in US fab, not yet qualified for radiation
  - Availability through Europractice uncertain
- Alternative rad-hard HV technologies could be investigated

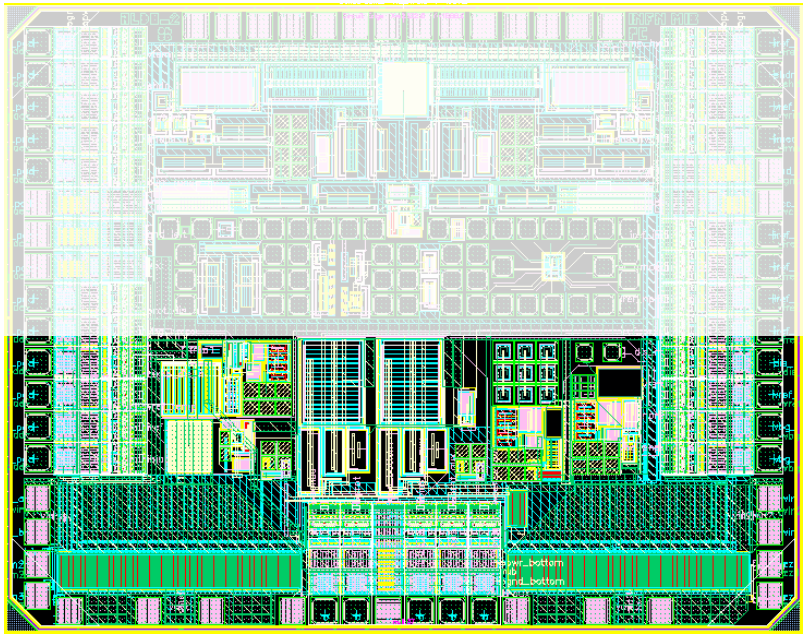
Thanks for your attention

Backup

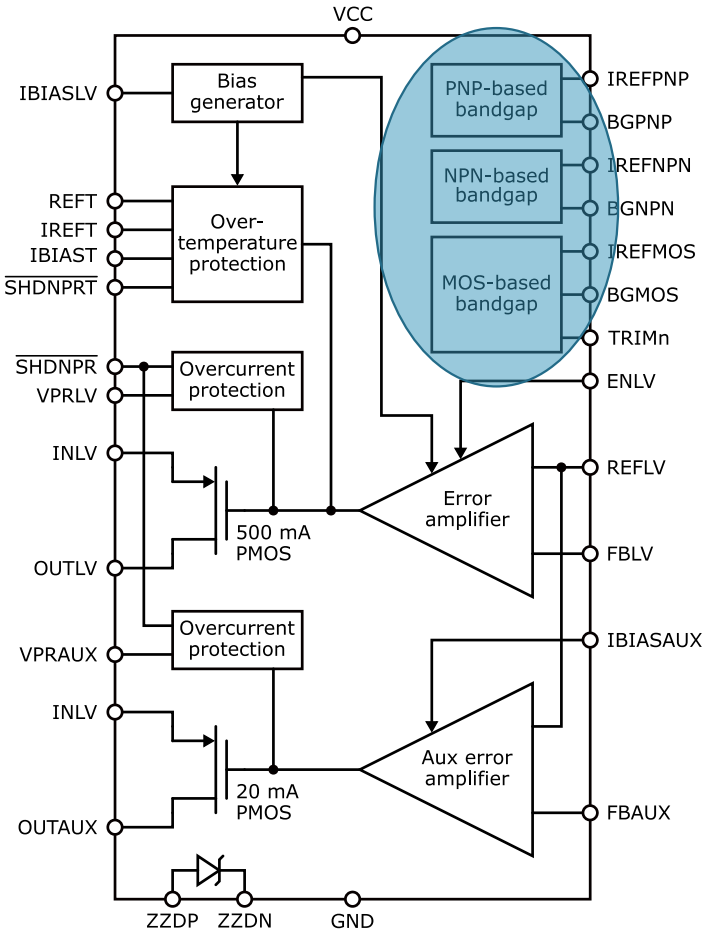
LV part (1)



- The LV part is completely independent from the HV part (this is the case when used with GBT-SCA)

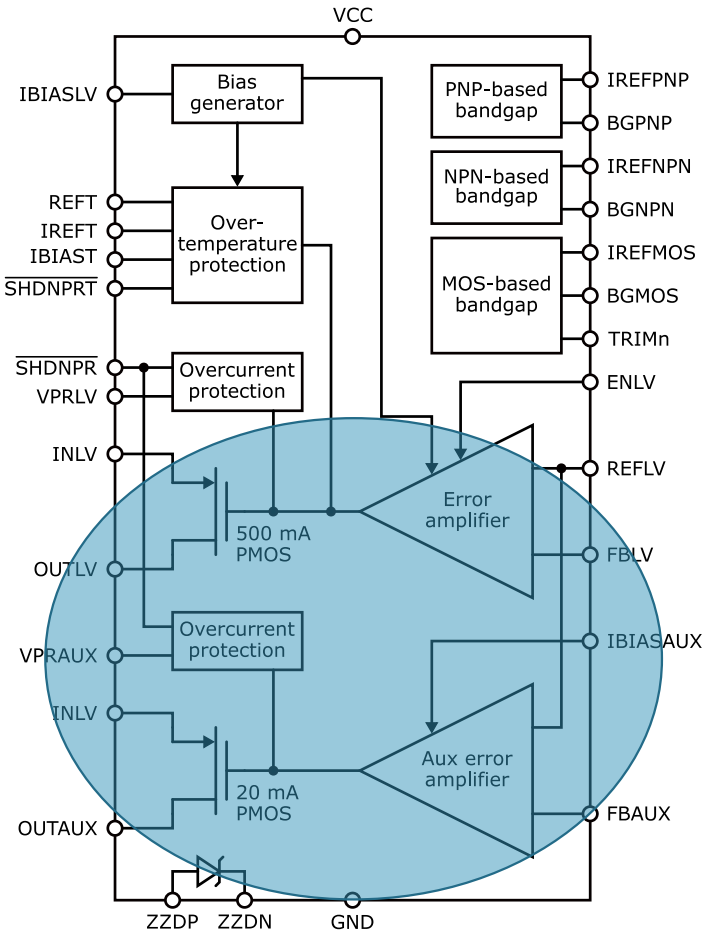


LV part (2)



- Three bandgaps included (only one selected in final application)
  - PNP-based
  - NPN-based
  - MOS-based
- The reason for this is that the expected radiation levels are right on the edge where bipolar-based bandgaps could still be used (and they offer superior stability)
- MOS-based bandgap can be trimmed to compensate corner spread and/or simulation mismatch due to the use of ELTs
  - «Passive» trimming: acts directly on bandgap resistors (resistors can be shorted externally to slightly tune the gain of the bandgap)
  - 4 bits, ~8 mV LSB (± ~10% trimming wrt 630 mV)
  - The trimming strategy relies on the fact that trimming can be done on a wafer-by-wafer basis

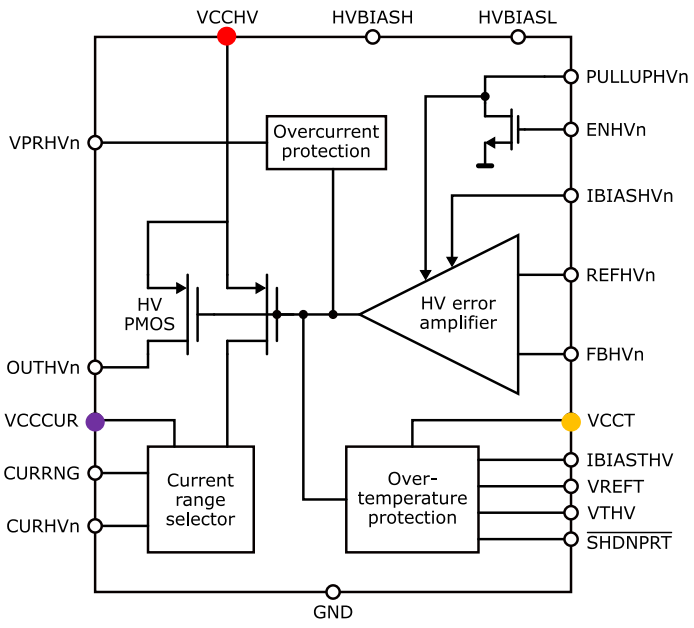
LV part (3)

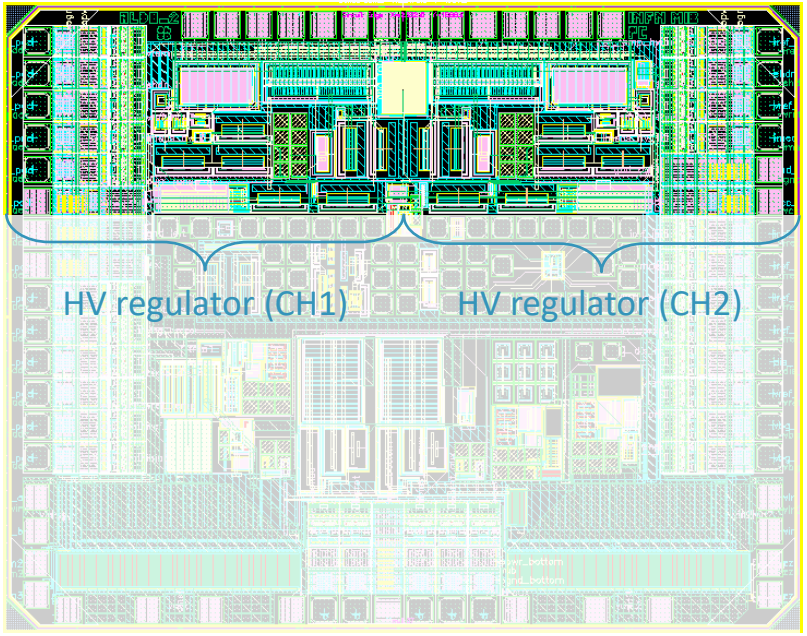


- In addition to the main regulator (0.5 A) there is also an auxiliary one (max 20 mA)
  - This was originally intended to provide an external voltage reference to the front-end ASIC
  - It is also used to generate the voltage reference for the over-temperature protection
- The design of the LV error amplifiers is quite standard
  - Typical closed-loop gain: 1-2
  - Loop gain: 54 dB
  - Single-stage “mirrored” amp, NMOS input
- Output voltage is adjustable by changing feedback resistors
- Any bandgap can be selected as input of the voltage reference
- Compensation on output node with low ESR tantalum capacitors
- Overcurrent protection is also very similar to HV part

HV part – Power domains

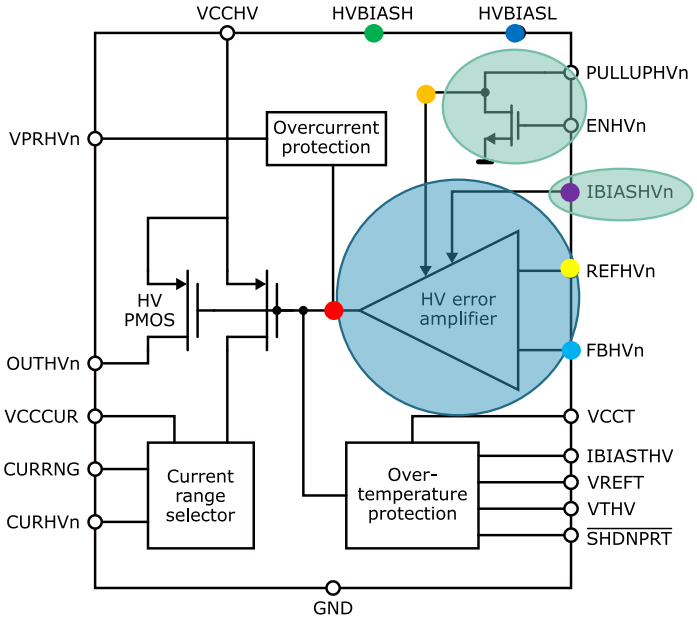
- The HV part is completely independent of the LV part
- Aux circuitry of the HV part has its own LV power domains
- No power-on sequence is required

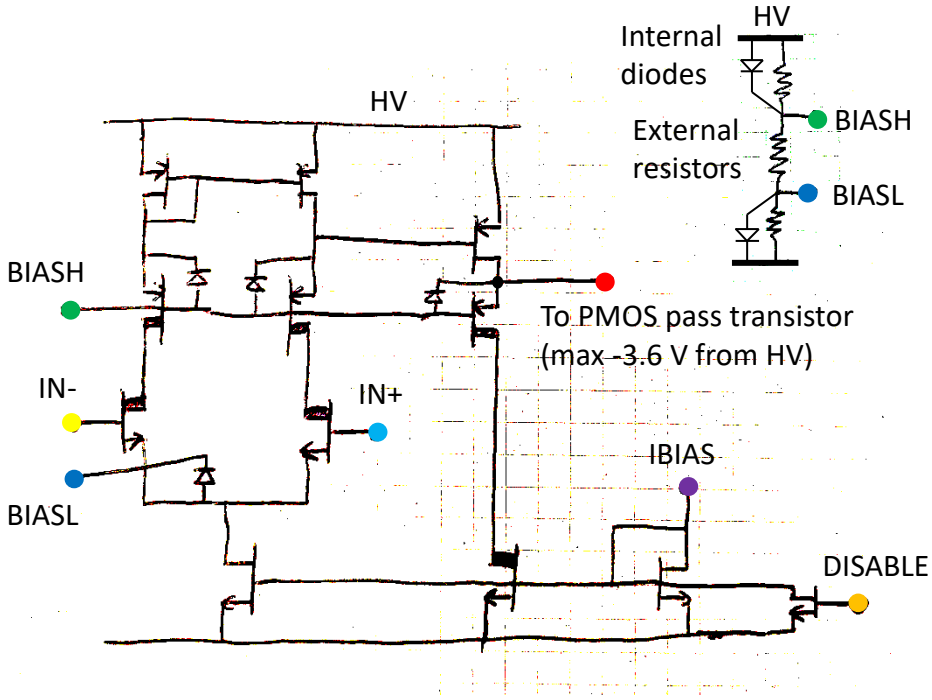




HV part – Error amplifier (2)

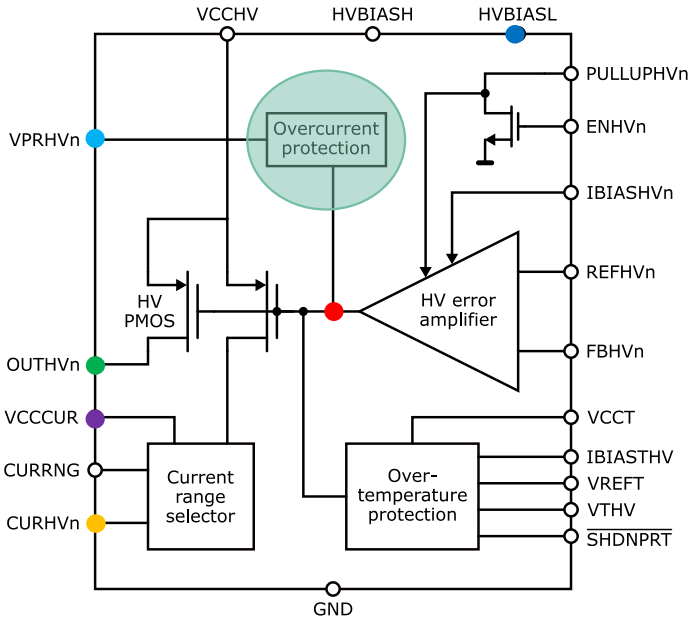
- The regulator can be disabled (default off)
- Bias current is provided externally (not from bandgap) to keep LV and HV independent

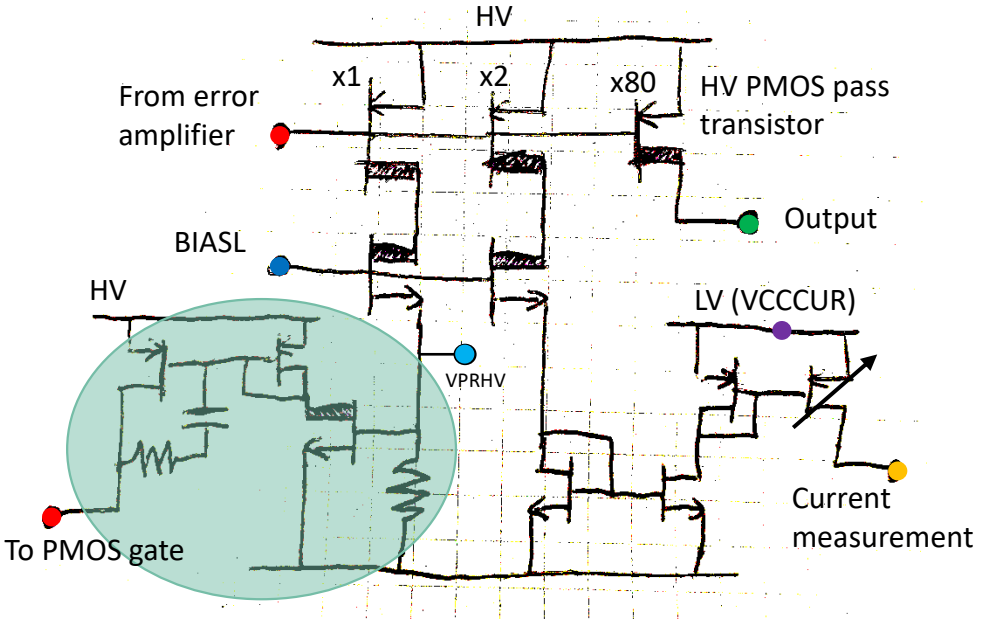




HV part – Overcurrent protection

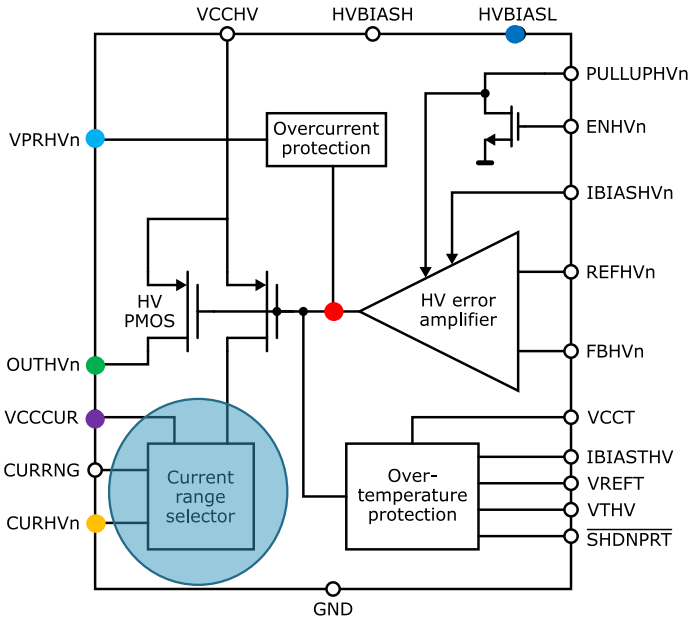
- The overcurrent circuit compares the output current to a gate threshold
- The error amplifier is disabled if current gets too high
- Current limit is constant (no foldback, operates together with over-temperature)

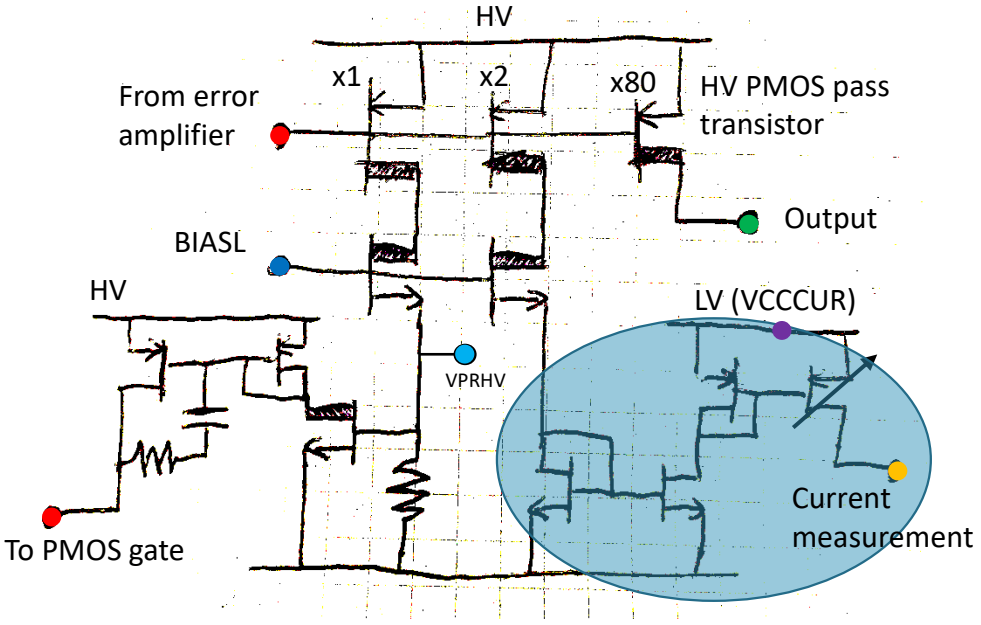




HV part – Output current measurement

- The current measurement circuit further mirrors the output current
- The ratio is tunable (1/40 and 1/800), adapting to BOL and EOL conditions
- An external resistor converts the output current to a voltage, matching the ADC full-range and SiPM specs



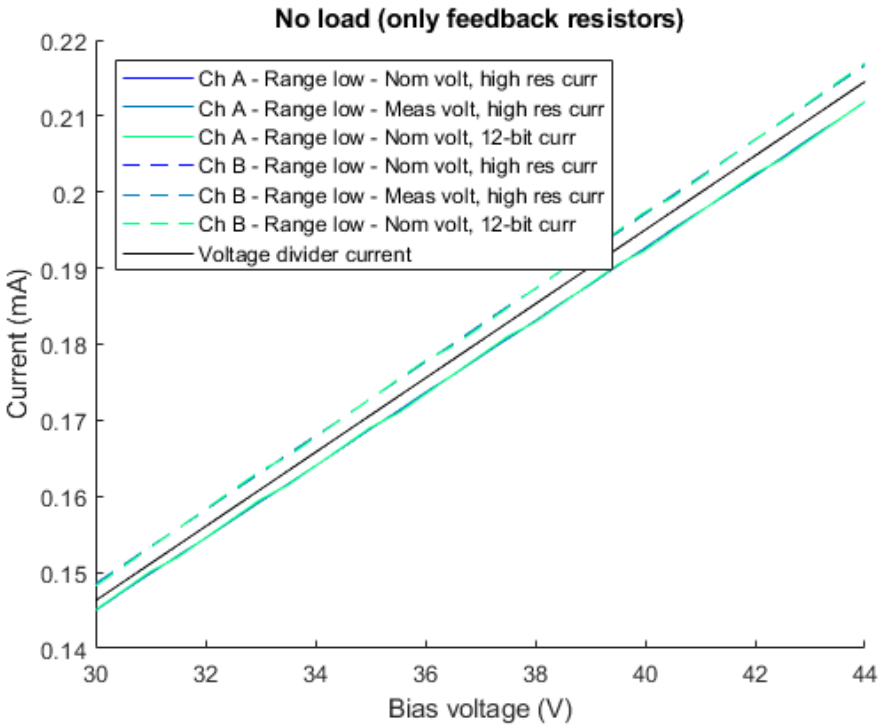


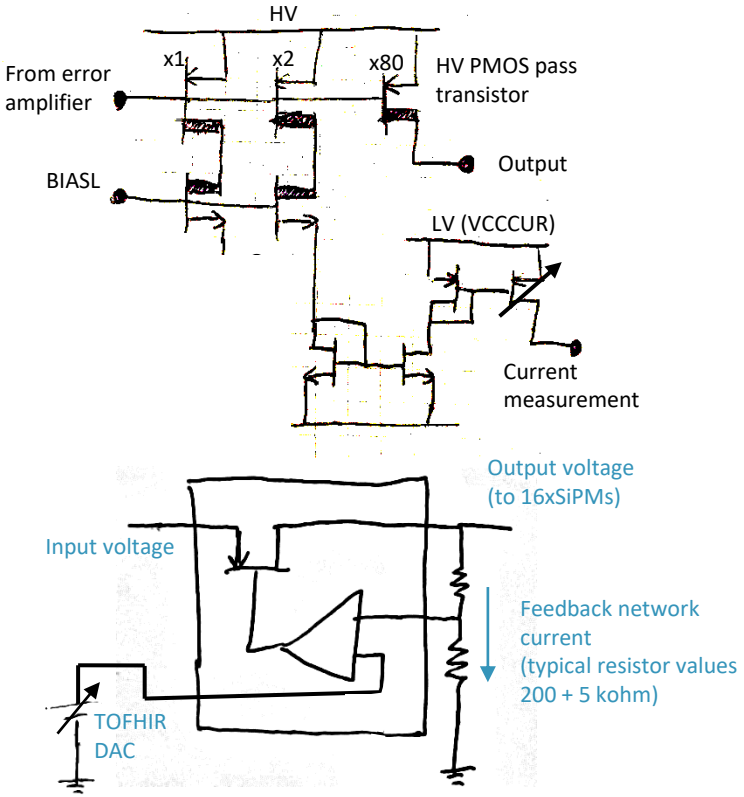
Tantalum capacitors

- For the stability, both HV and LV regulators rely on low ESR tantalum capacitors on output nodes
- Radiation hardness is not a problem
  - Used widely in space applications due to they higher reliability and compact size
  - Sensitive to humidity
    - No problem in HEP detectors where ambient is controlled
  - Tested up to 5 Mrad (https://core.ac.uk/download/pdf/227725417.pdf)
- Several models available for LV in small packages (22-100 µF, ESR < 200 mohm)
- Less models for HV ones
  - 50 V/63 V capacitors are thick
  - Selected model: KEMET T521V106M050ATE090 (50 V, 10 µF, 90 mohm ESR, height 1.8 mm)
  - Costly

Accuracy of I-V curves

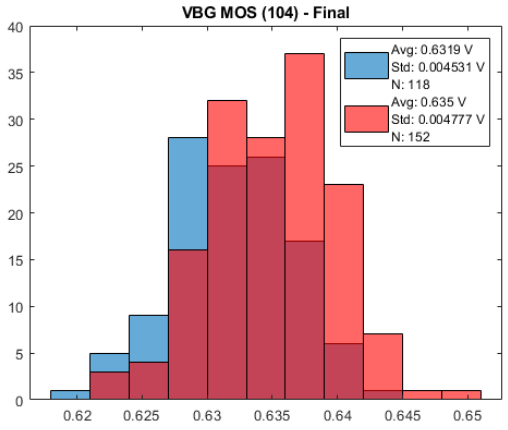
- The I-V curve with no load (only feedback resistors) shows that the accuracy of the current measurement circuitry is as expected from simulations and previous measurements (<2% spread)

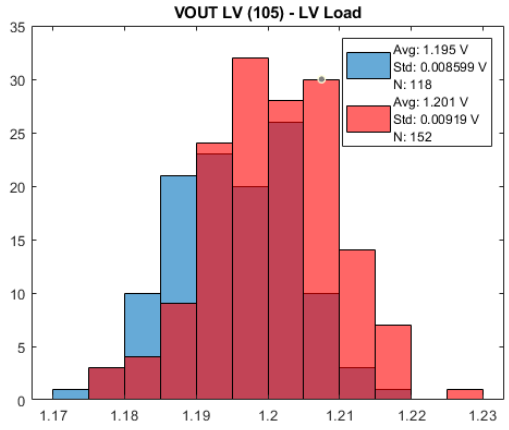




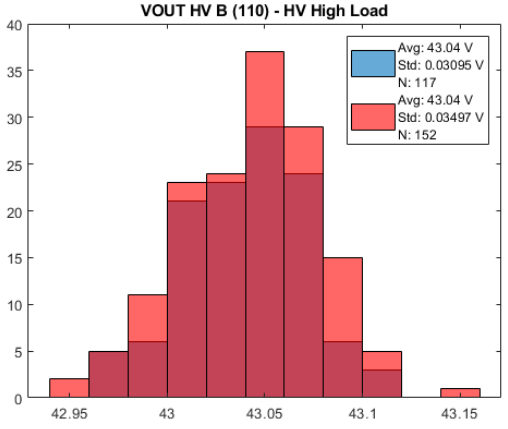
Spread

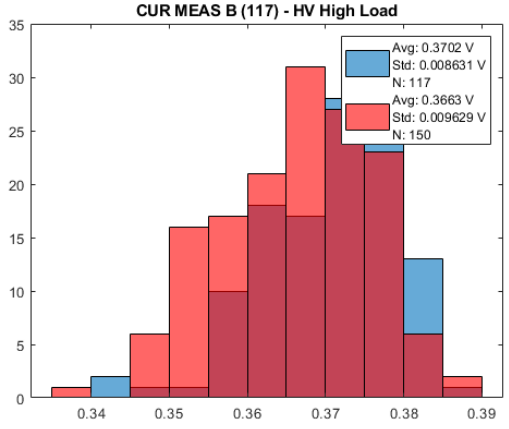
- Spread from the whole production (ALDO2v2) is small, no need for bandgap trimming
  - 0.7% RMS on bandgap/LV regulator





  - <0.1% RMS on HV regulator





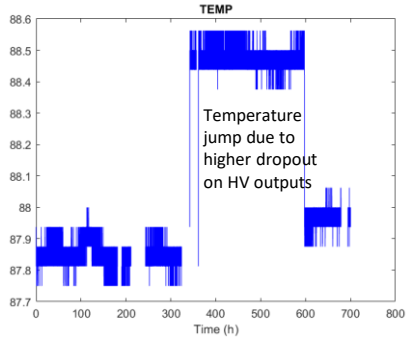
Blue:
ALDO2v2 from same wafer

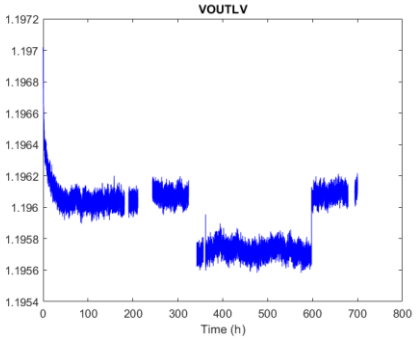
Red:
ALDO2v2 sampled randomly from 6 wafers

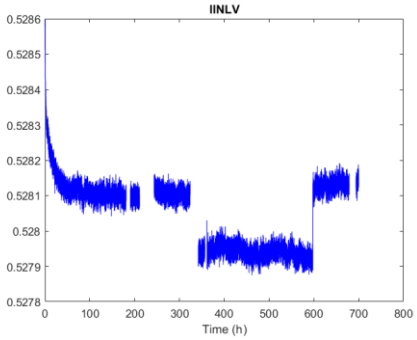
Accelerated aging

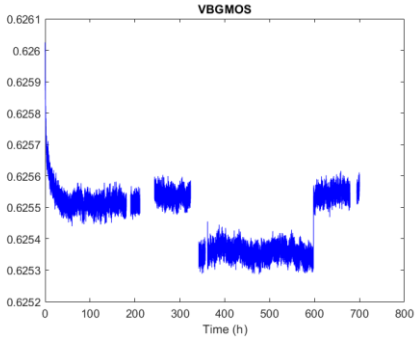
- Accelerated aging using Arrhenius equation gives x2 acceleration factor every 10 °C increase
- 10 years of operation can be accelerated to 1 month if temperature is set 70 °C above operating temp
- In BTL operating temperature will be -30 °C

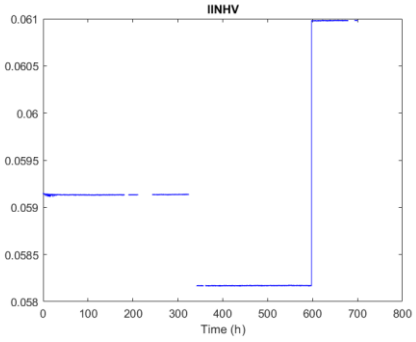
- We decided to perform accelerated aging at 80 °C
- Input voltages: 1.8 V and 45 V, output voltages: 1.2 V and 42 V (40 V), nominal load currents: 500 mA and 30+30 mA
- Run fine for >700 hours (30 days), with 1 chip
- Temperature with on-board thermometer: 88 °C

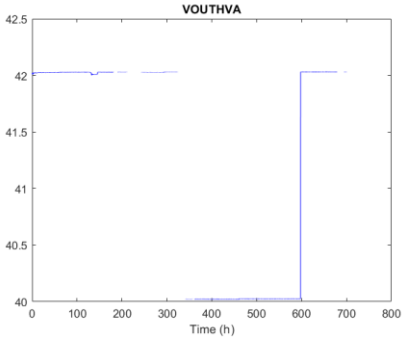


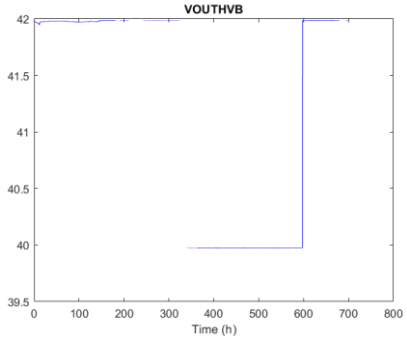


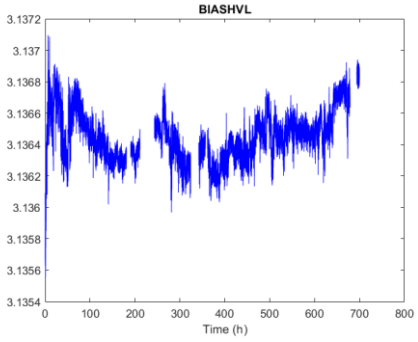






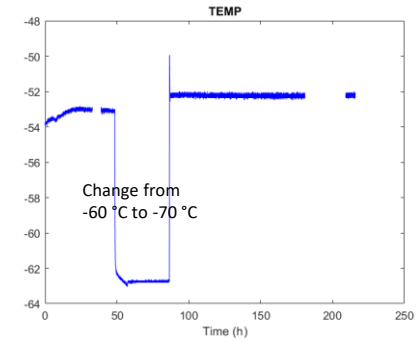


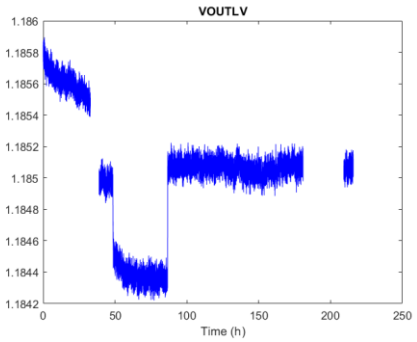


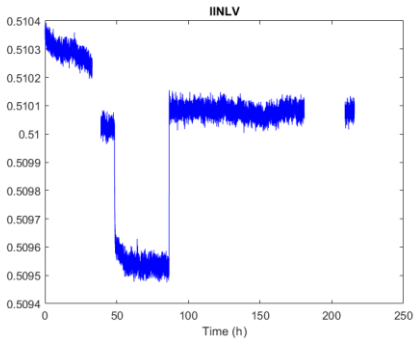


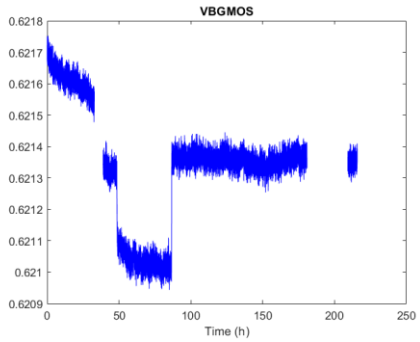
Operation at extremely low temperature

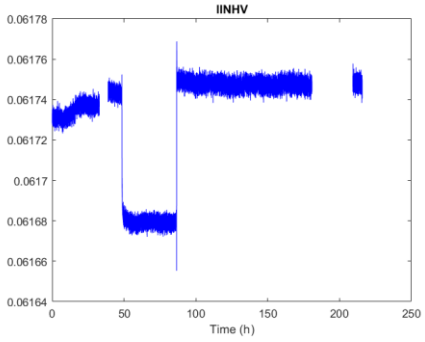
- We tried to do the same thing at low temperature (climatic chamber at -60 °C and -70 °C)
- Run fine for 240 hours (10 days), with 1 chip
- Temperature with on-board thermometer: -52 °C or -63 °C

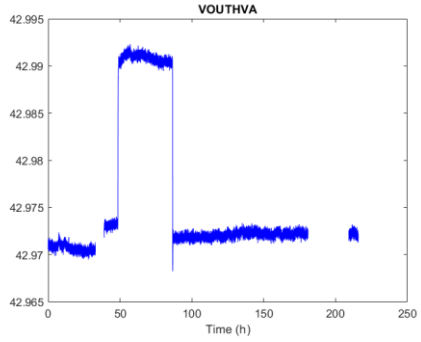


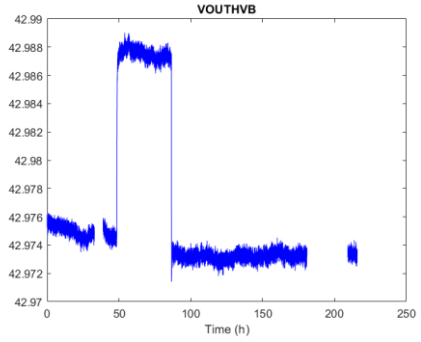


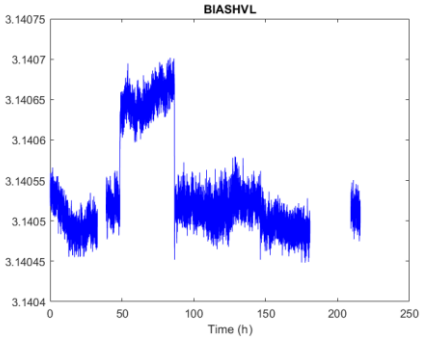






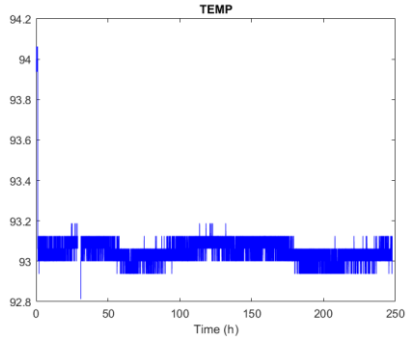


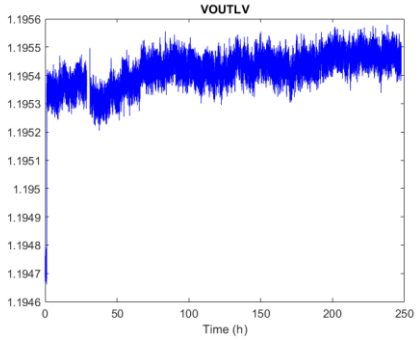


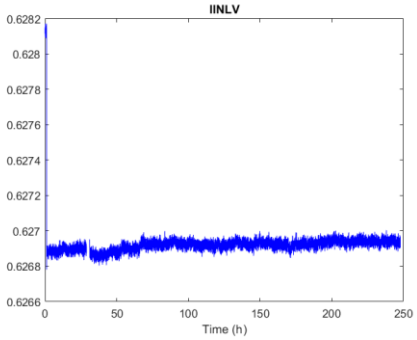


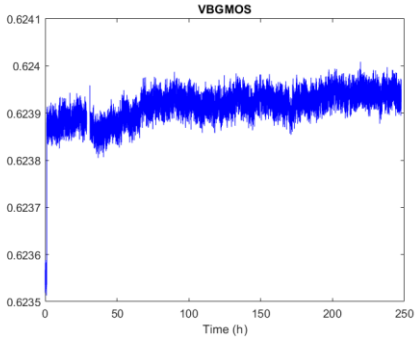
Operation beyond specs

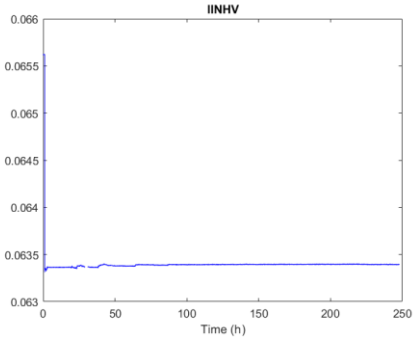
- What happens if the chip is operated beyond specs?
- We increased the temperature to 90 °C, increased input voltages to 2.5 V and 50 V. Now BIASL voltage is at 3.5 V (beyond specs of diode-connected LV MOS and possibly beyond SOA of DMOS)
- Both regulators worked for 10 additional days

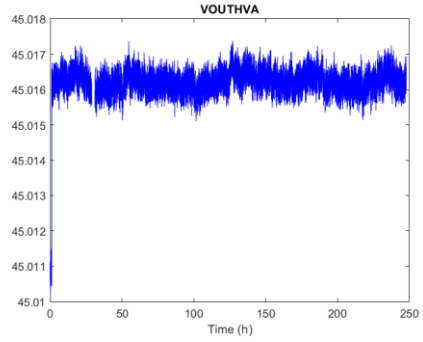


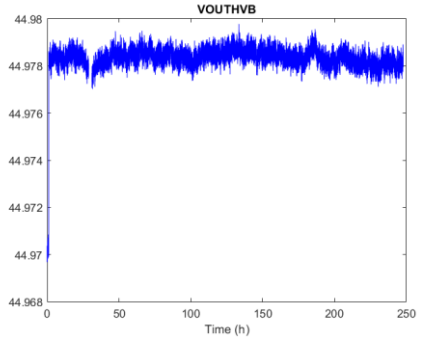


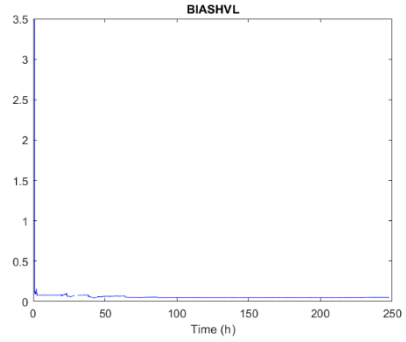






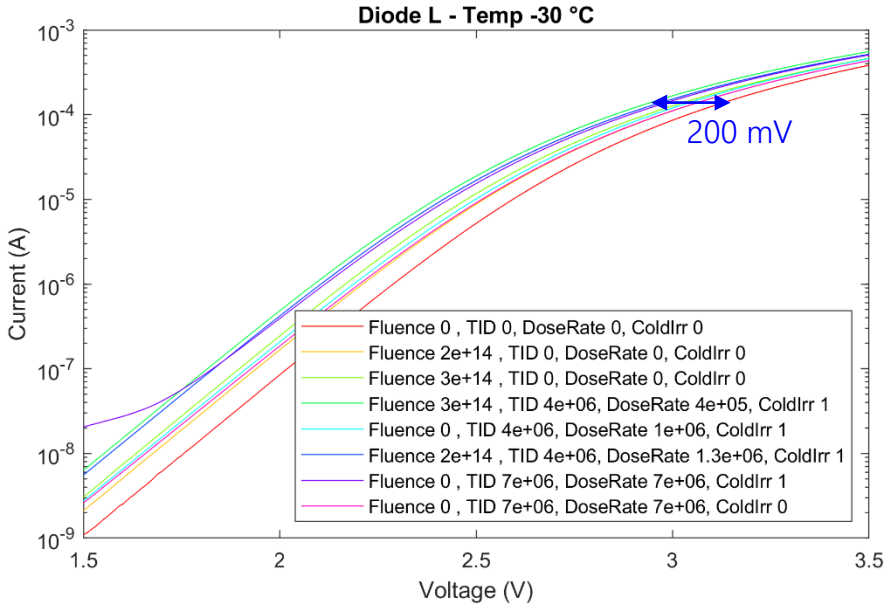


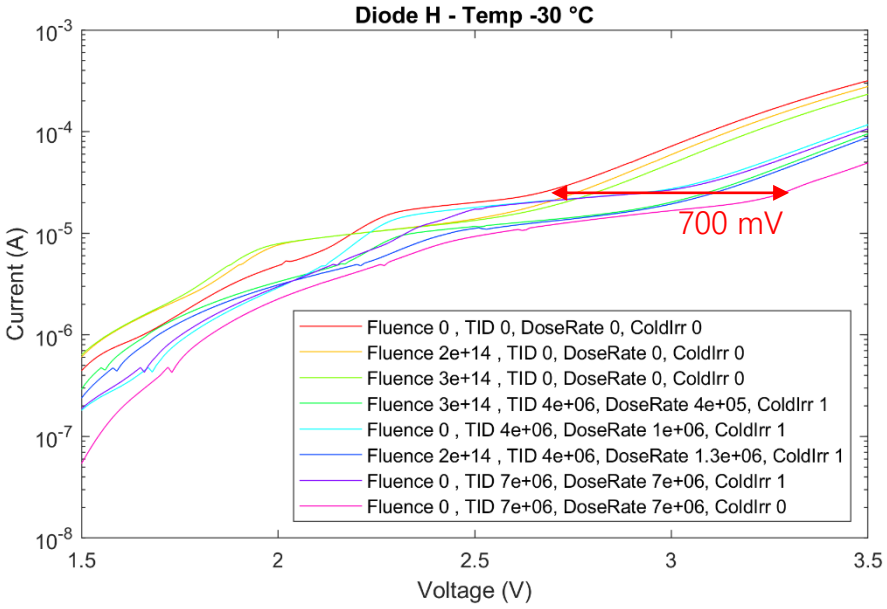




Biasing diodes – IV curves

- After irradiation, we measure the diode IV curves using a Keithley 4200 semiconductor analyzer at different temperatures (-50 °C to +70 °C)
- NMOS-based diode (diode 'L') has small drift due to radiation
  - Up to 200 mV voltage drift at fixed current
- PMOS-based diode (diode 'H') has significant drift
  - Up to 700 mV voltage drift at fixed current

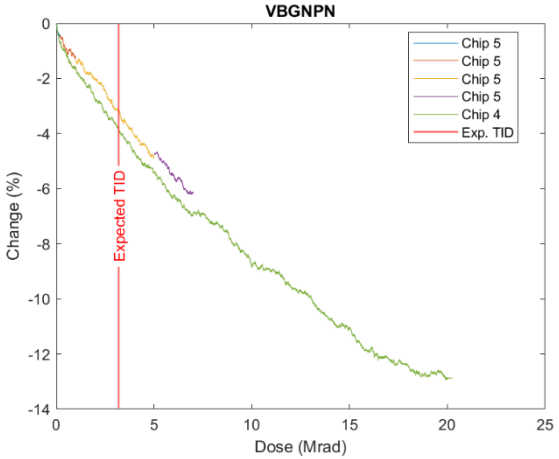


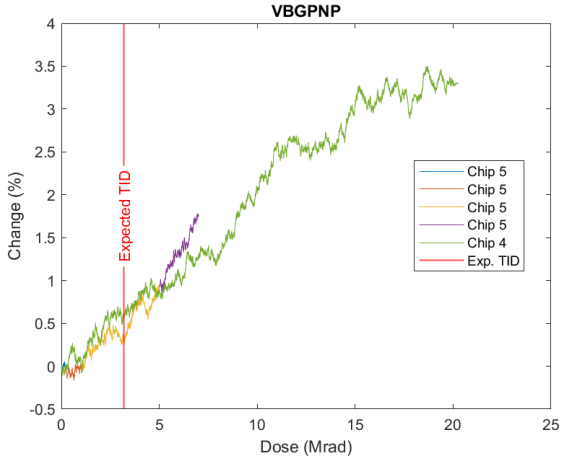


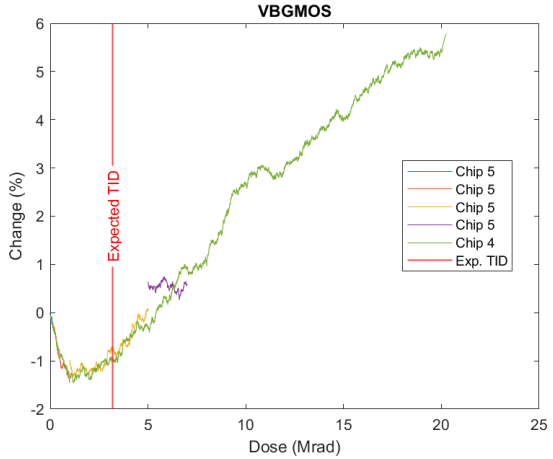
I3T80 Fab2 closure

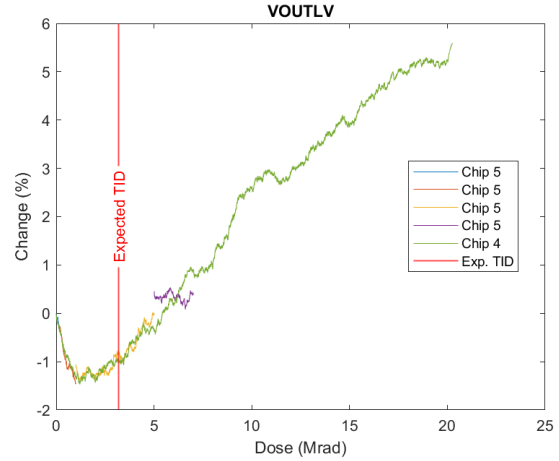
- I3T80 Fab2 in Oudenaarde (Belgium) was closed in June 2022
- There is a backup solution to Fab2: I3T80 fab in Gresham (USA)
  - 8-inch wafers
  - Different rules for metal slotting
  - Radiation hardness unknown
- In 2021 we did an MPW of ALDO2v1 in Gresham fab
  - Dies are unpackaged
  - Available for radiation hardness qualification
- Future MPW runs with Europractice uncertain

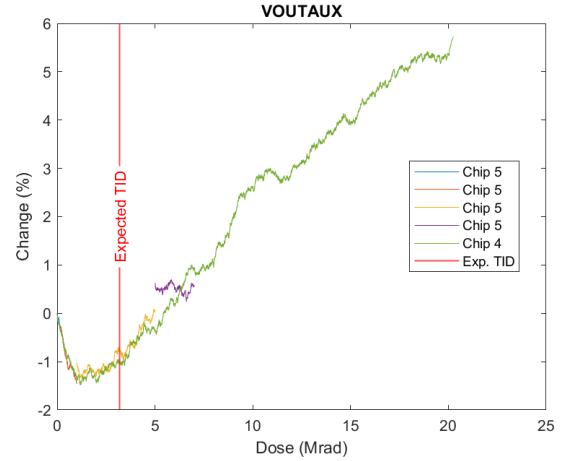
TID online monitoring - LV

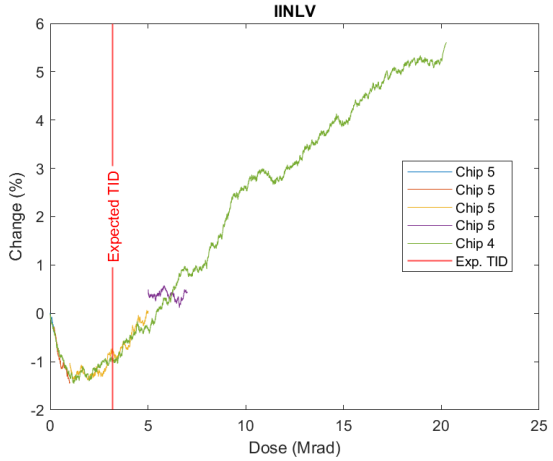






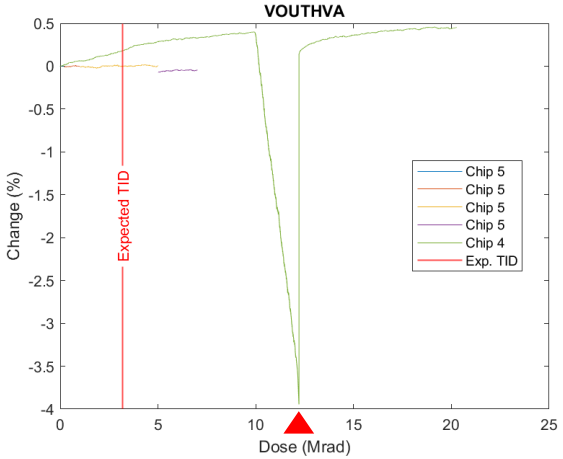


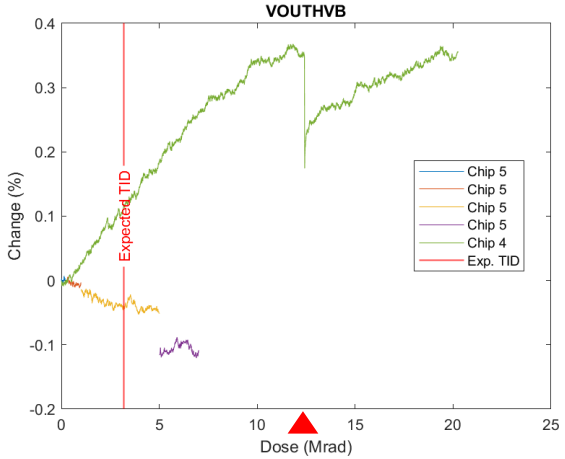


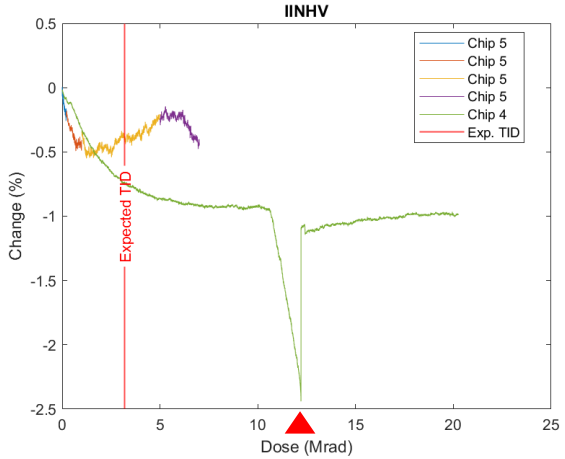


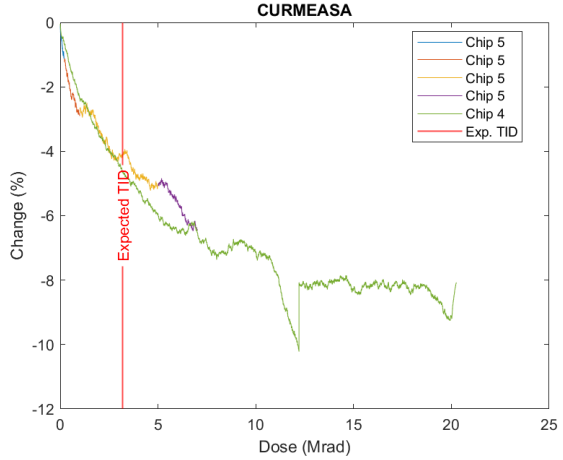
- LV regulator is fully operational up to 20 Mrad at ambient temperature and 520 mA load
- All three bandgaps are well within a few % range at 3.2 Mrad (PNP and MOS ones are better, <1%)

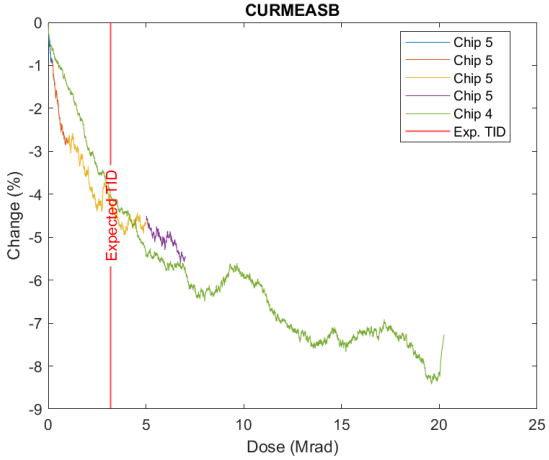
TID online monitoring - HV

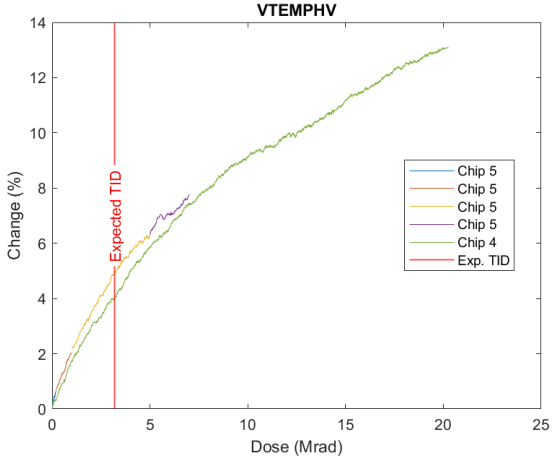








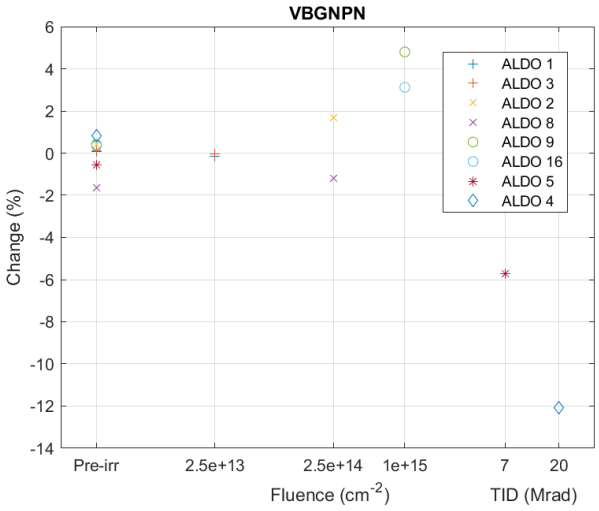


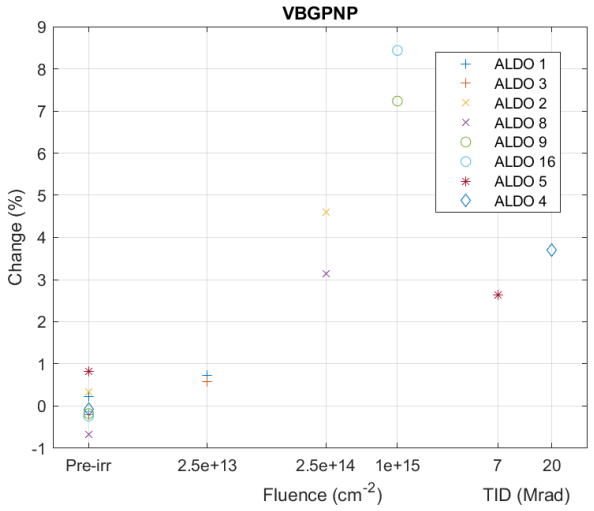


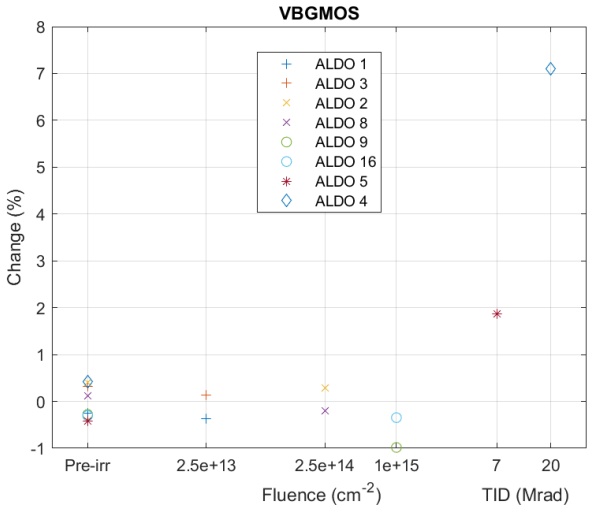
- HV regulator is fully operational up to 20 Mrad at ambient temperature and 20 mA load
- Channel A started working in current-limited mode at about 12 Mrad (marker: ▲), because the over-current limit lowered during irradiation. Recovered temporarily by switching off the over-current protection

Bandgap voltage references

- Bandgaps drifted by few percent after irradiations. All are well within usable range at nominal radiation levels
  - Best: MOS bandgap, Second best: PNP bandgap







NPN	Value	Var	T Drift
Pre-irrad	1.22 V	-	-100 ppm/°C
2.5e14 cm^{-2}	1.22 V	1%	-
1e15 cm^{-2}	1.27 V	4%	-270 ppm/°C
7 Mrad	1.15 V	-6%	-140 ppm/°C
20 Mrad	1.07 V	-12%	-200 ppm/°C

PNP	Value	Var	T Drift
Pre-irrad	1.17 V	-	-20 ppm/°C
2.5e14 cm^{-2}	1.21 V	3-4%	-
1e15 cm^{-2}	1.26 V	8%	150 ppm/°C
7 Mrad	1.2 V	2%	-10 ppm/°C
20 Mrad	1.21 V	4%	-40 ppm/°C

MOS	Value	Var	T Drift
Pre-irrad	625 mV	-	70 ppm/°C
2.5e14 cm^{-2}	625 mV	0%	-
1e15 cm^{-2}	621 mV	<1%	120 ppm/°C
7 Mrad	637 mV	2%	70 ppm/°C
20 Mrad	669 mV	7%	100 ppm/°C