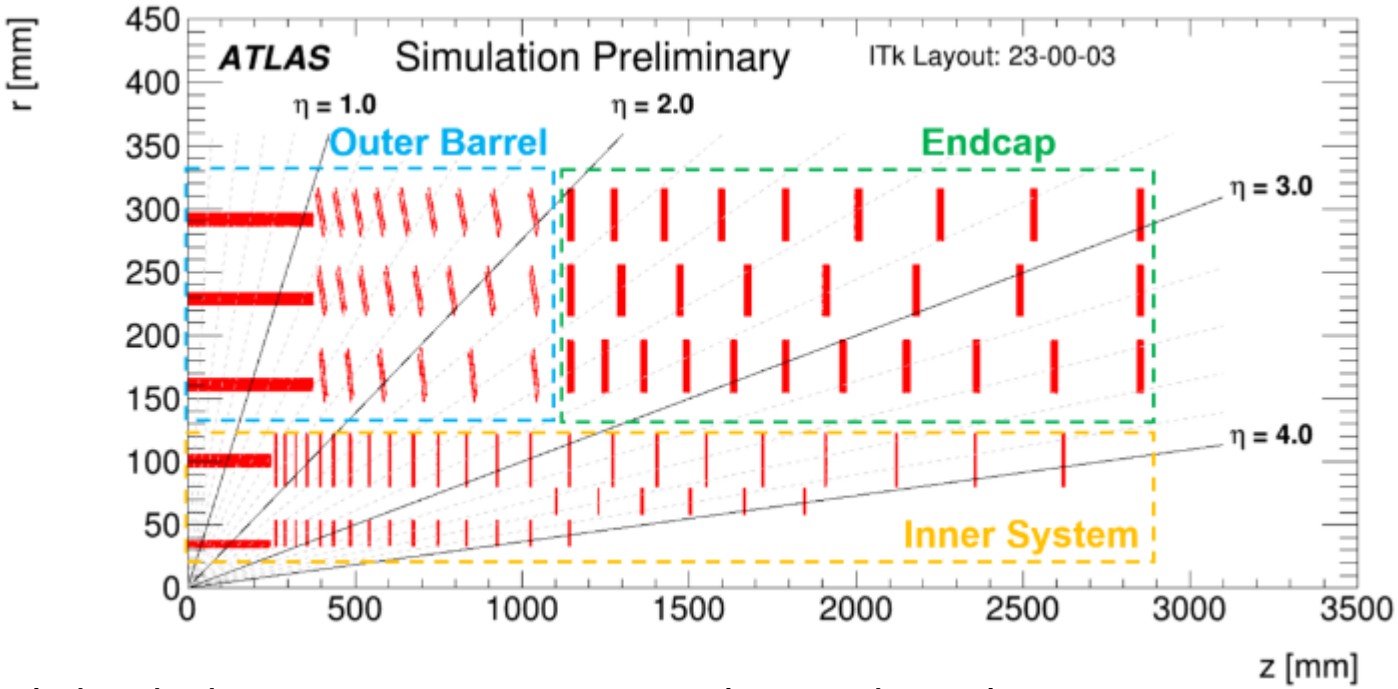
System tests of the ATLAS ITk planar and 3D pixel modules

TECHNOLOGY IN INSTRUMENTATION &
PARTICLE PHYSICS CONFERENCE
4th – 8th September 2023

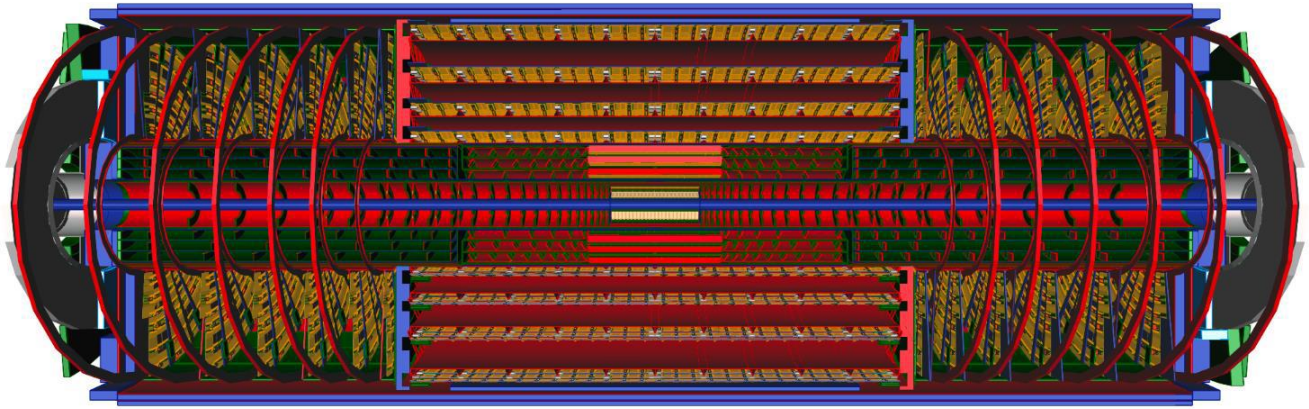
David Vázquez Furelos on behalf of the ATLAS ITk collaboration

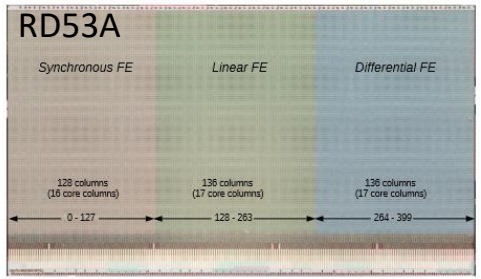
The Inner Tracker (ITk) pixel detector

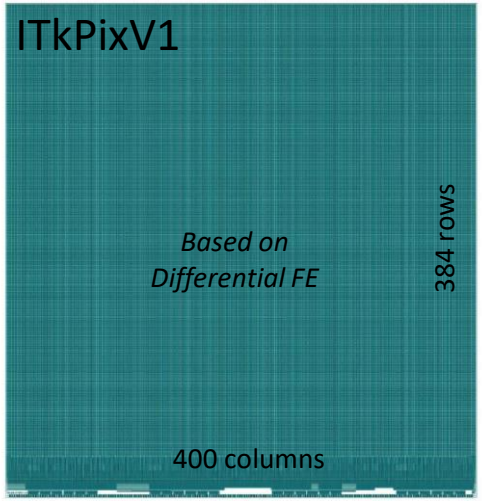


- The ITk is subdivided in 2 systems: Strip Tracker and Pixel Detector
- Pixel detector consists on 2 subsystems
  - Inner System (2 layers) → contains planar and 3D sensors
  - Outer System (3 layers) → contains planar sensors
    - Outer Barrel
    - Endcap
- Each subsystem is formed by different local supports, global supports, cooling and electrical service which are part of the system tests

System tests



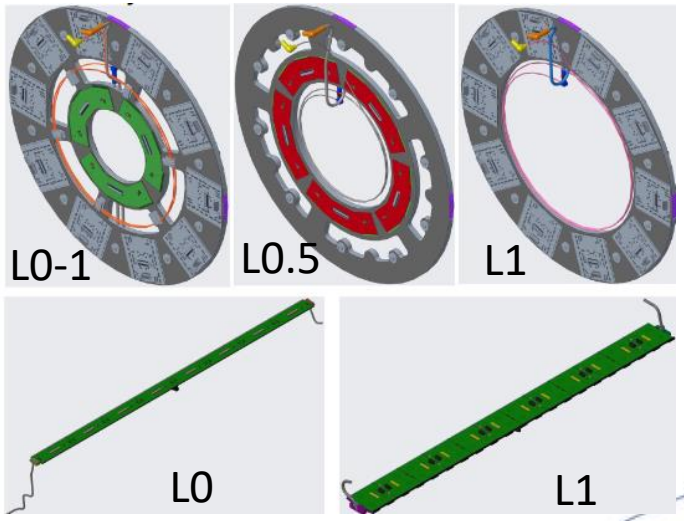




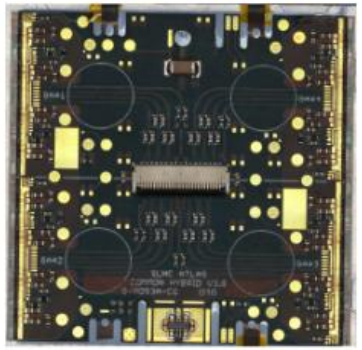
- The objective of the system tests is to validate the detectors working together and integrated in prototypes of the final detector
- The modules are connected in serial mode through serial power chains to reduce the amount of cabling needed
- The RD53A chip (400x192 pixels) is the first prototype of chip for ITk and it was used for the subsequent system tests (2x1.2 cm^2; 50x50 μm^2)
  - Three parts were tested and the differential FE was chosen to be used in the ITk
- ITkPixV1.1 (400x384 pixels) is the evolution of the RD53A chip and will be used in later prototypes for system test (2x2.1 cm^2; 50x50 μm^2)

Inner System

Inner System

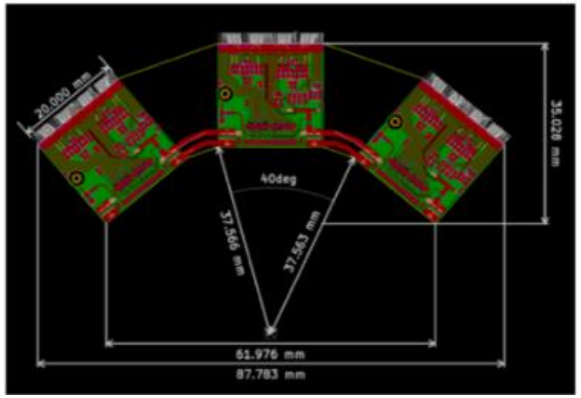


Layer 1-4 Quad



LinearTriplet Flex (Layer-0 barrel)

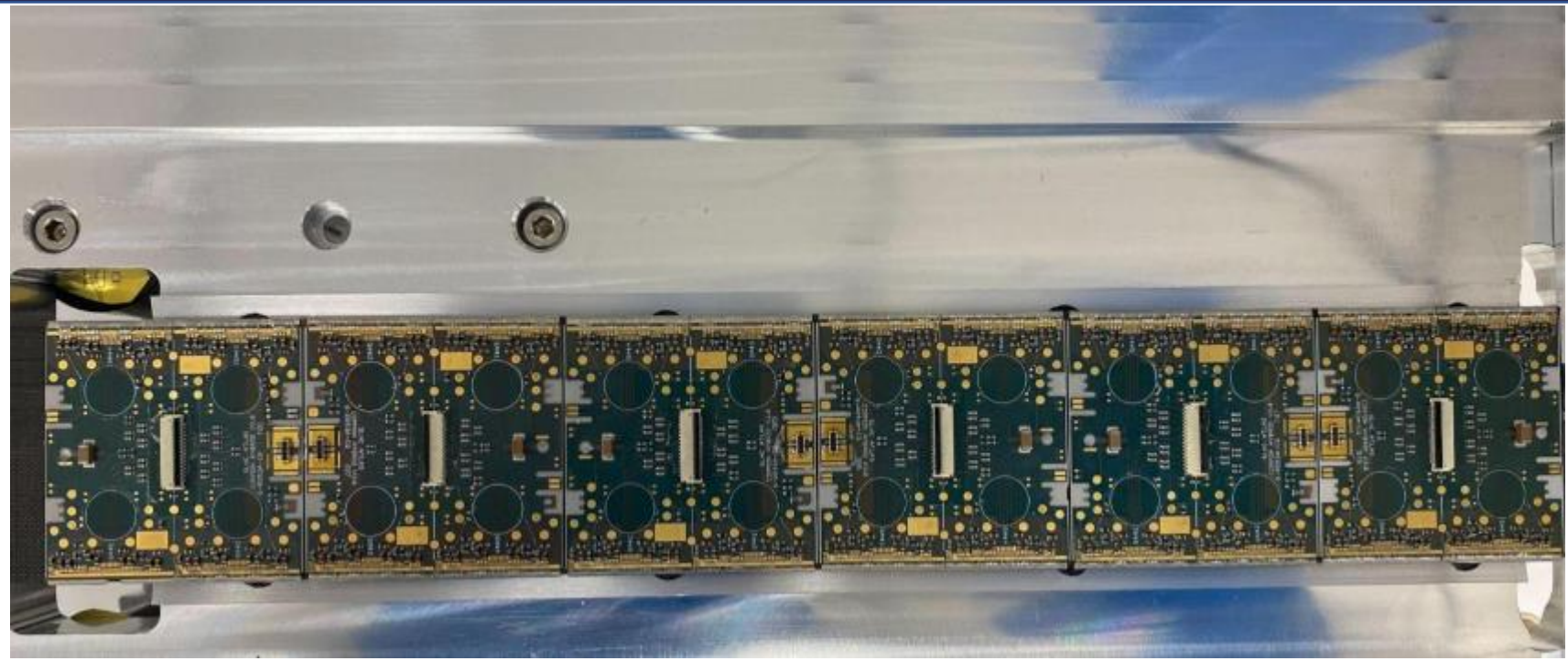
Ring Triplet Flex (Layer-0 rings)



- The inner system consists on two layers of staves and double sided rings on the endcaps
- The modules on innermost layer barrel and rings are mounted in Triplet Flex: 3 single modules in the same flex
- The other layers (barrels and rings) have quad modules: 1 large sensor connected to 4 readout chips

Inner System - Prototypes

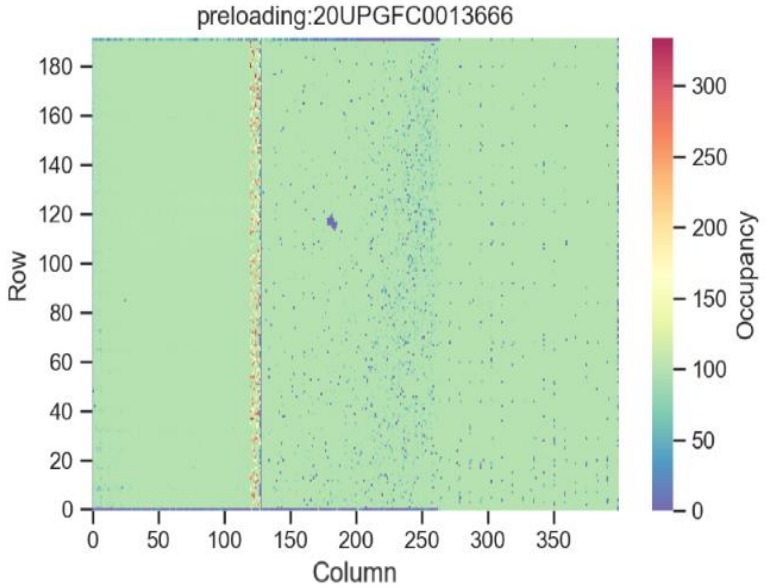
Prototype of one endcap L0-1 ring

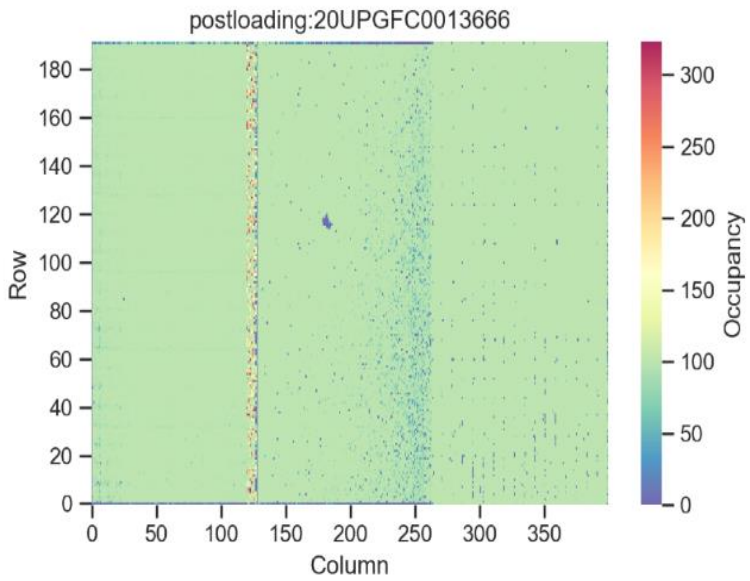


Prototype of half loaded L1 stave mounted on loading baseplate

- The modules tested in the endcap ring are 10 quad RD53A in the outer perimeter and 3 triplet RD53A in the inner
- The modules in the L1 stave are 6 quad RD53A
- Objective: characterize modules at different steps of loading to check if degradation occurs

Readout characterization - Ring L0-1

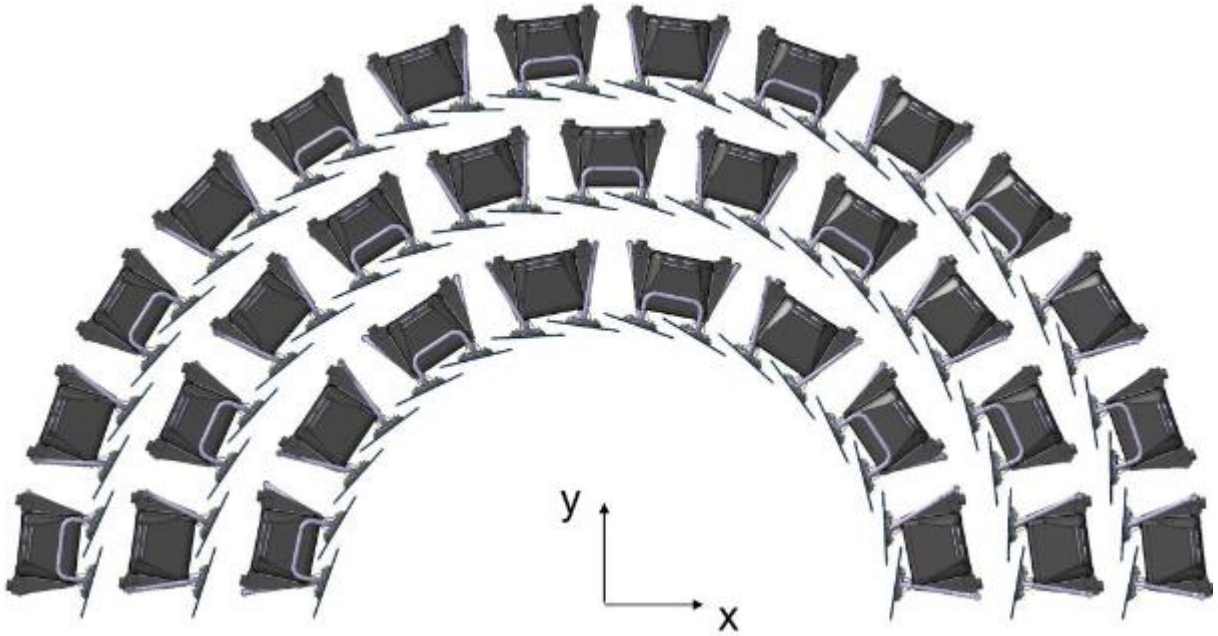




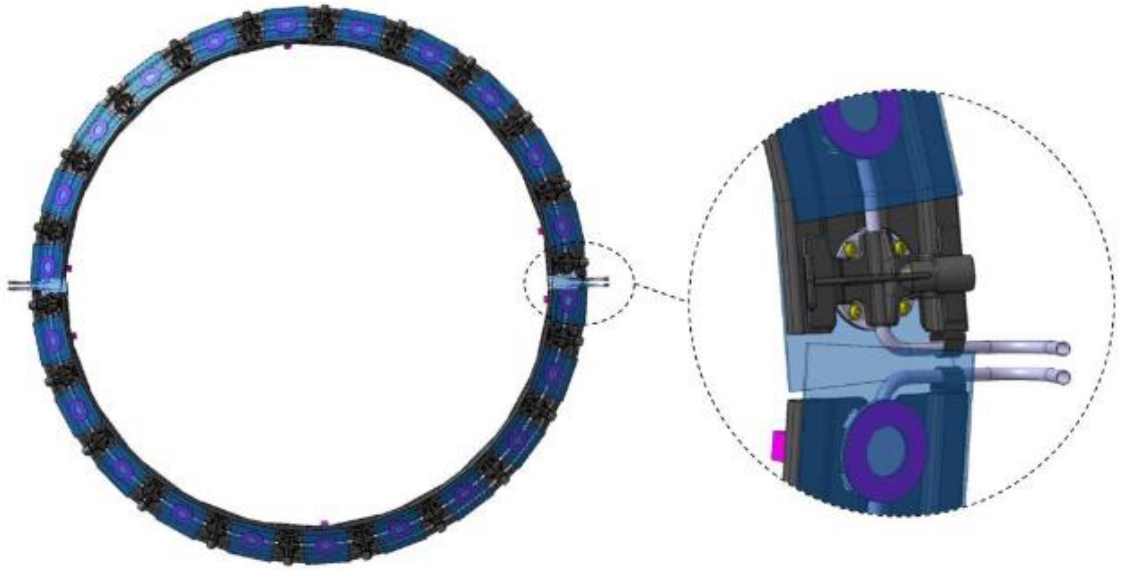
- The connection to the serial power chain is monitored for the 10 quads → all working
- Showing one representative module for digital scan → no signs of degradation during loading process
- All modules give similar results on digital/analog/threshold

Pixel Outer Barrel

Pixel Outer Barrel

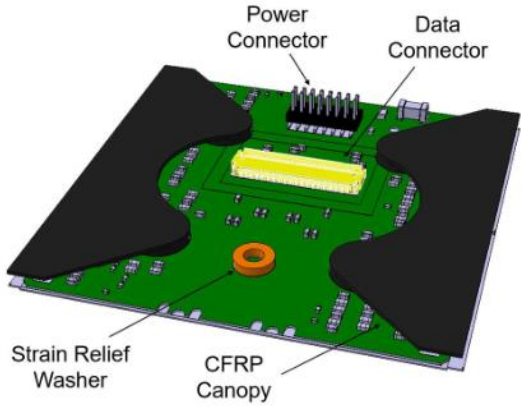


Front view of the longerons



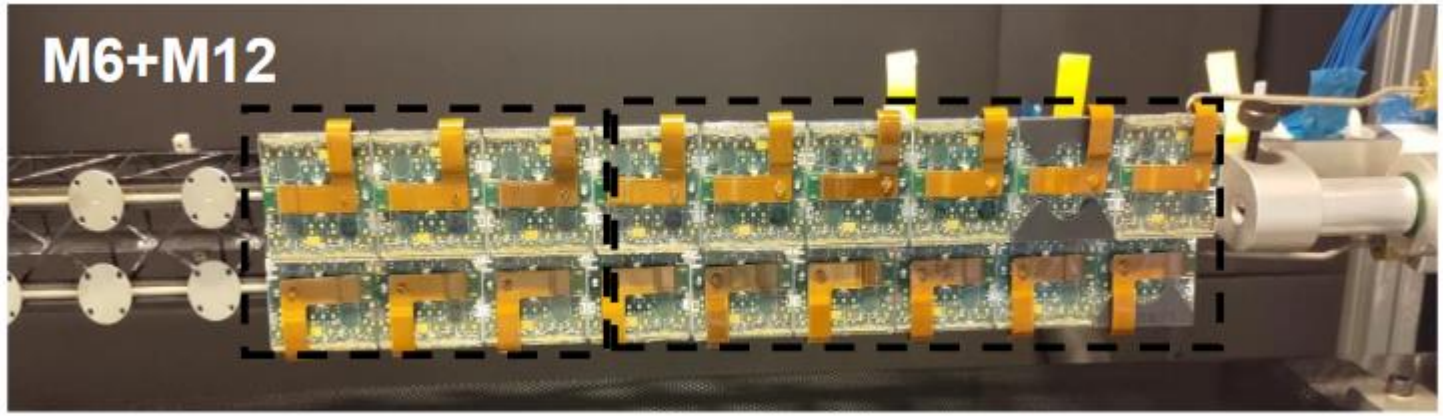
Inclined half rings

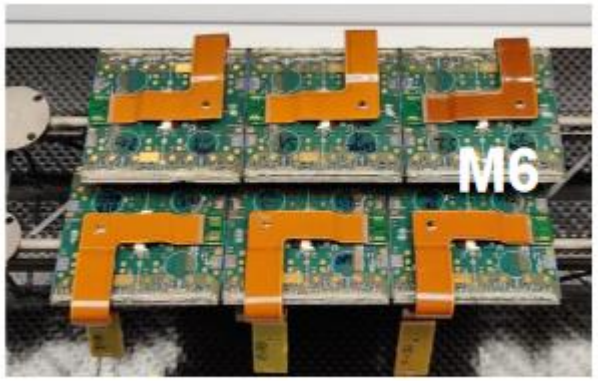
- The pixel Outer Barrel consists on the section parallel to the beam pipe where the longerons act as support structures and the inclined half rings which form an angle between 55 and 67 degree to the beam pipe

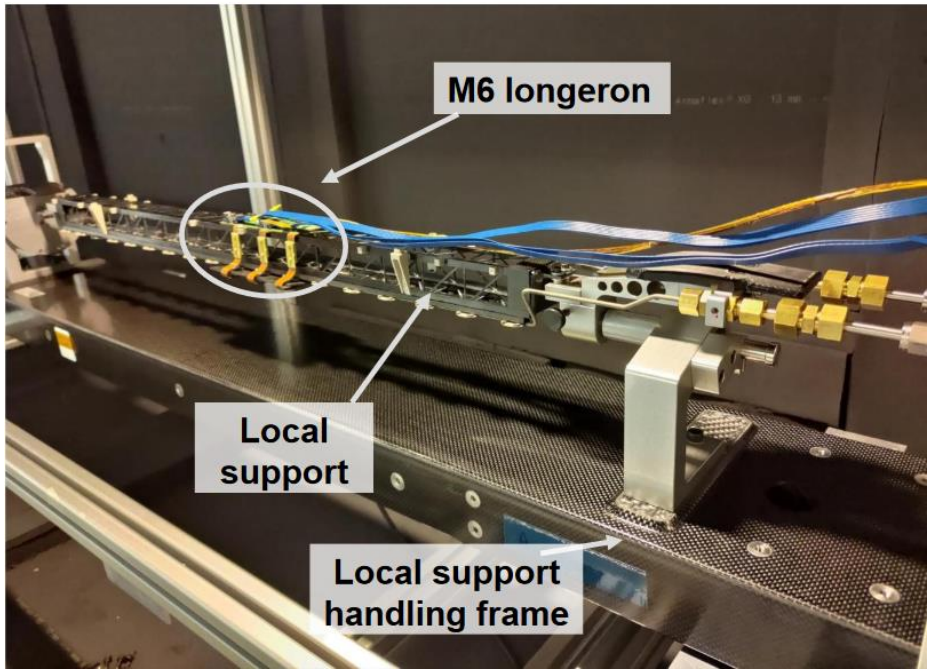


Quad module used in the Pixel Outer Barrel

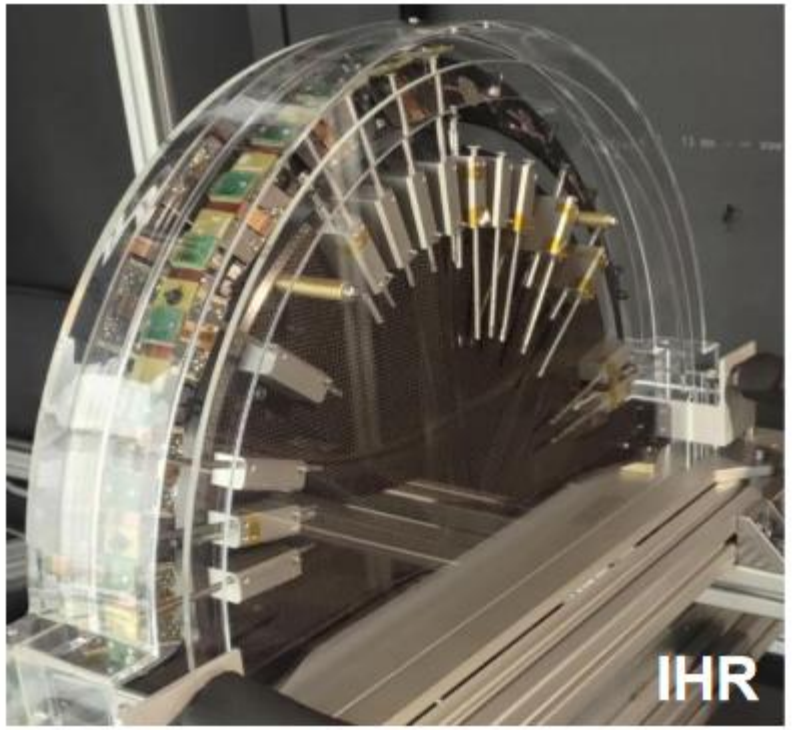
Pixel Outer Barrel - Prototypes



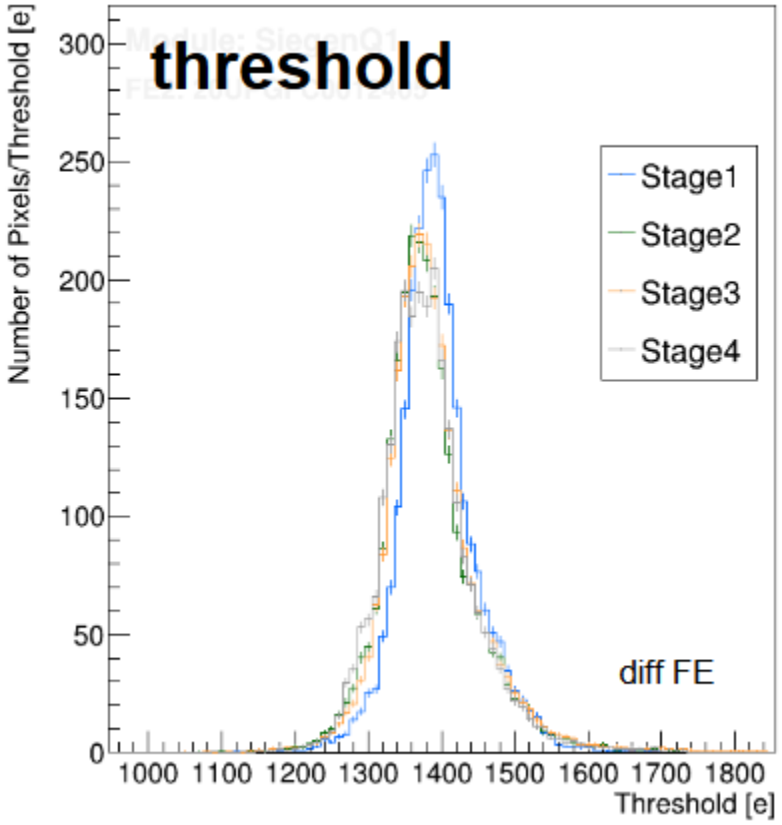


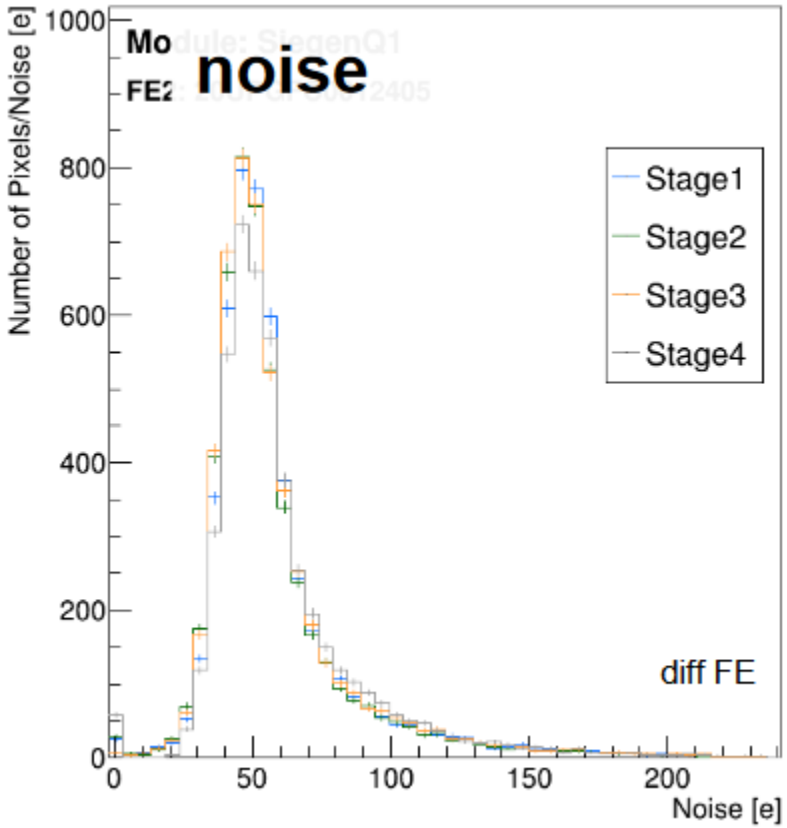


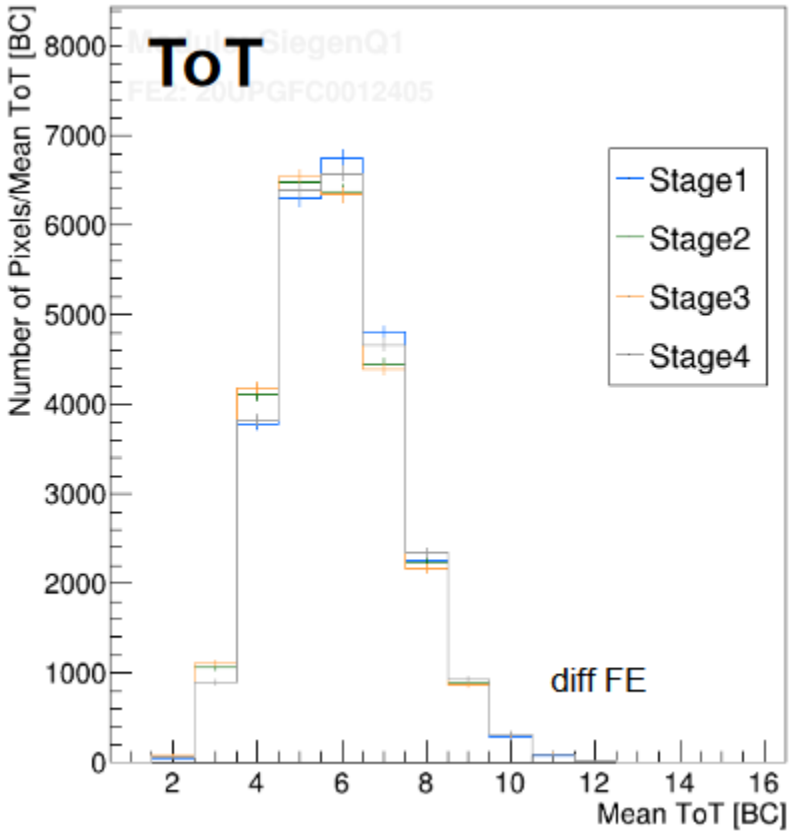
- The quad modules tested in the longeron prototype and the inclined half ring are RD53A
- Performance measurements
  - Threshold
  - Noise
  - ToT
  - IV



Readout characterization

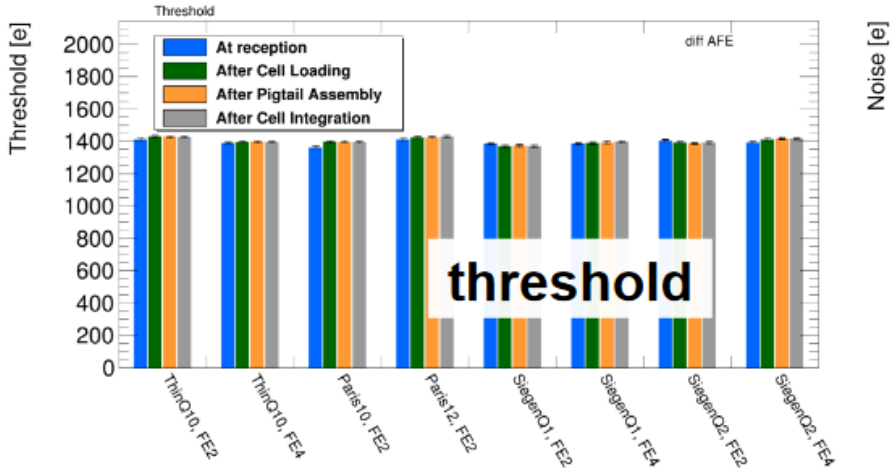


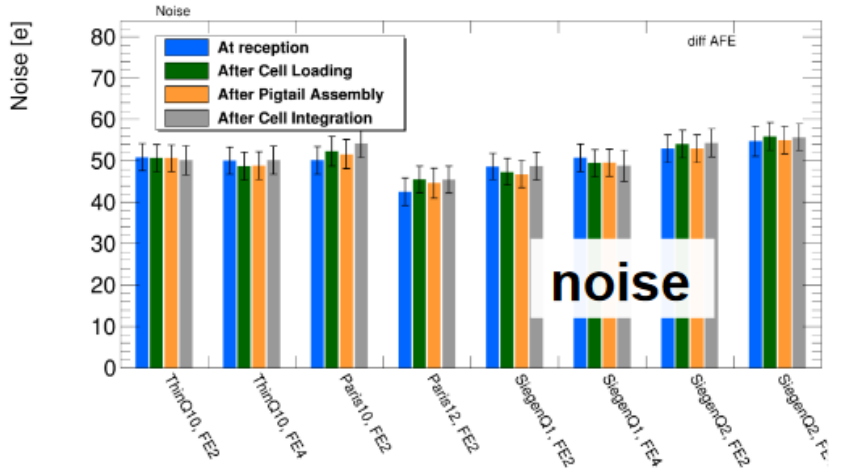


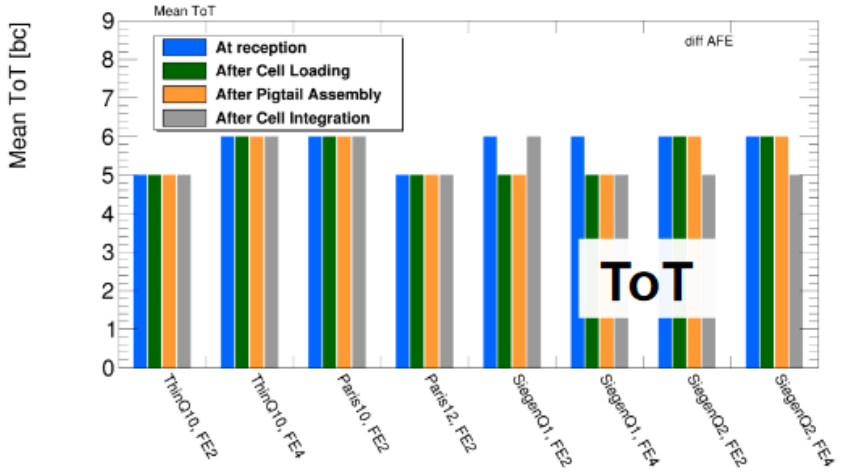


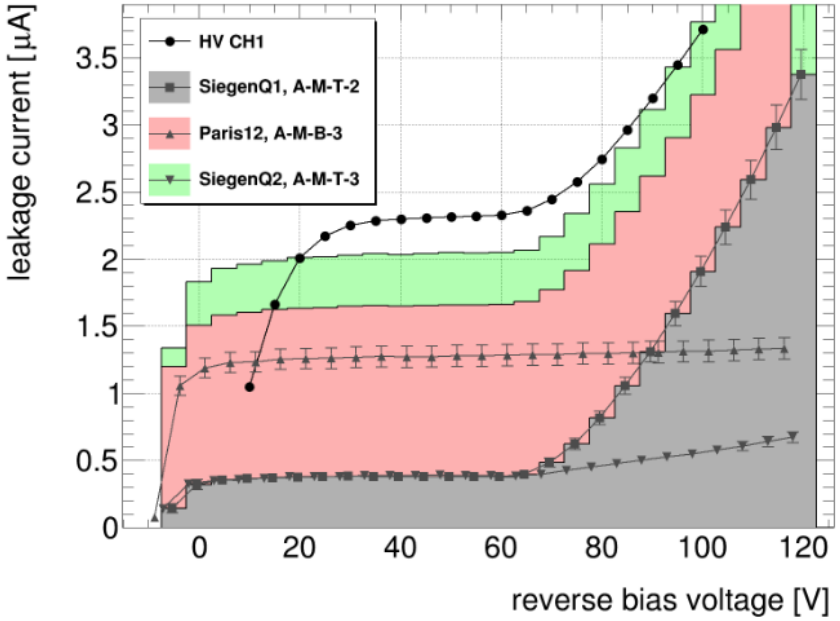
- Testing of the modules in different steps (showing differential results)
- Stages 1 (after module production), 2 (after cell loading), 3 (after pigtail assembly, 4 (after final cell integration)

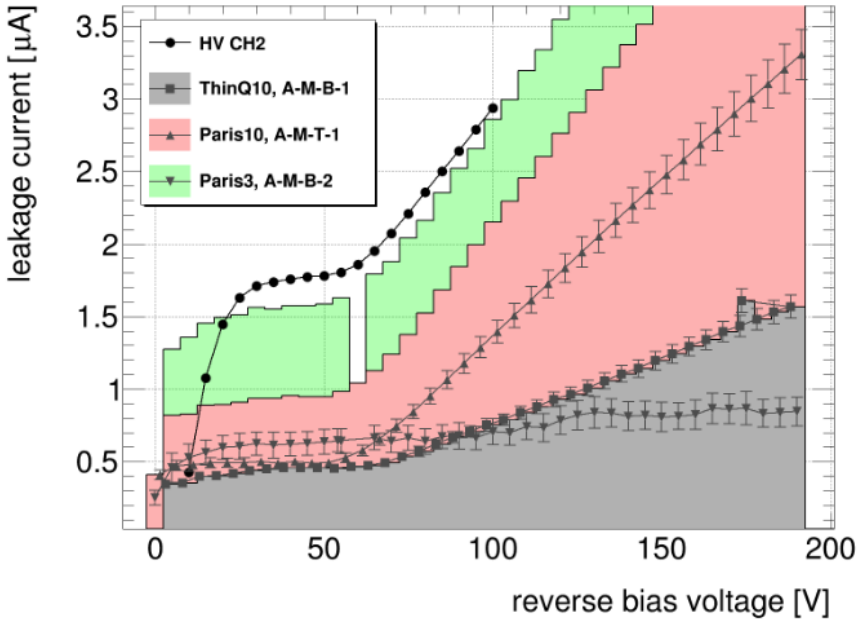
Readout characterization – M6 longeron





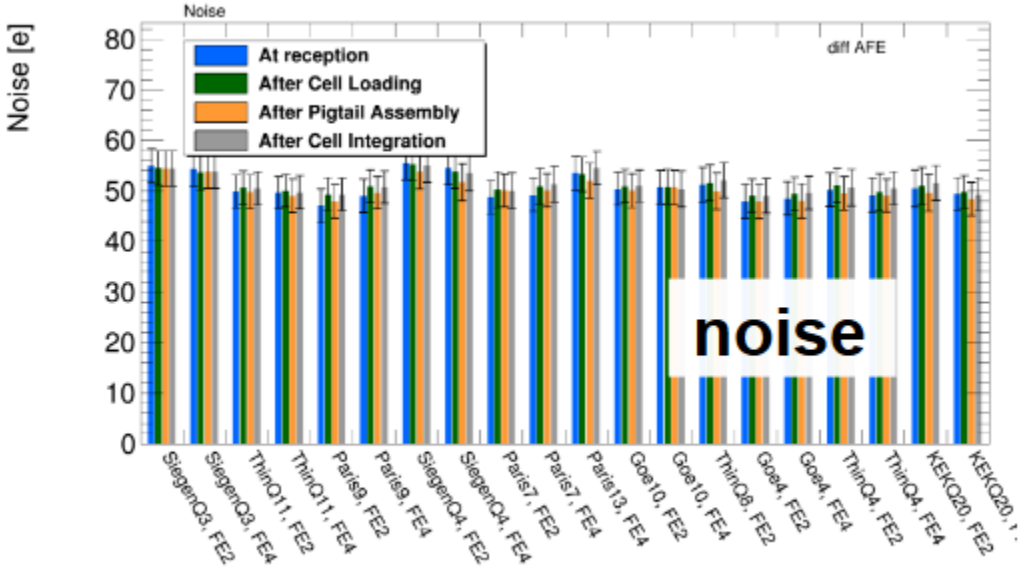


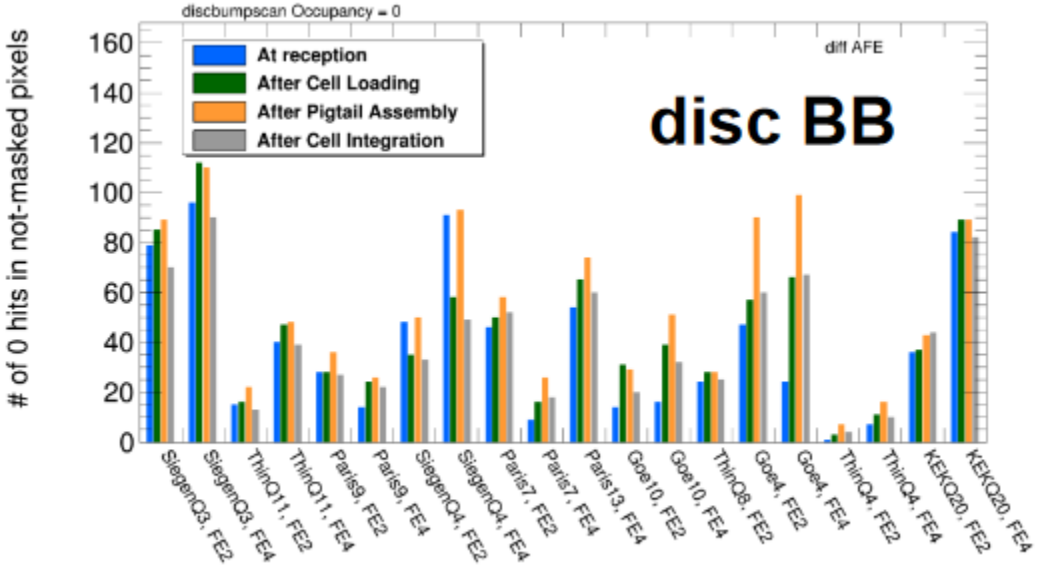




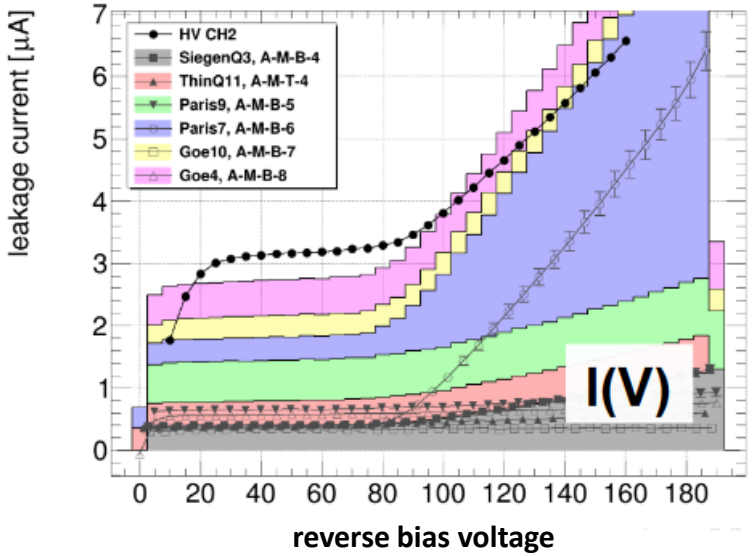
- M6 longeron performance
- Excellent agreement of threshold, noise and measured time-over-threshold between stages
- No indication for degradation of the readout chip performance
- Expected leakage currents in HV group estimated by sum of individual contributions measured after cell loading

Readout characterization – M12 longeron

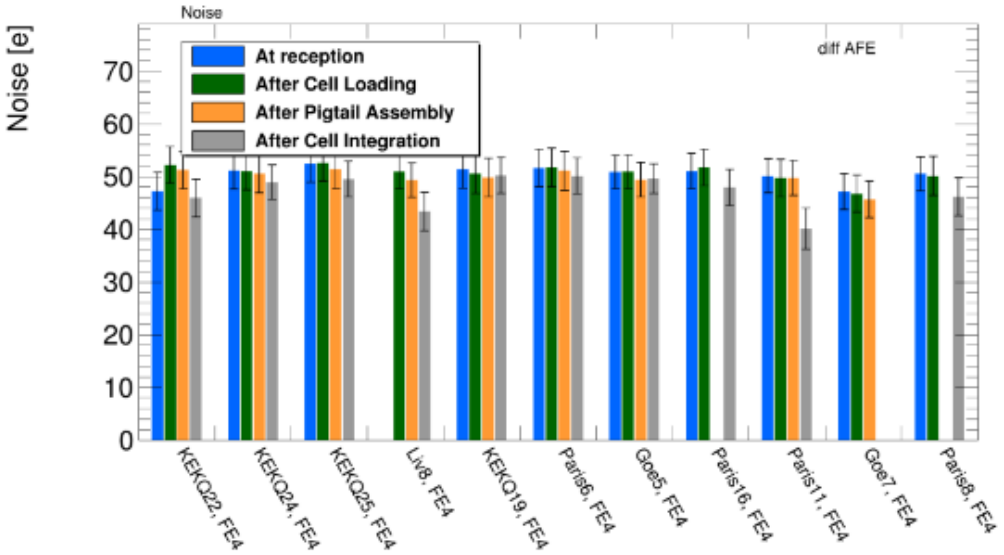


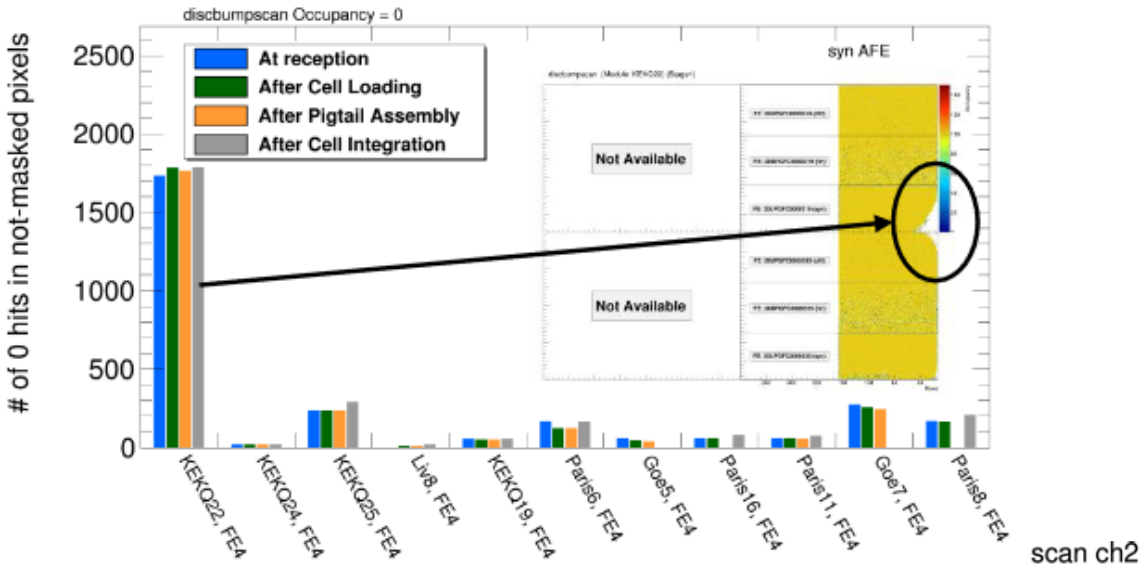


- Overall good performance of the M12 longeron
- Excellent agreement between different stages
- No sign for any degradation of the performance of the modules before and after cell integration
- Leakage current of the serial power chain compatible with the sum of the individual contributions

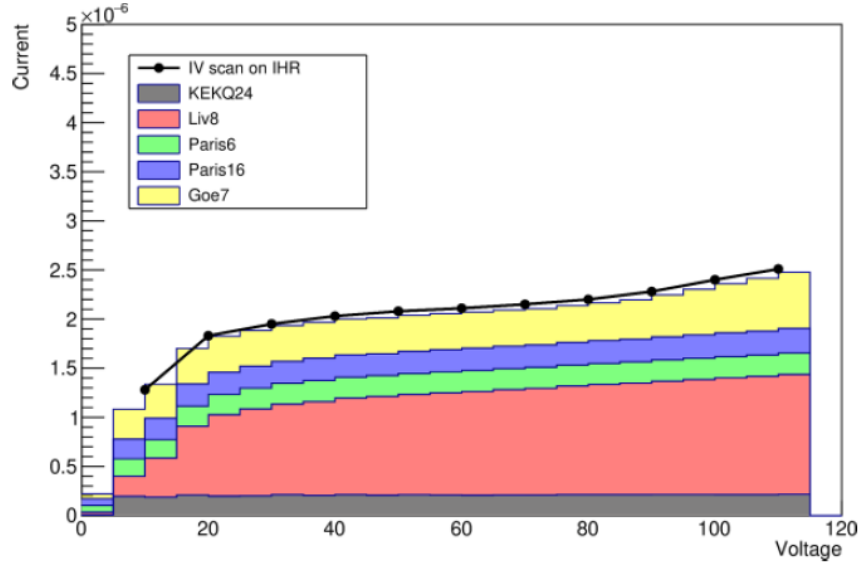


Readout characterization – Inclined half ring



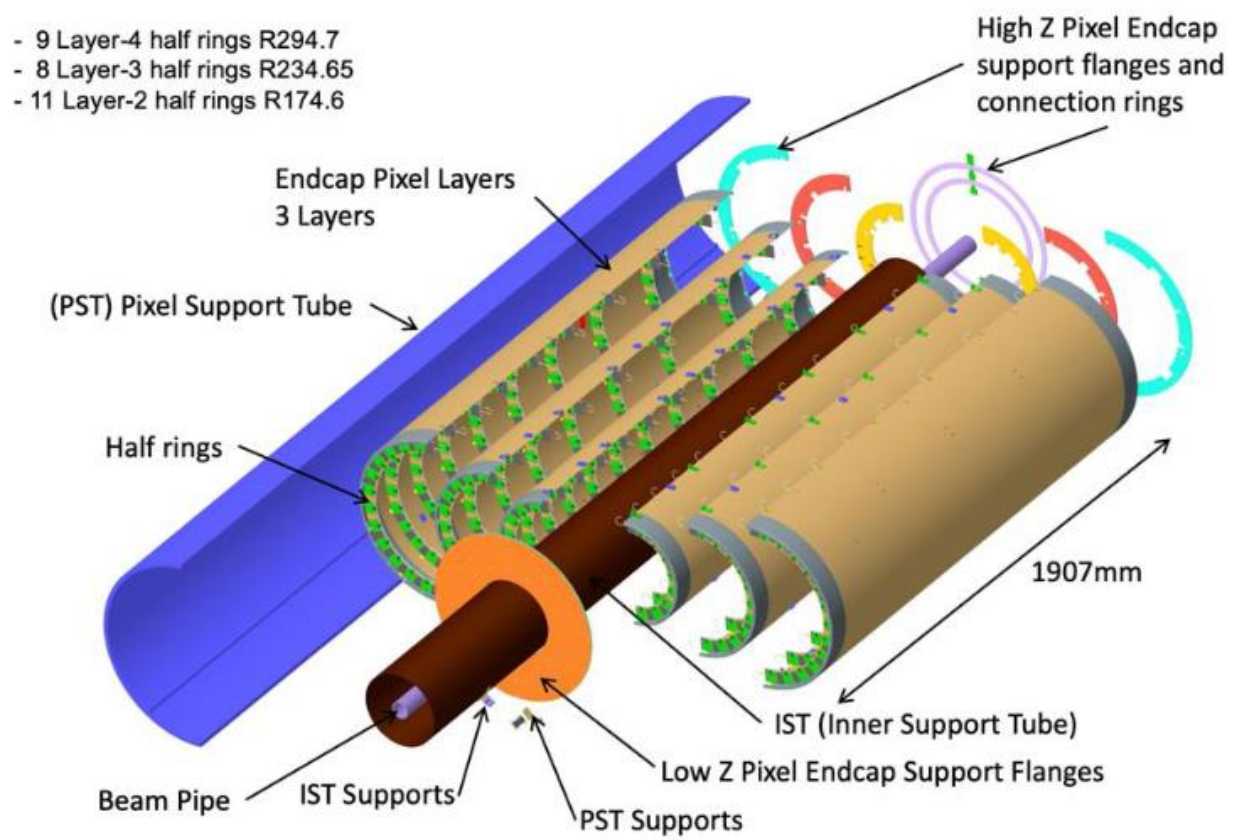


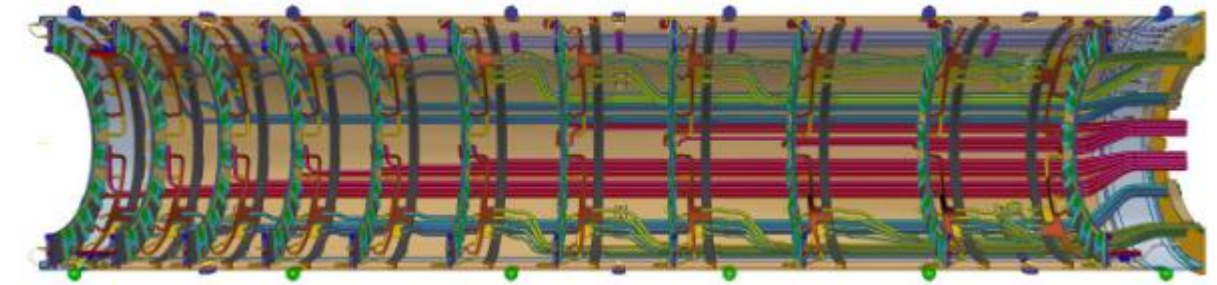
- Good agreement between stages
- No sign of degradation before and after cell integration
- Leakage current of the serial power chain compatible with the sum of the individual contributions

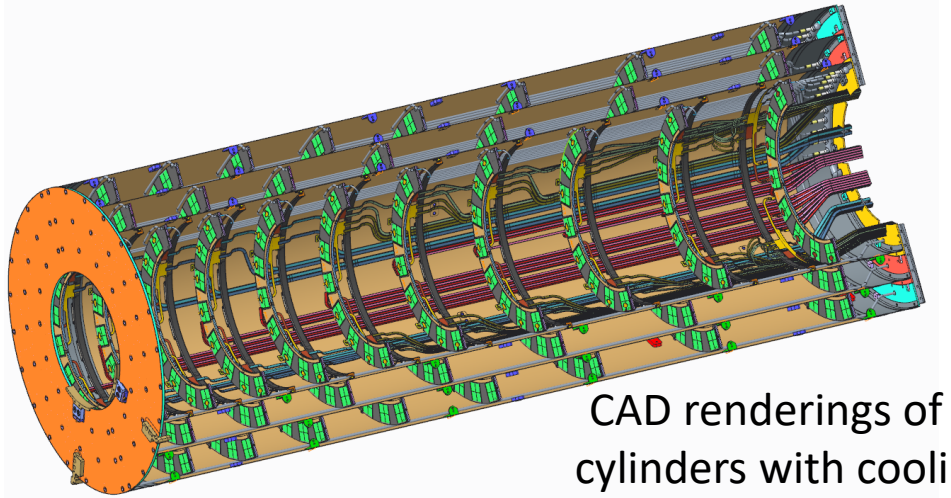


Pixel Outer Endcaps

Pixel Outer Endcaps



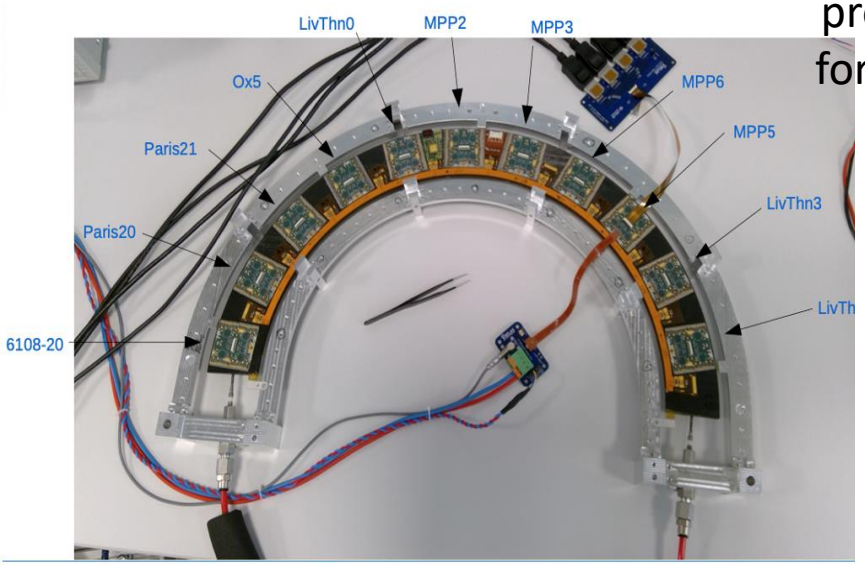




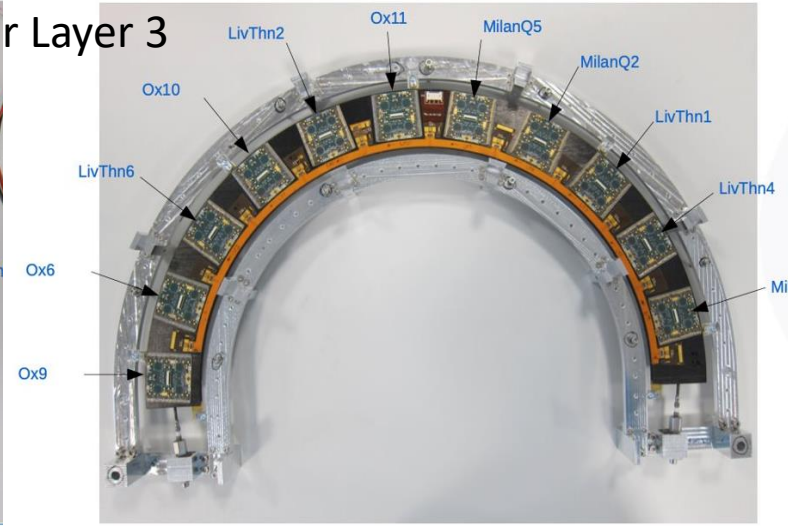
CAD renderings of the support cylinders with cooling pipes and cabling visible

- Half ring → basic local-support structure for the Outer Endcaps
  - Supports two serial-powering chains of modules one per face of the half-ring
- The half rings tested are loaded with modules using RD53A chip

Ring 1 Prototype



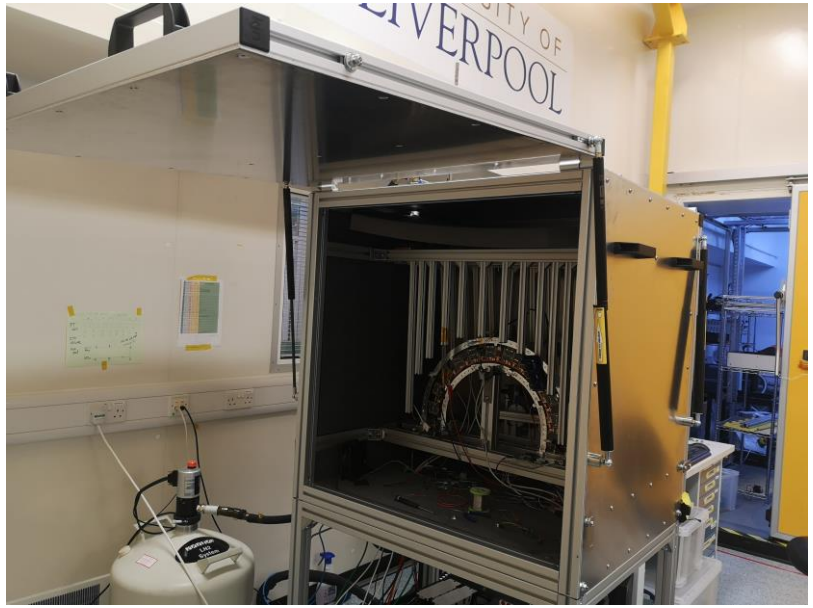
Ring 1 prototype for Layer 3



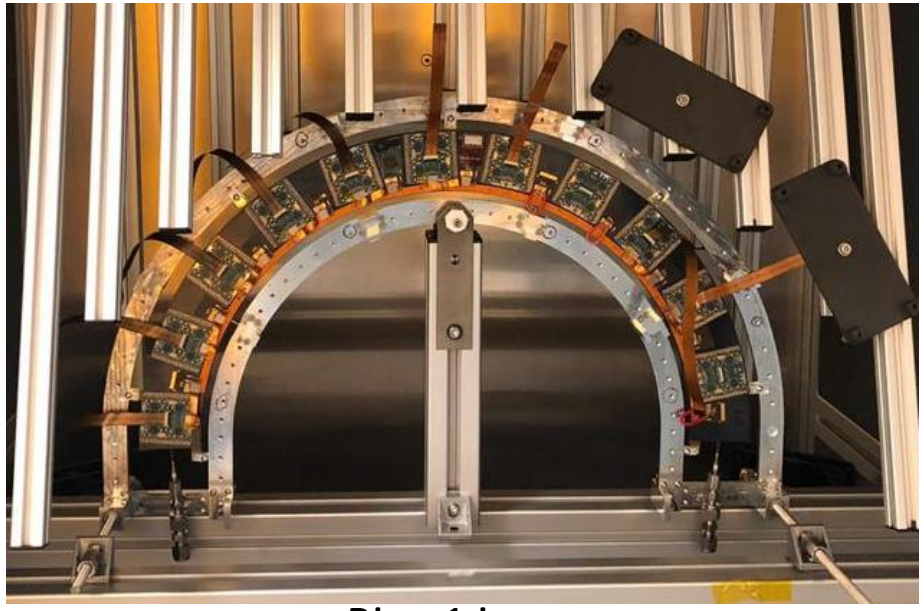
Prototype of support cylinder for Layer 4

- First prototype of half ring was populated with RD53A quad modules
- Each side of the ring 1 has 11 quad modules
- Testing consists in evaluating each module before being loaded, after being loaded individually and connected to the serial power chain
- The tuning of the modules before loading was used in all the latter steps to determine if loading produced any changes

Ring 1 Prototype



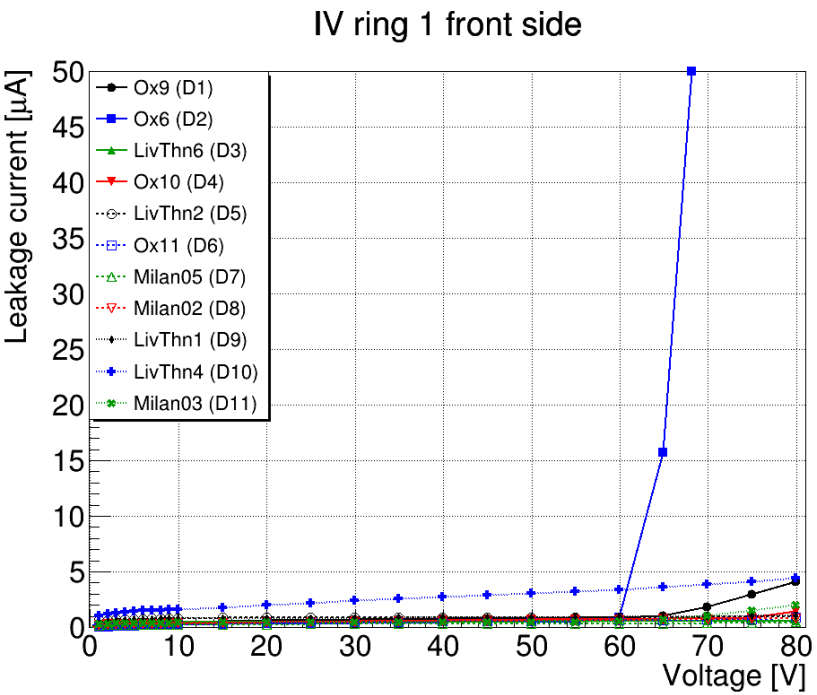
Cooling box at Liverpool – can hold any half ring size

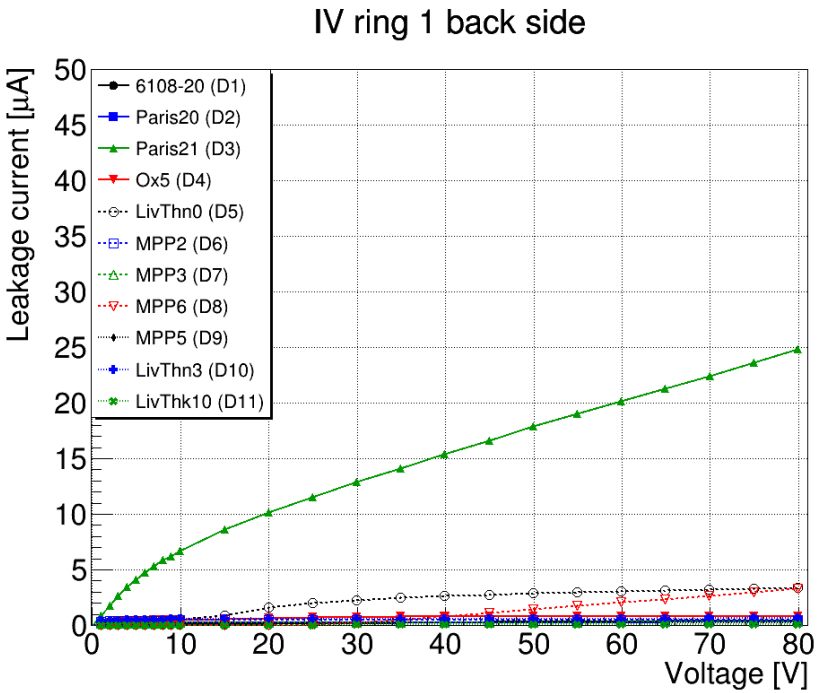


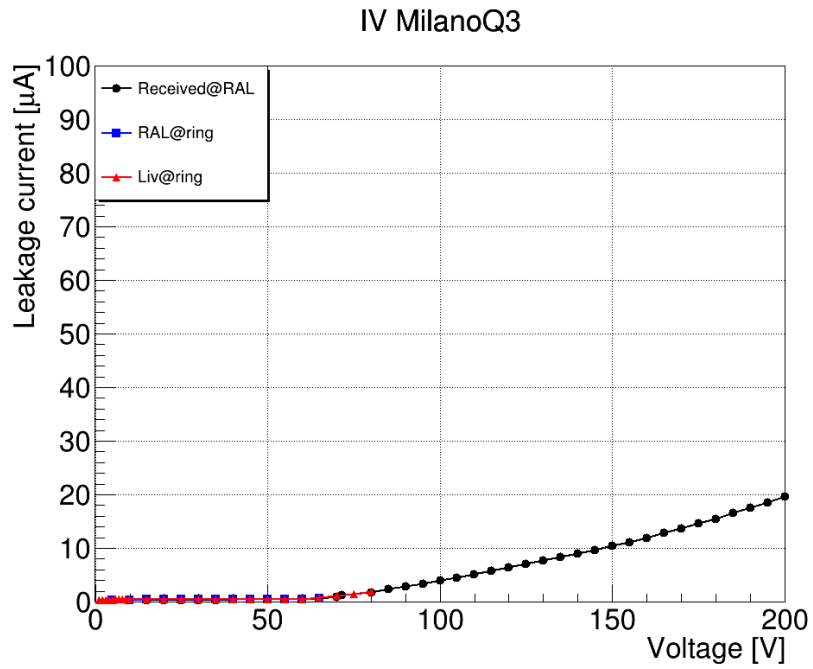
Ring 1 in cooling box

- Using the cooling box, a set of different tests were performed
  - Individual IVs for all the modules at different temperatures
  - Low voltage probing connecting modules to the chain 1 by 1
  - IV scan for the full chain with LV supply off and on at different temperatures
  - Electrical characterization comparing results with previous results

IV single modules

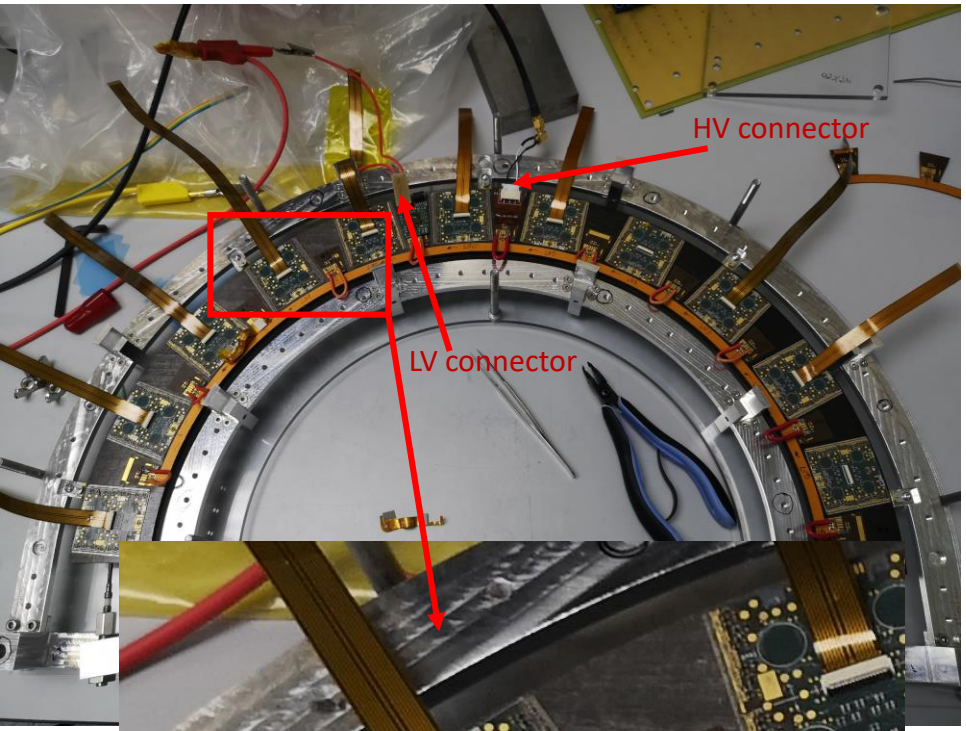


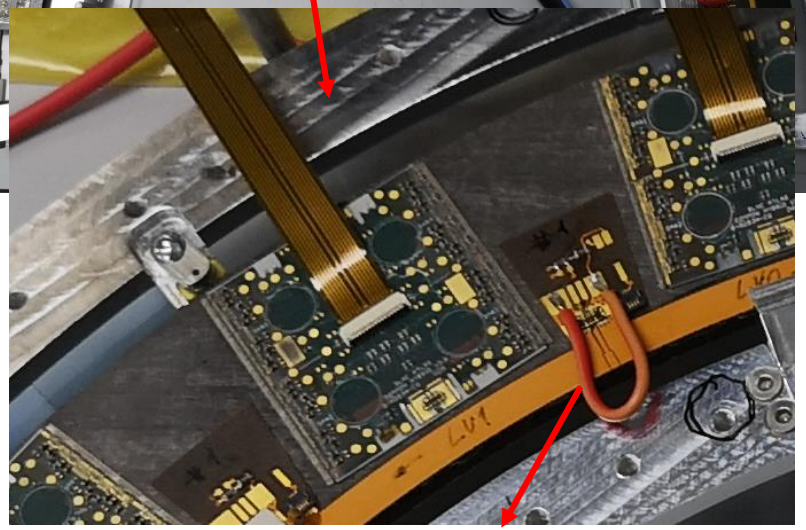




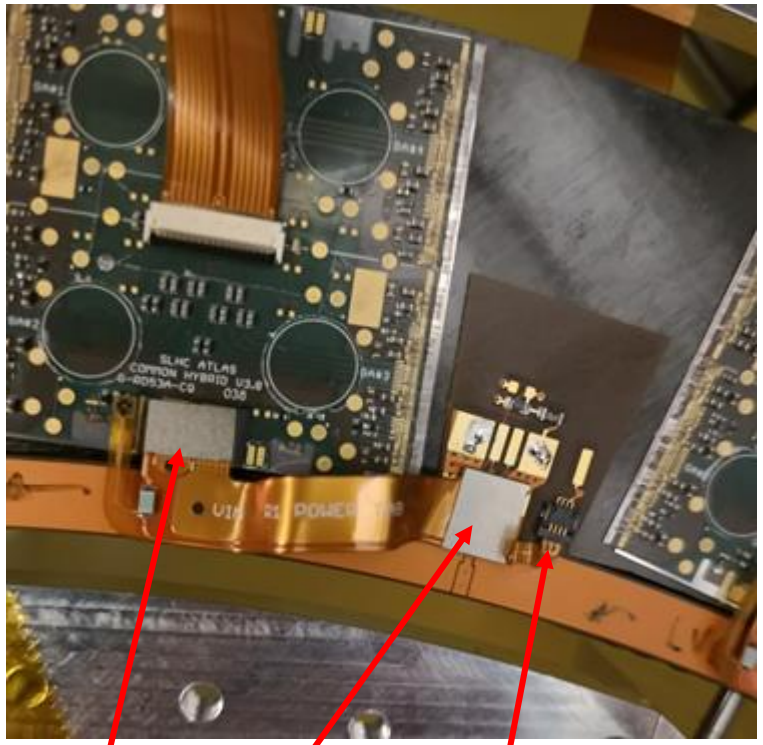
- Done at room temperature (~20 ^{o}C) with low voltage power off out of the cooling box
- Comparison of the IV at different loading steps show good agreement meaning no degradation

Testing module Low Voltage connection





Bypass

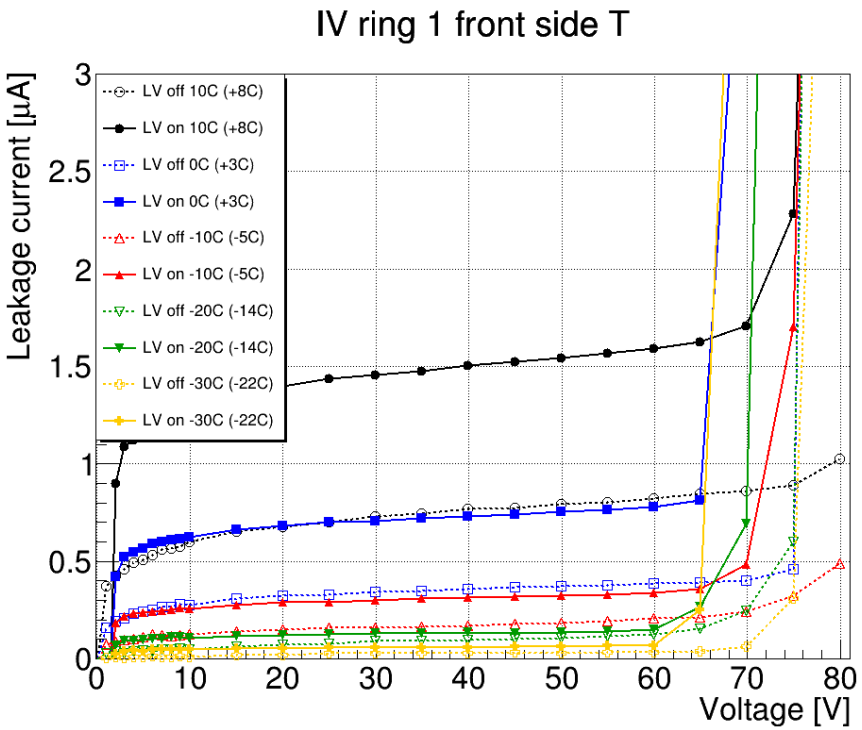


- LV/HV connector
- LV connector
- Tape HV ZIFF connector

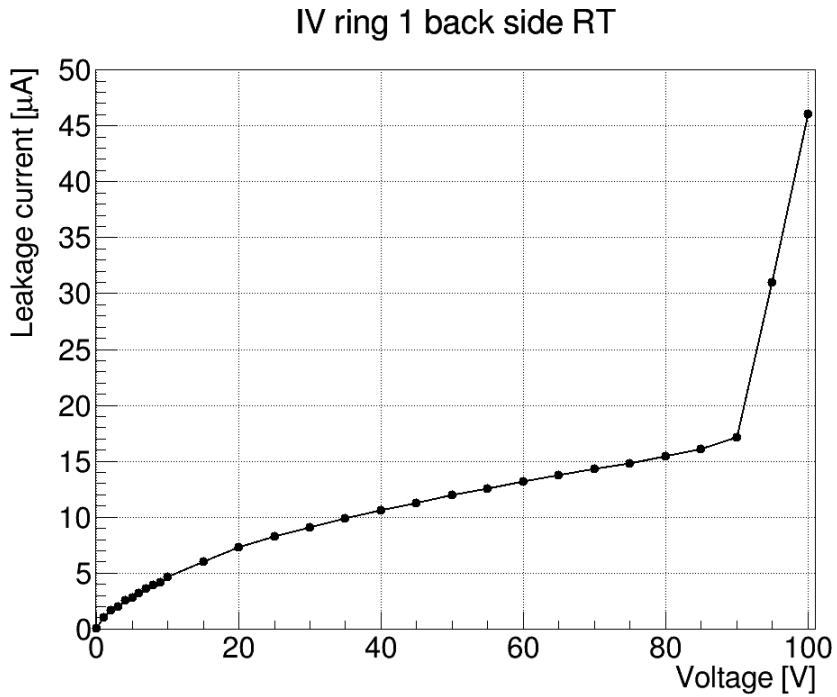
# of devices	LV (V)
1	2.375
2	3.992
3	5.613
4	7.249
5	8.888
6	10.503
7	12.069
8	13.685
11	18.4

- All the sensors but one were bypassed
- Measurement of LV were done adding modules one by one
- Power supply in constant current mode @ 4.6 A

IV on serial power chain

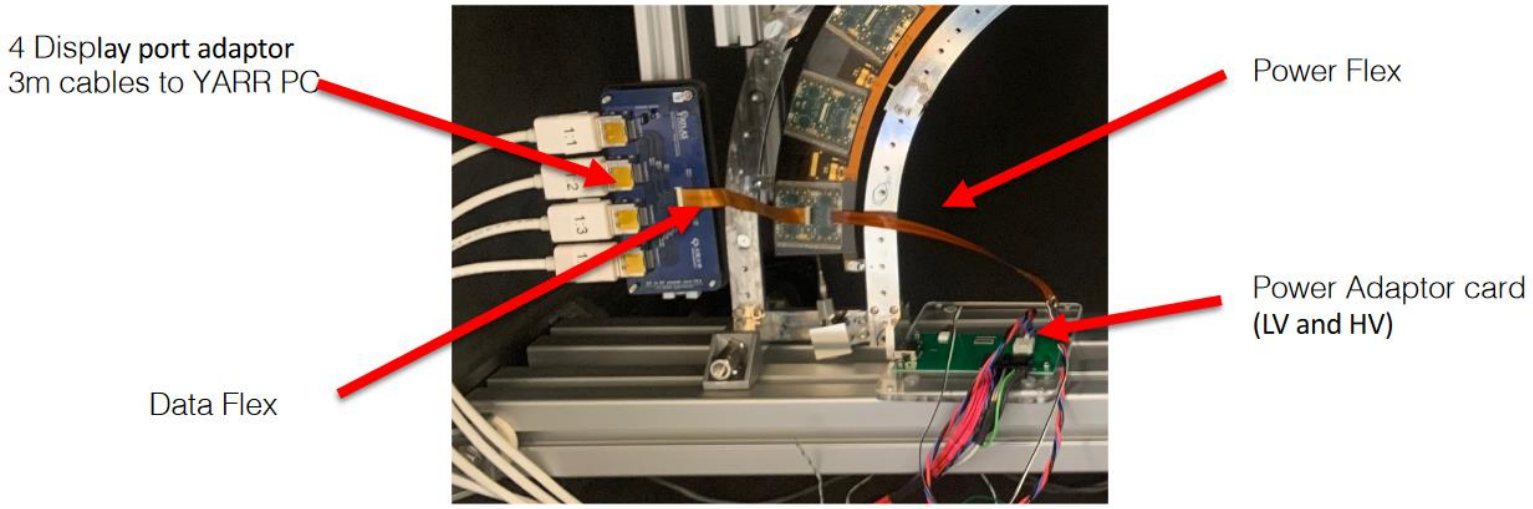


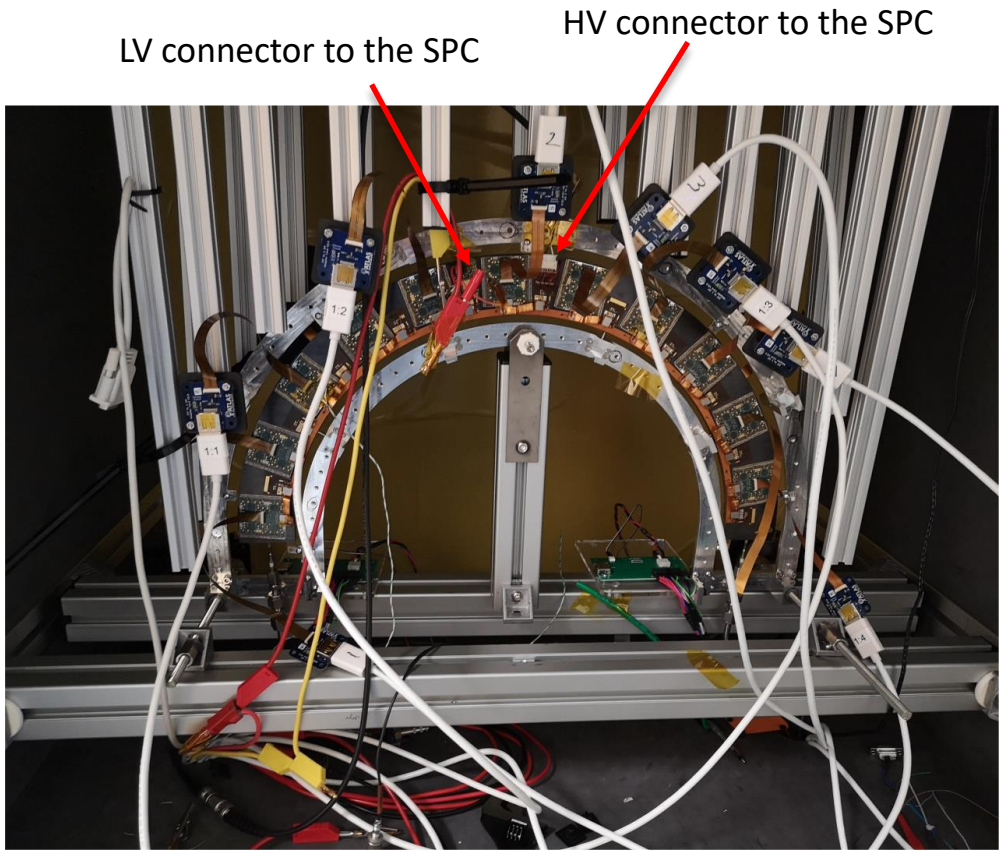
Plant T [ºC]	Module T [ºC]
+10	+8
0	+3
-10	-5
-20	-14
-30	-22



- Front side leakage current measured at different temperatures with LV supply powered off and on
  - Modules with low breakdown voltage will be removed in future testing to avoid working at the power supply limit
- Back side only measured at room temperature with LV supply powered off (ongoing)

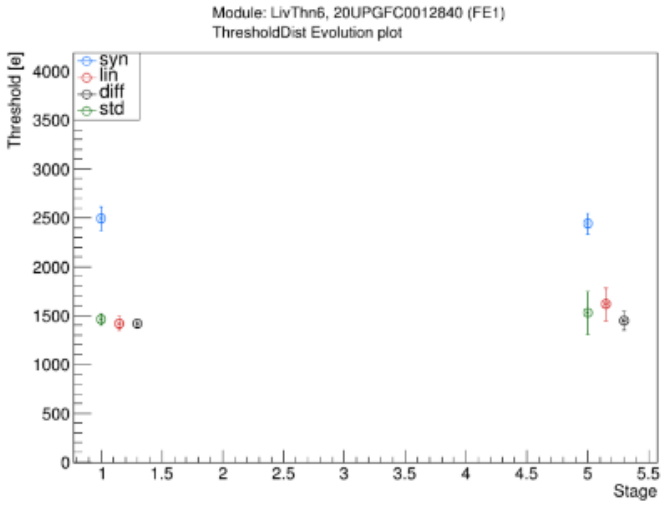
Readout characterization

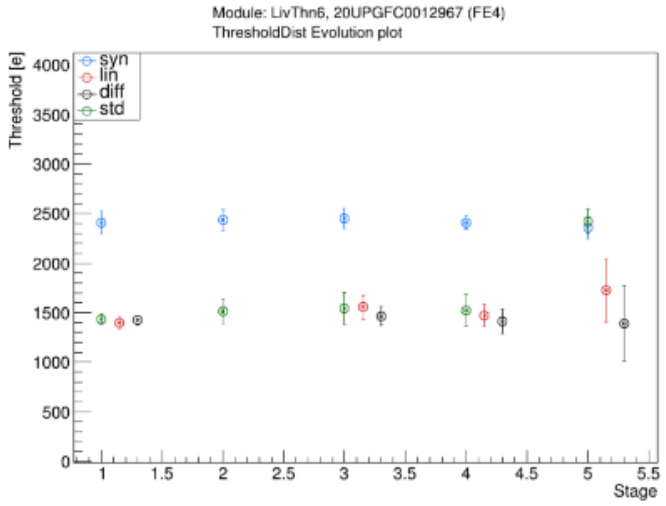


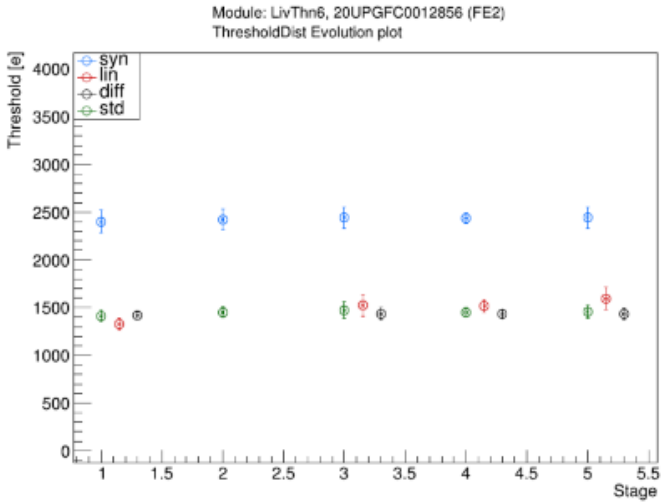


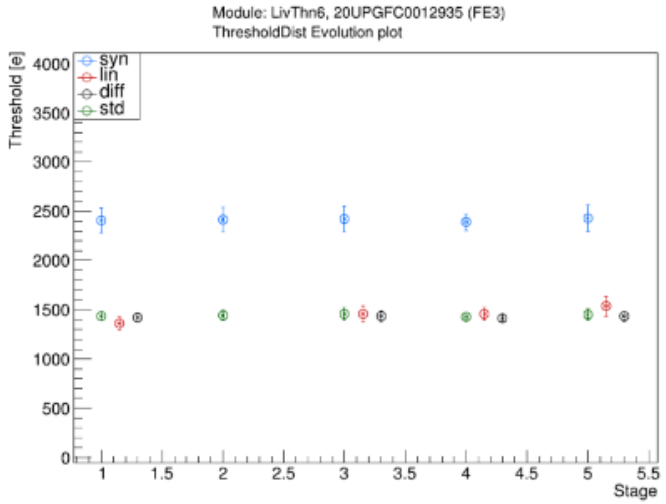
- Setup to do the characterization at the different building steps: single module testing and SPC testing

Readout characterization (threshold)









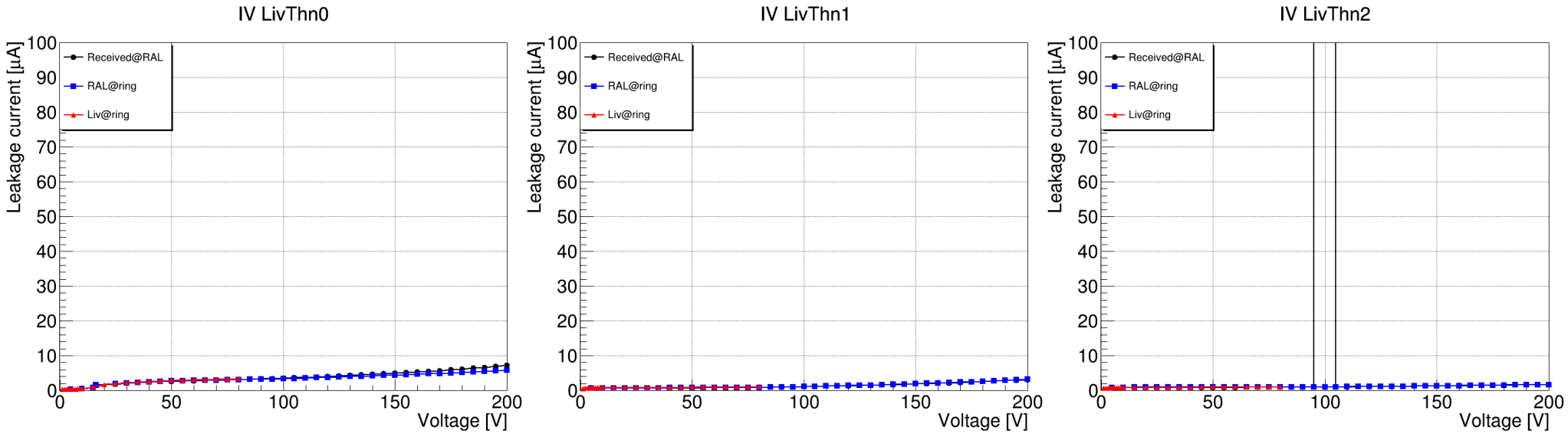
- Taking one module as representative for all results
- Scans for stages 1 (module build), 2 (pre loading), 3 (post loading), 5 (serial power chain)
- Plots show number of good pixels and no degradation on the different steps

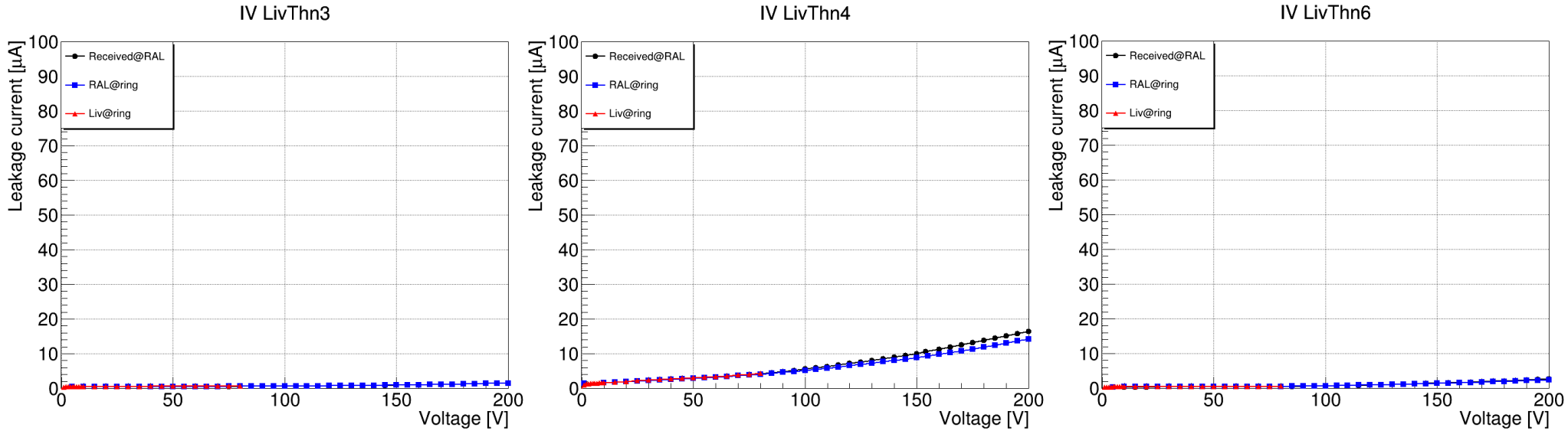
Conclusions

- Validation of the Inner System, Outer Barrel and Outer Endcaps is an on going effort
- Modules were tested in different steps of construction and integrated on prototypes of the different systems
- Good performance of the modules through all the loading steps for all the systems
- No degradation observed during module integration on prototypes
- Still a long road to validate but it is moving forward!

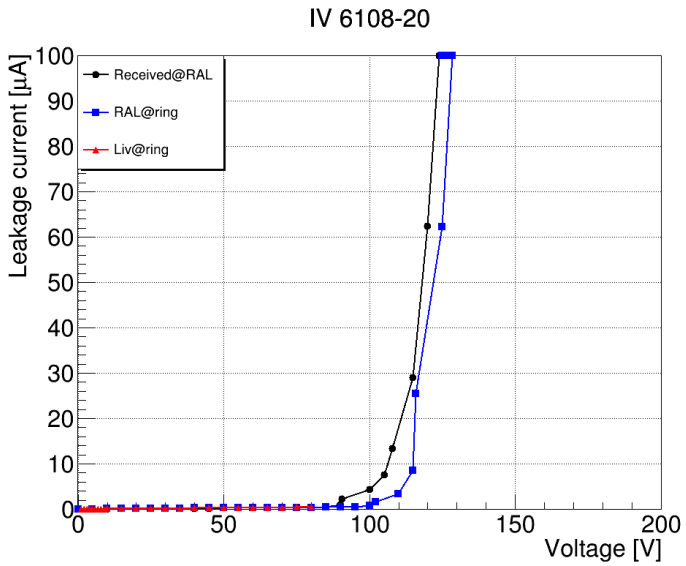
Questions?

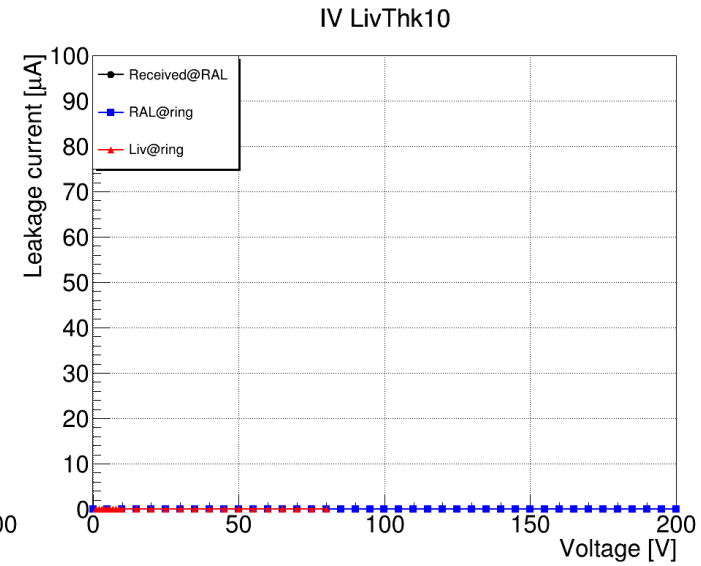
Ring 1 IV measurements - comparison

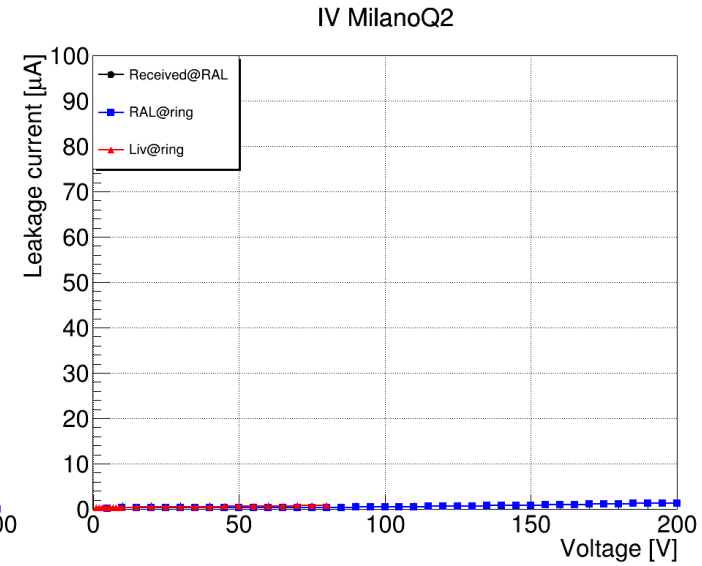


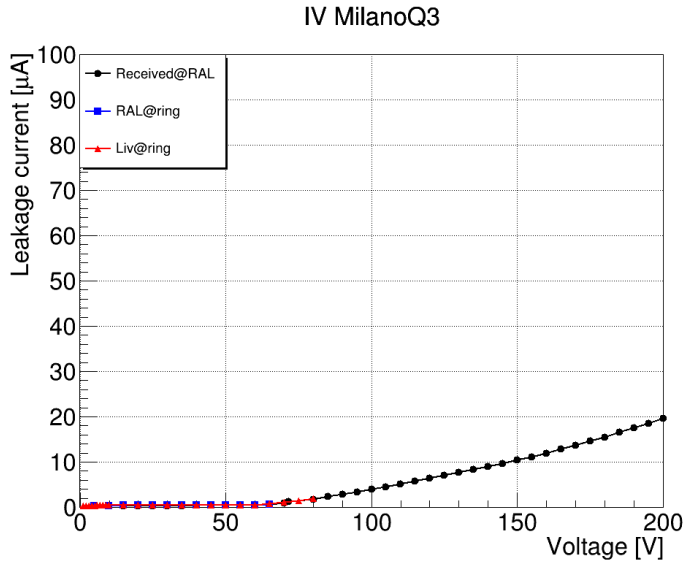


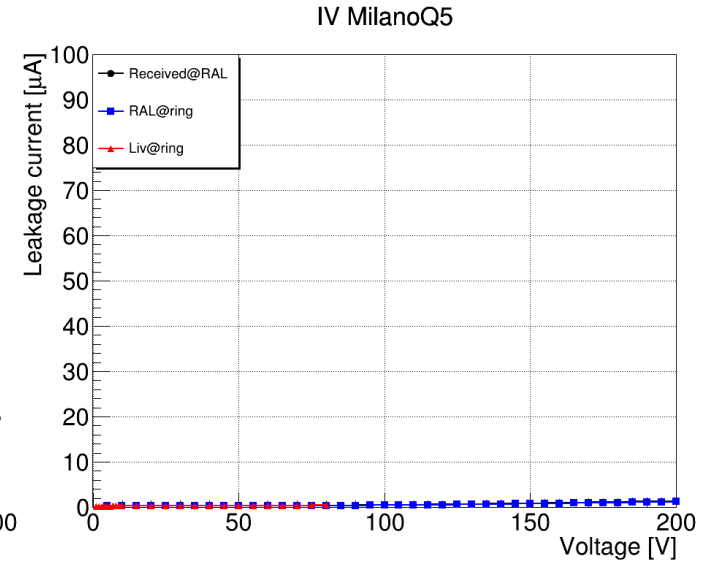
Ring 1 IV measurements - comparison

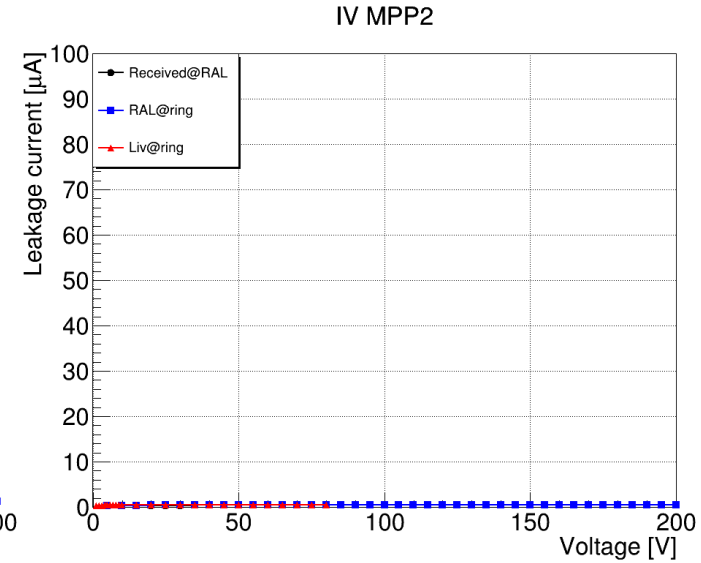




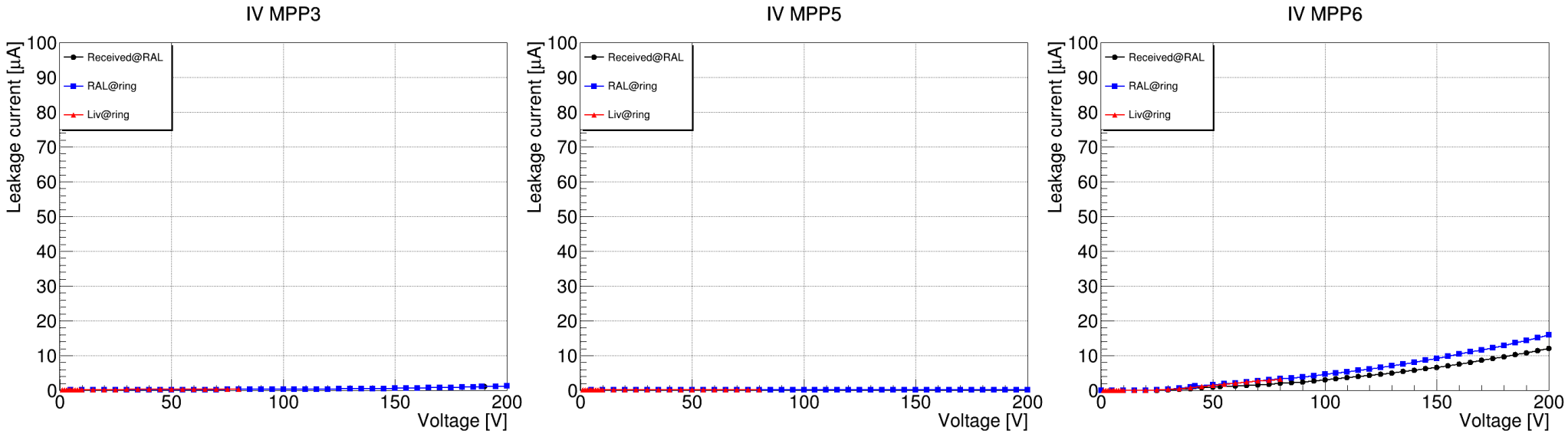


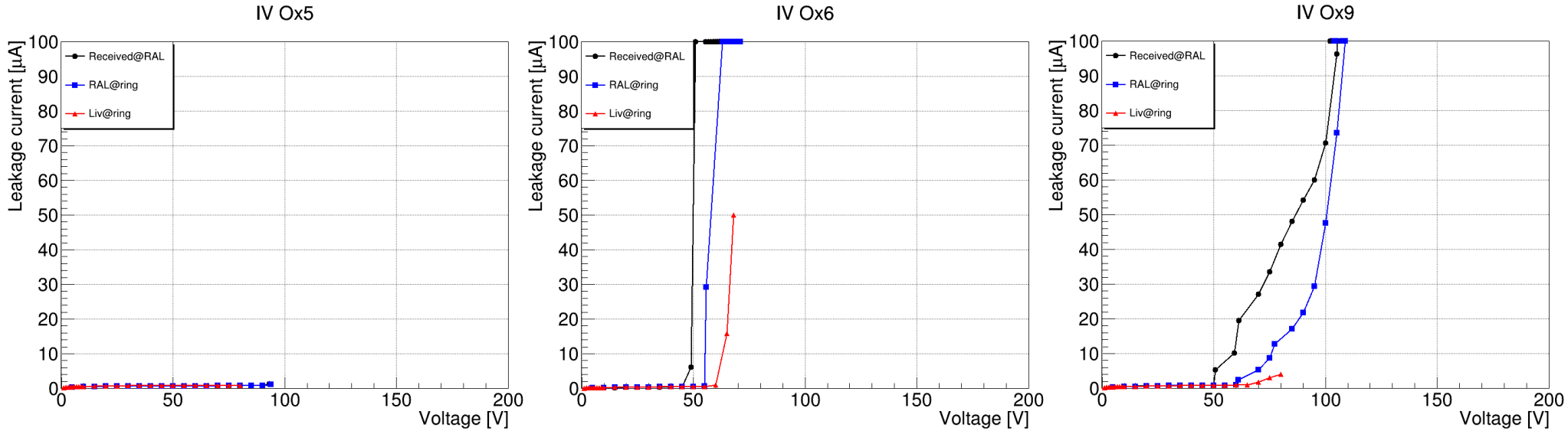




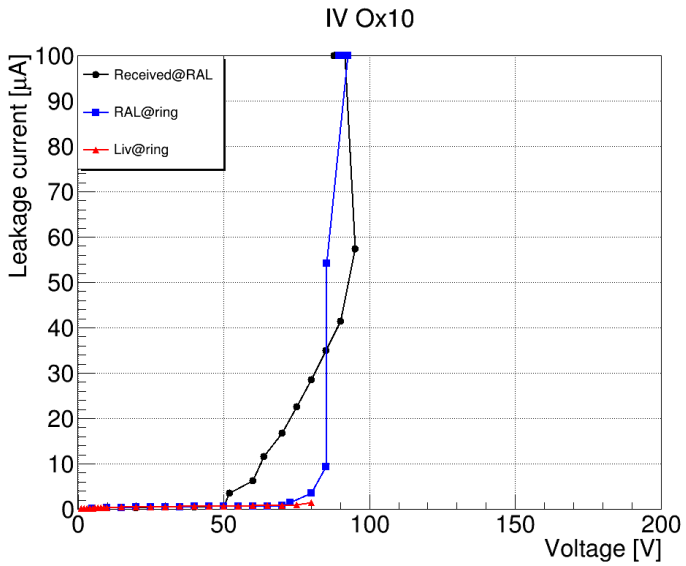


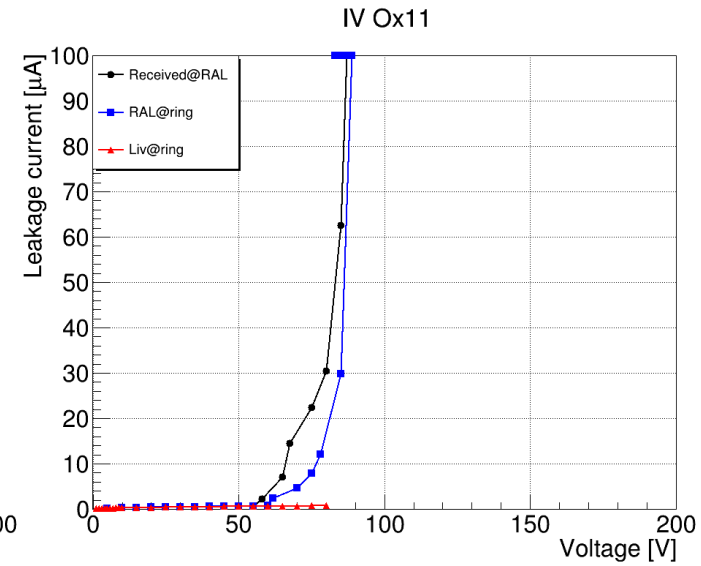
Ring 1 IV measurements - comparison

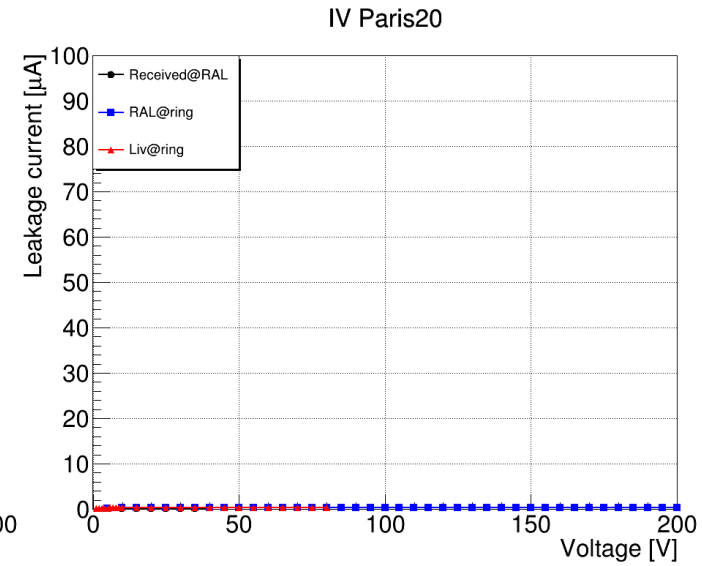


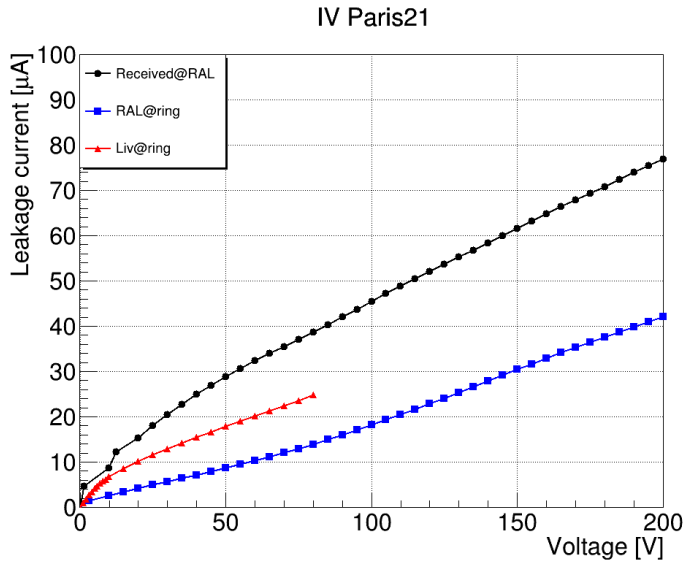


Ring 1 IV measurements - comparison

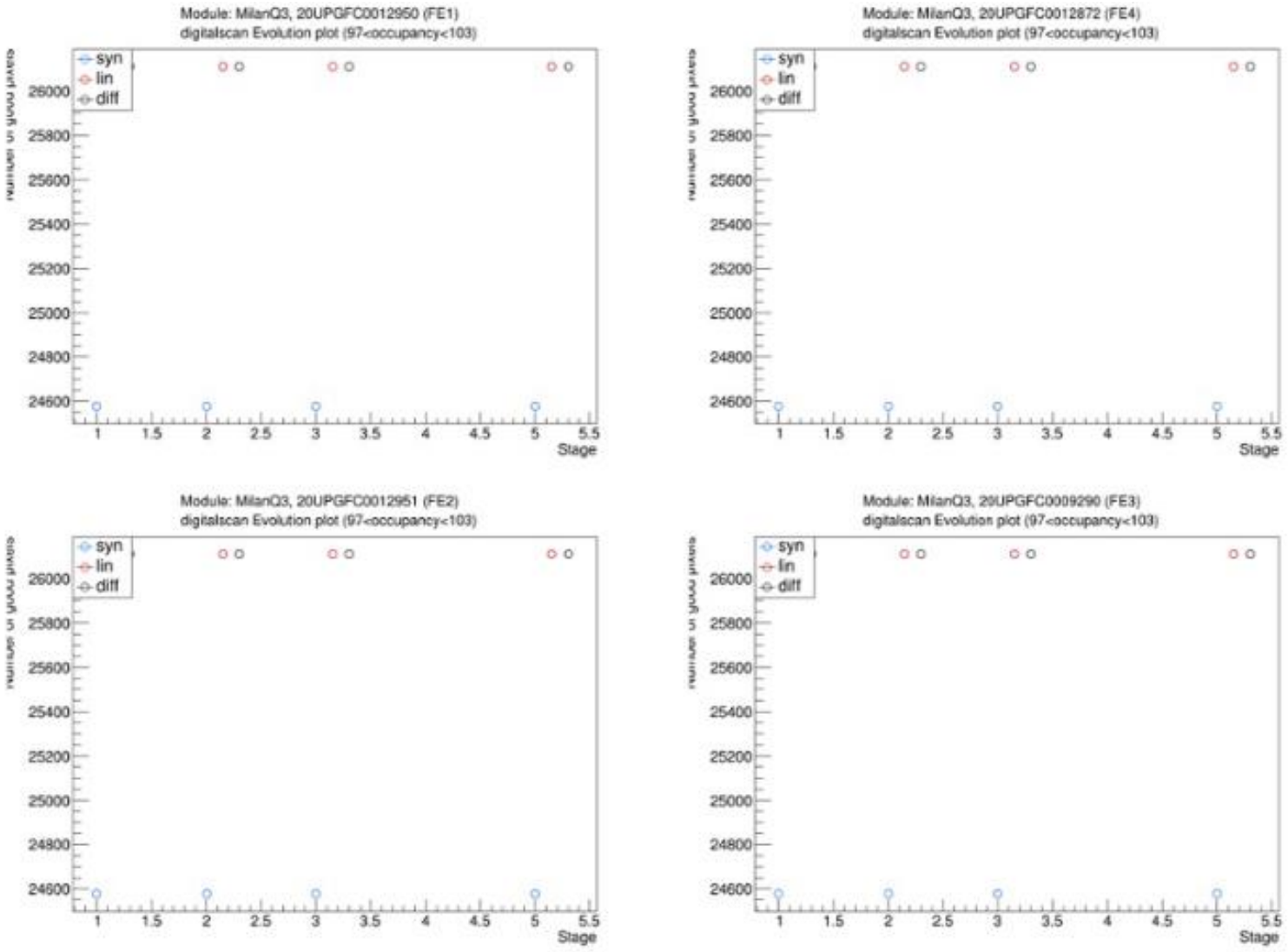






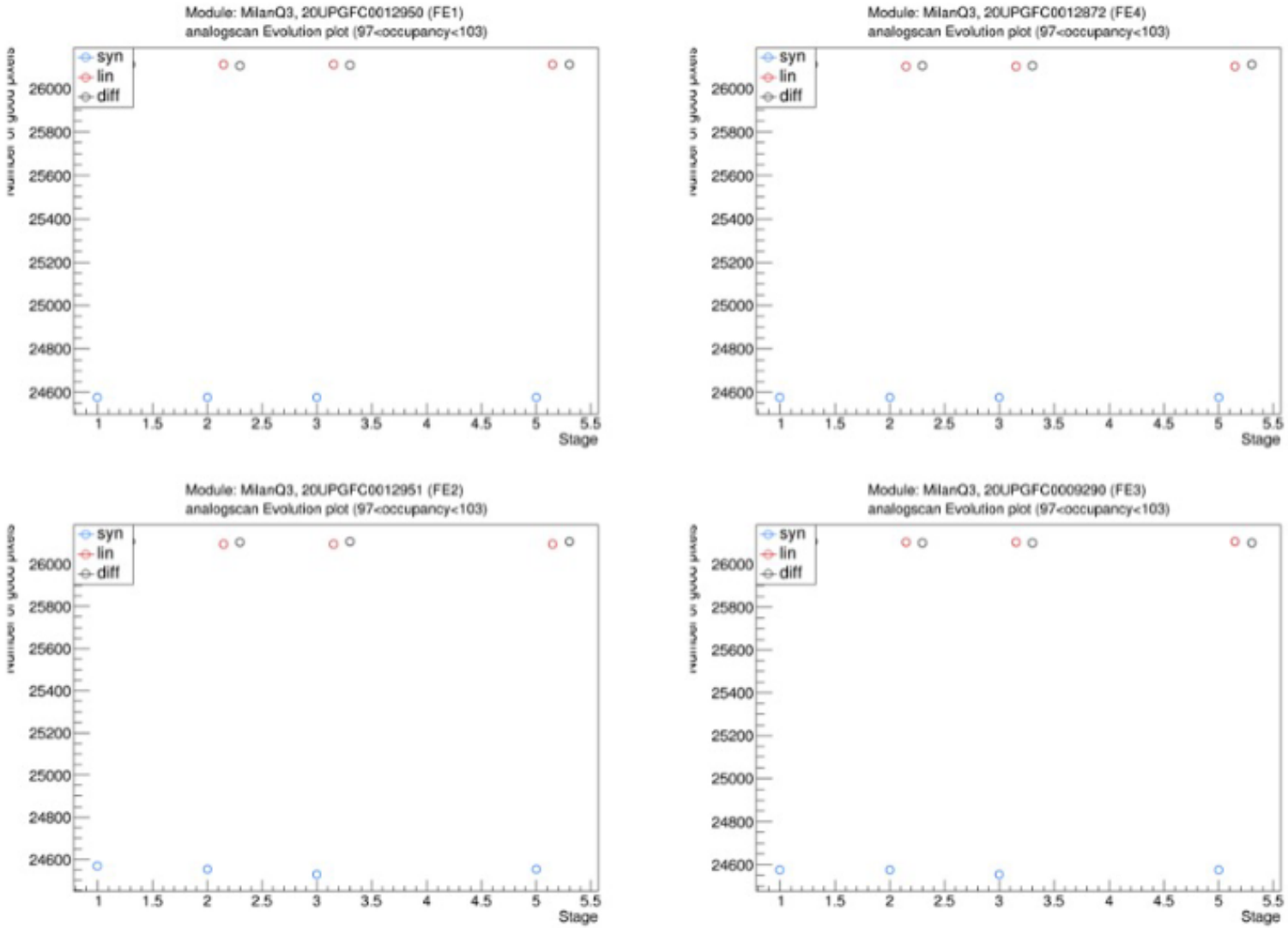


Readout characterization (digital)



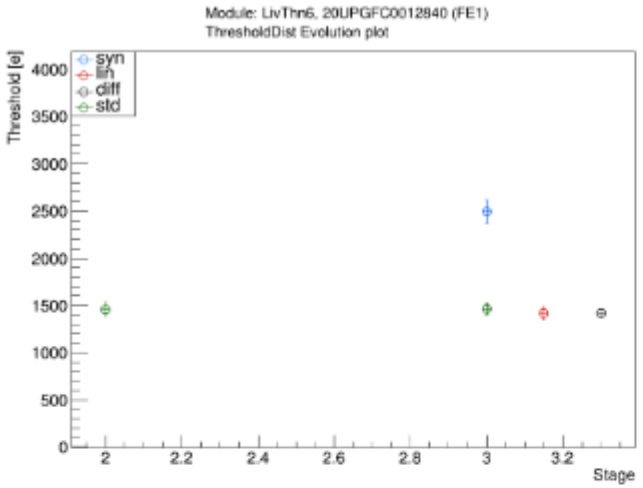
- Taking one module as representative for all results
- Scans for stages 1 (module build), 2 (RAL pre loading), 3 (RAL post loading), 5 (Liv serial power chain)
- Plots show number of good pixels

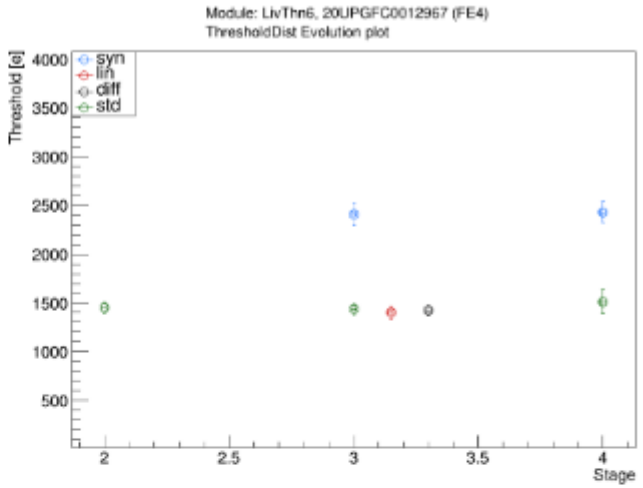
Readout characterization (analog)

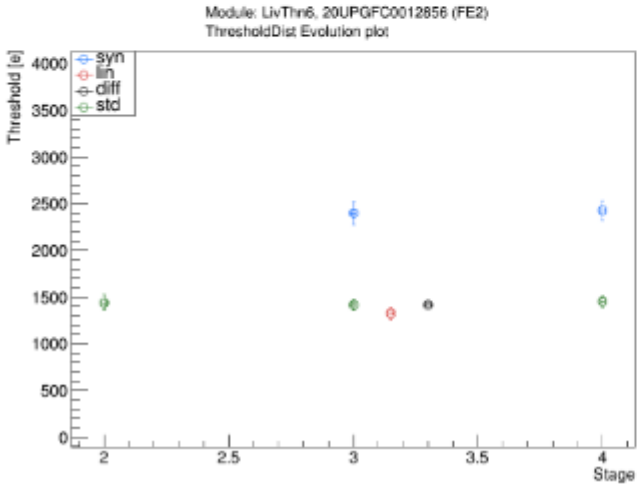


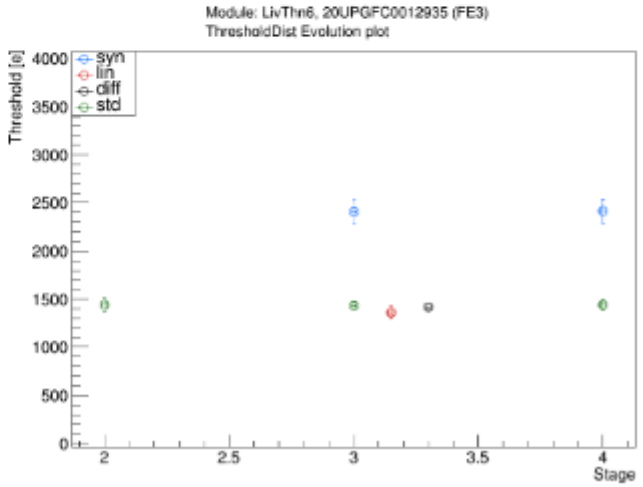
- Taking one module as representative for all results
- Scans for stages 1 (module build), 2 (pre loading), 3 (post loading), 5 (serial power chain)
- Plots show number of good pixels

Readout characterization (threshold)



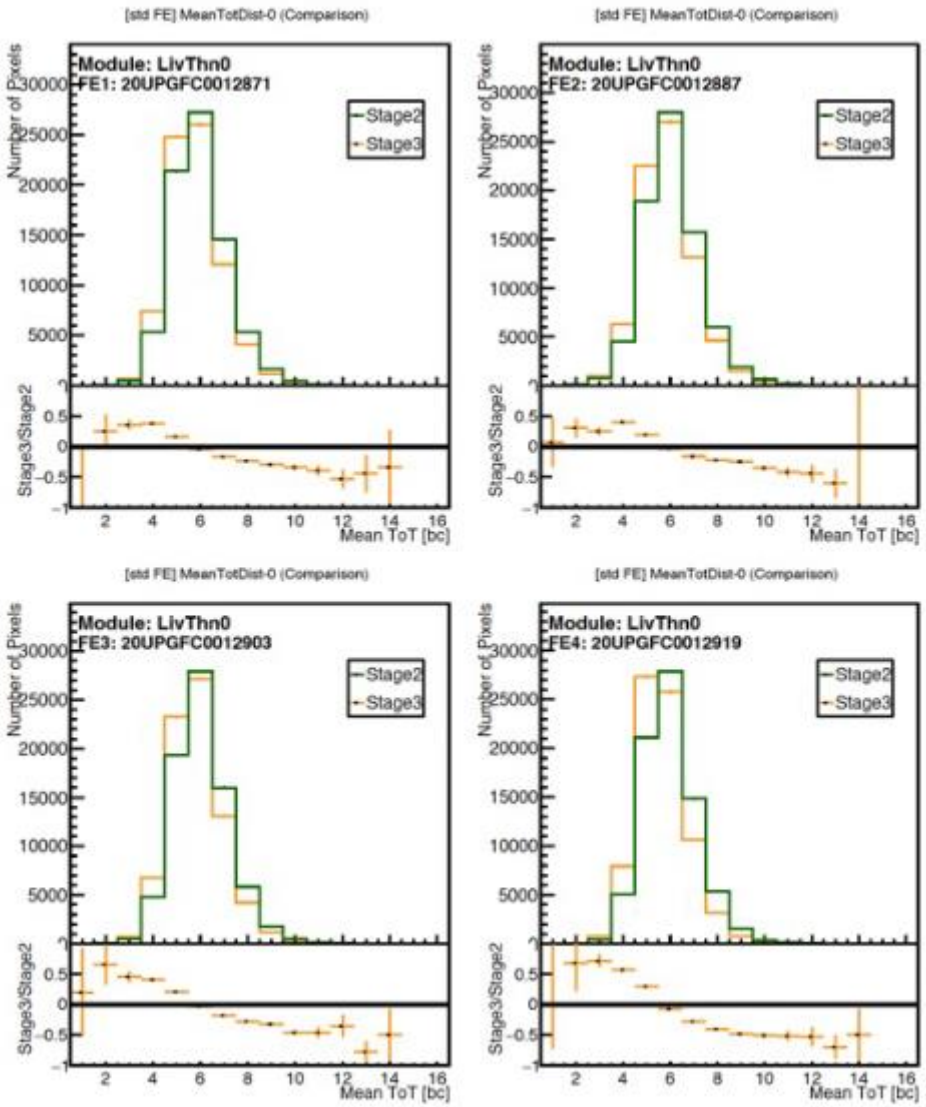






- Taking one module as representative for all results
- Scans for stages 1 (module build), 2 (RAL pre loading), 3 (RAL post loading), 5 (Liv serial power chain)
- Plots show number of good pixels

Readout characterization (ToT)



- Taking one module as representative for all results
- Scans for stages 1 (module build), 2 (RAL pre loading), 3 (RAL post loading), 5 (Liv serial power chain)
- Shift observed