HKROC : a modern front-end ASIC for the PMT readout of Cherenkov-based experiments

Rudolph Rogly - September 5th 2023

Technology in Instrumentation & Particle Physics Conference 2023

Outline

I. **Physics motivation**

II. ASIC design

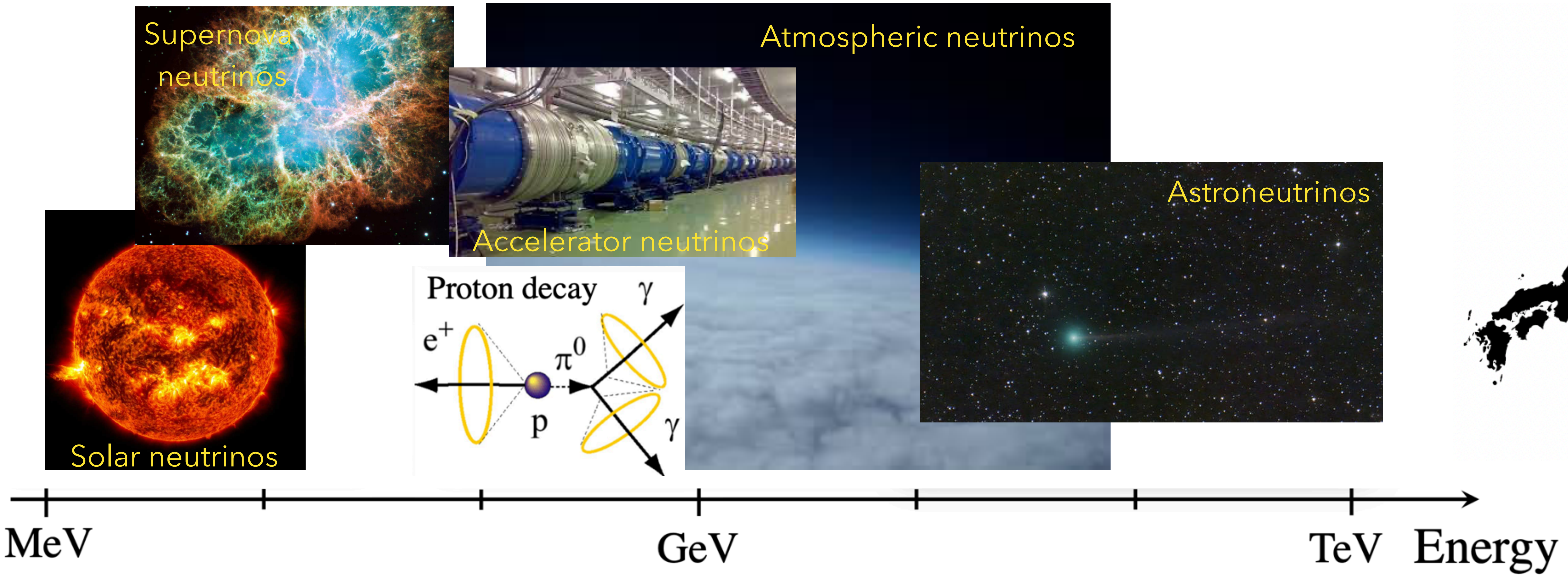
III. Characterization measurements

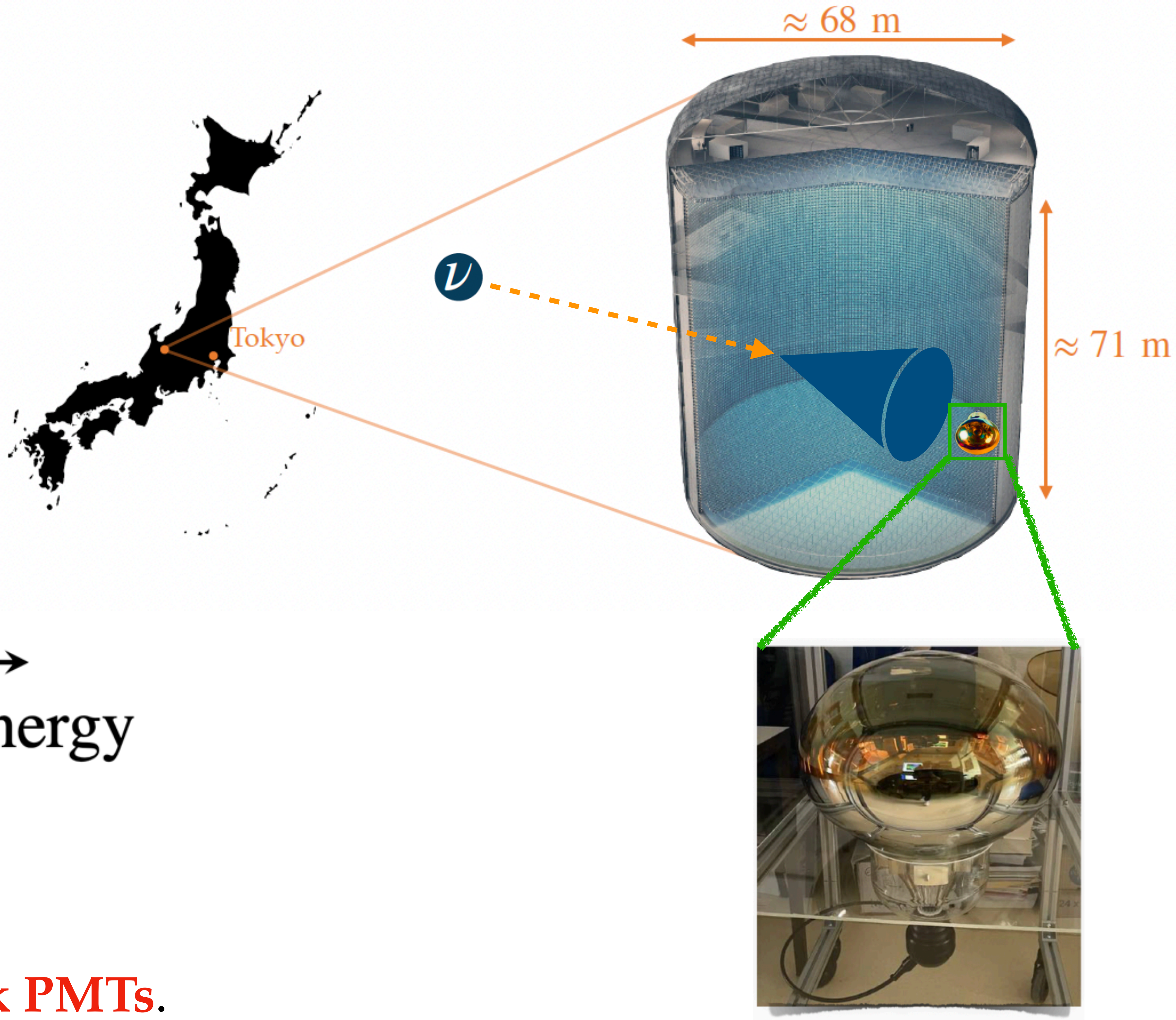
IV. Latest upgrades and prospects

Conclusions

I. Physics motivation

- **HKROC** (***H***yper ***K***amiokande ***R***ead-***O***ut ***C***hip) is a high-performance ASIC, originally designed for the PMT read-out of the Hyper Kamiokande experiment (2027).





Hamamatsu R12860-HQE

- Hyper Kamiokande is a multi-purpose Cherenkov-based experiment with:
  - ➡ Real time measurement of vertex, direction, energy of impinging particles.
  - ➡ Multi-channel read-out of the Cherenkov signal of interacting particles, with **~20k PMTs**.
  - ➡ Wide energy range, **from MeV to TeV**.
  - ➡ Event rates **up to 1 MHz** (close supernova burst, e.g. Betelgeuse).

From **Physics program** *to* **Electronics specifications**

1p.e. ↔ 2pC

Physics constraints	Electronics requirements
Low power consumption	< 1 W / channel
Detect synchronous & asynchronous events (accelerator/atmospheric/solar/supernova neutrinos, p decay)	Auto-triggering capability
Detect close supernova without event loss	Dead time < 1 μs
Low energy events detection (e.g. solar/supernova neutrinos)	Detection threshold: 1/6 p.e.
Detection of events from MeV to TeV	Dynamic range up to 1250 p.e.
Electronics time resolution < PMT time resolution (1.3 ns)	Time resolution < 300 ps for 1 p.e.
Excellent energy reconstruction capability	Charge linearity & resolution ~1%

While HK physics has driven the design, HKROC will not be deployed there.

Yet, its performance exceeds HK requirements and it is very flexible by design.

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HKROC building blocks

Main charasteristics

- ASIC in TSMC 130 nm node.
- 36 channels ↔ **12 PMTs / ASIC**.
  - ➡ *High gain* : up to 35 p.e. (70 pC)
  - ➡ *Medium gain* : up to 350 p.e. (700 pC)
  - ➡ *Low gain* : **up to 1250 p.e. (2500 pC)**
- Low power: **10 mW / channel**.

Measurements

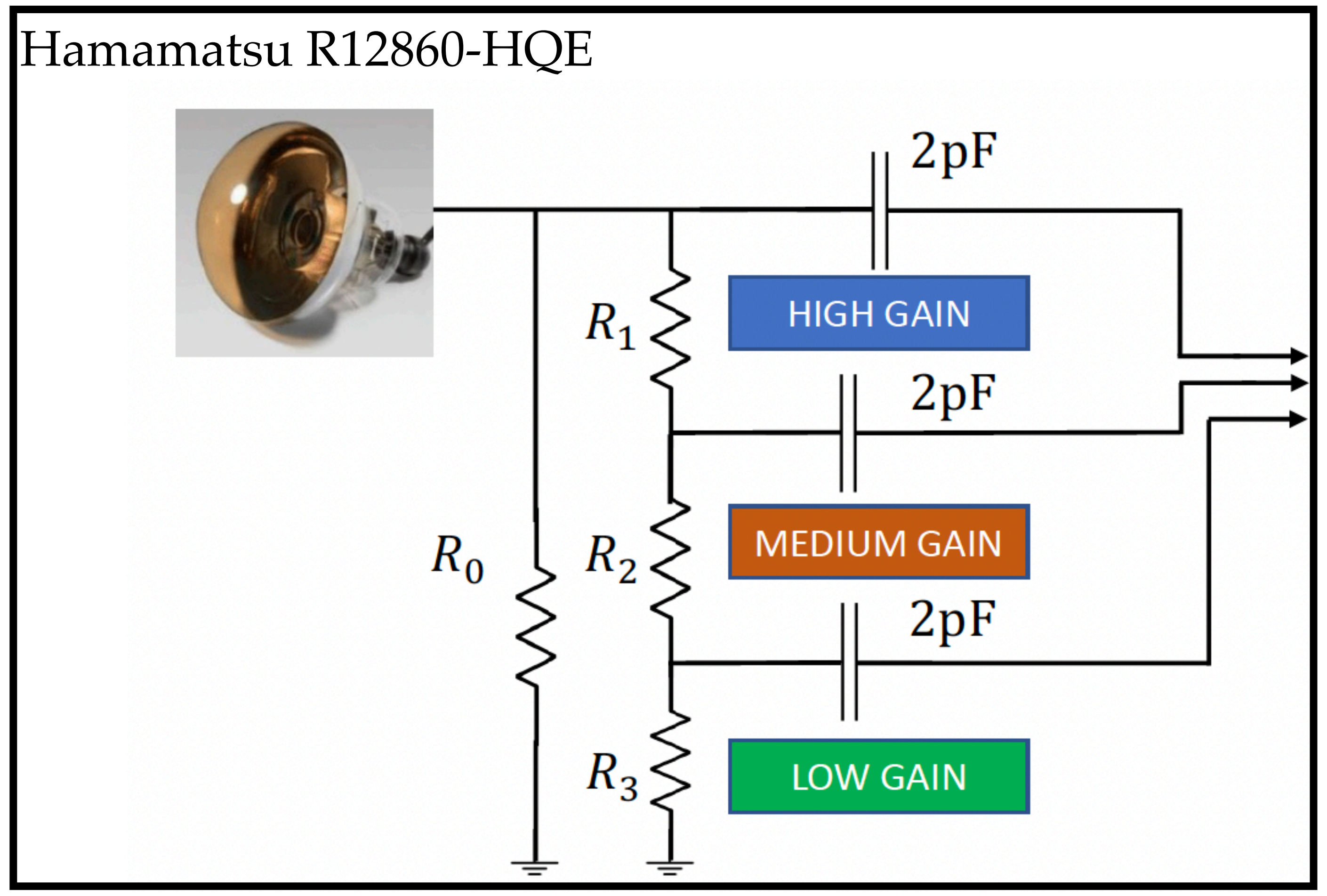
- **Slow path** with shaper: **10b SAR-ADC** for charge measurement **@ 40MHz**, dynamic range defined by the voltage divider and pre-amp. gain.
- **Fast path: 10b TDC** for time measurement, **LSB = 25 ps**.

Readout

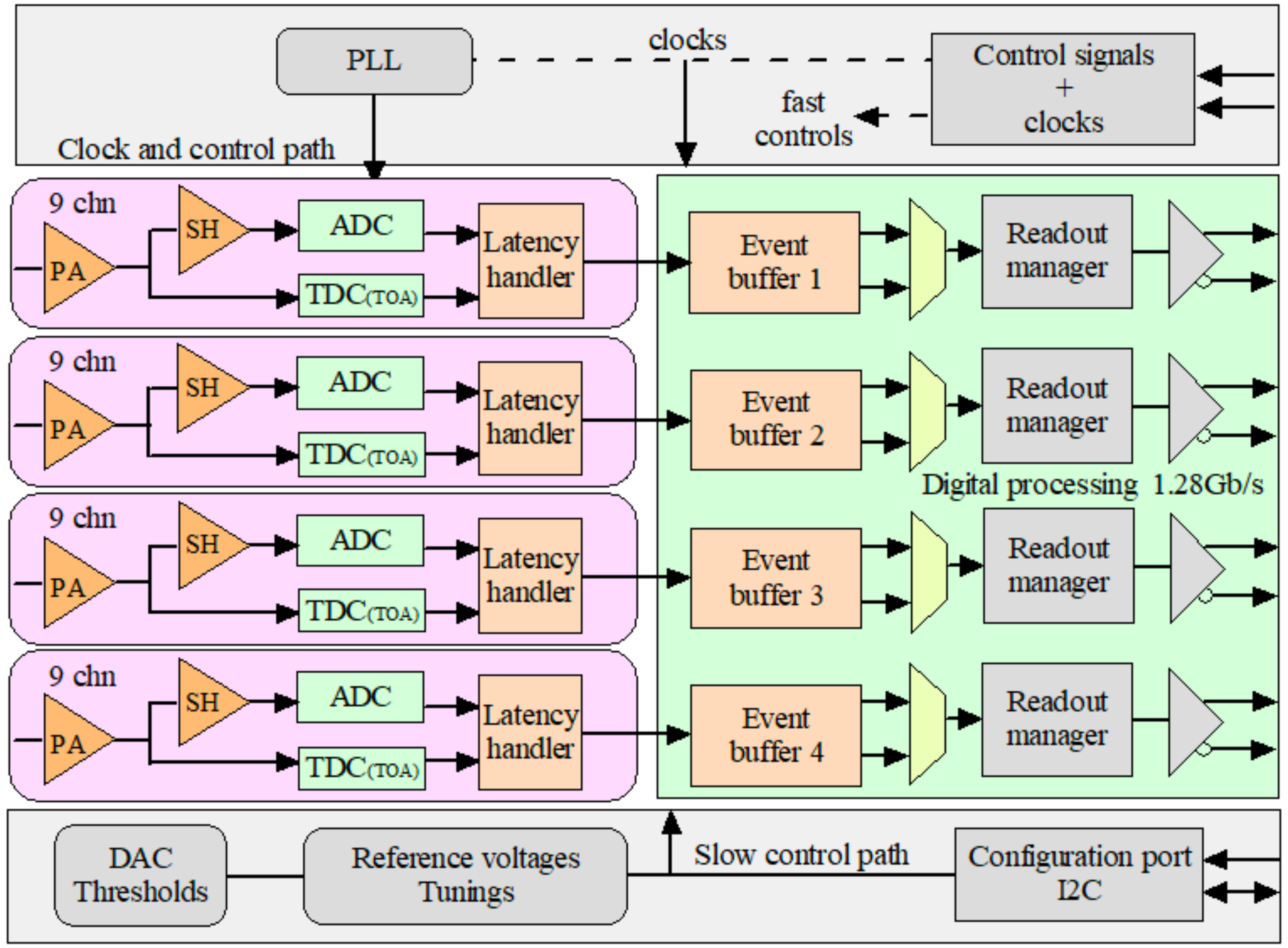
- **4 readouts / ASIC** : 1 readout ↔ 3 PMTs, i.e. 9 channels.
- High speed links (**1.28 Gb/s**).

Control

- 320 MHz fast commands.
- I2C protocol for slow control.



On-board analog input signal

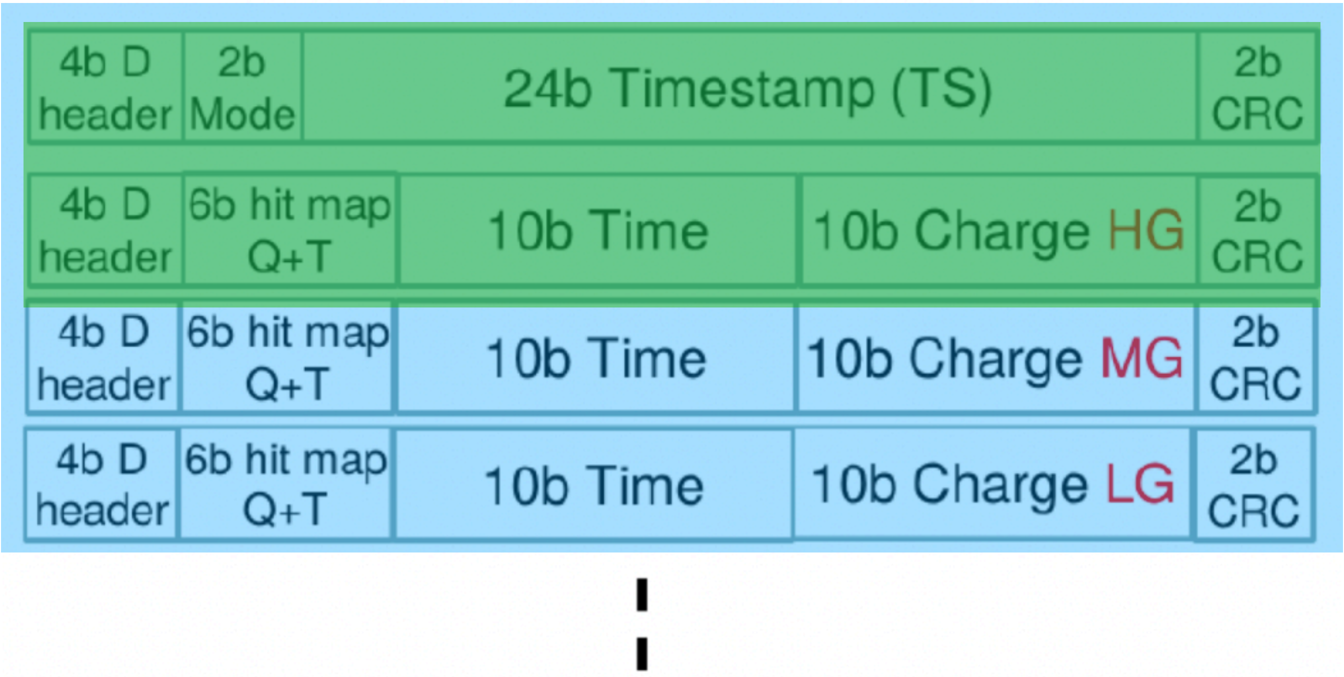


HKROC digitization

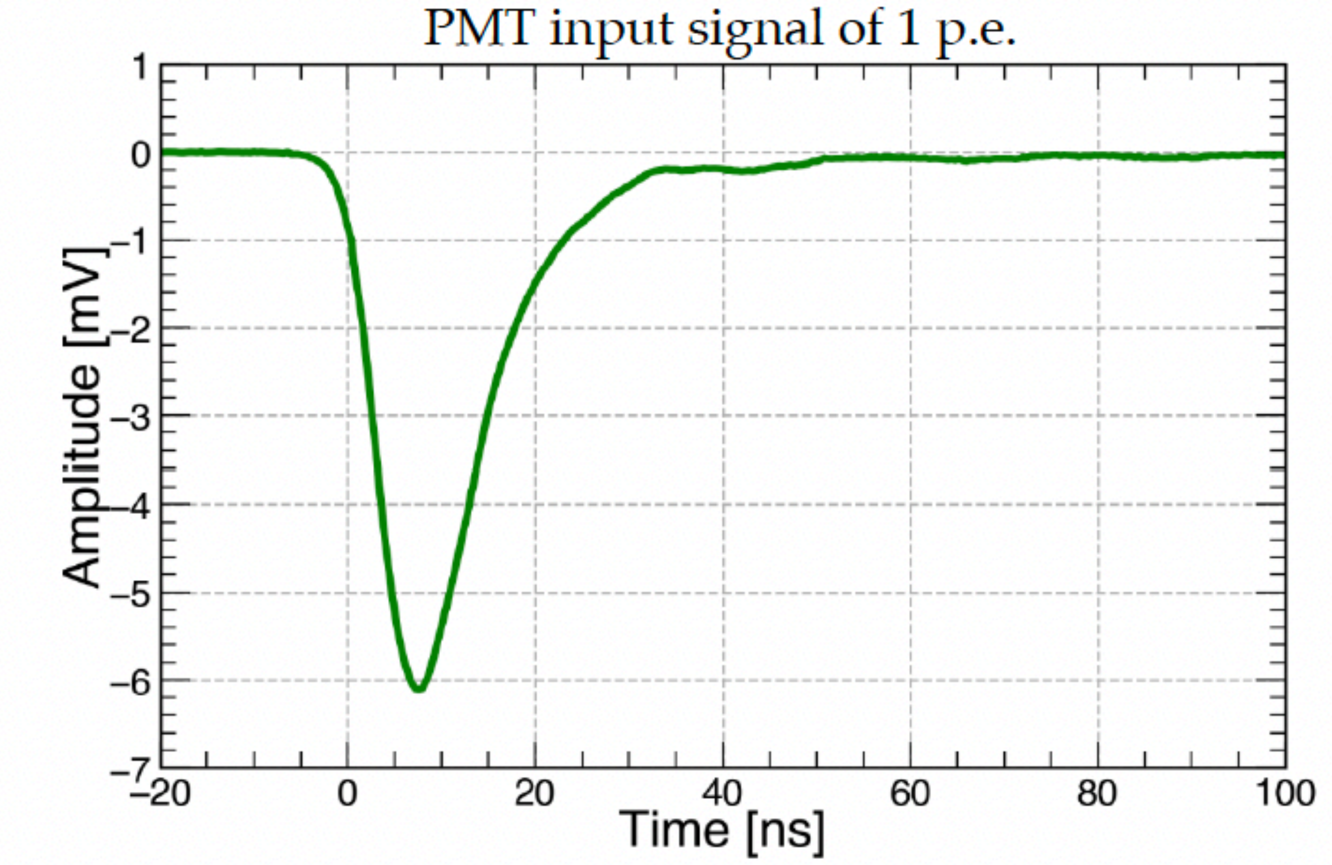
HKROC key features

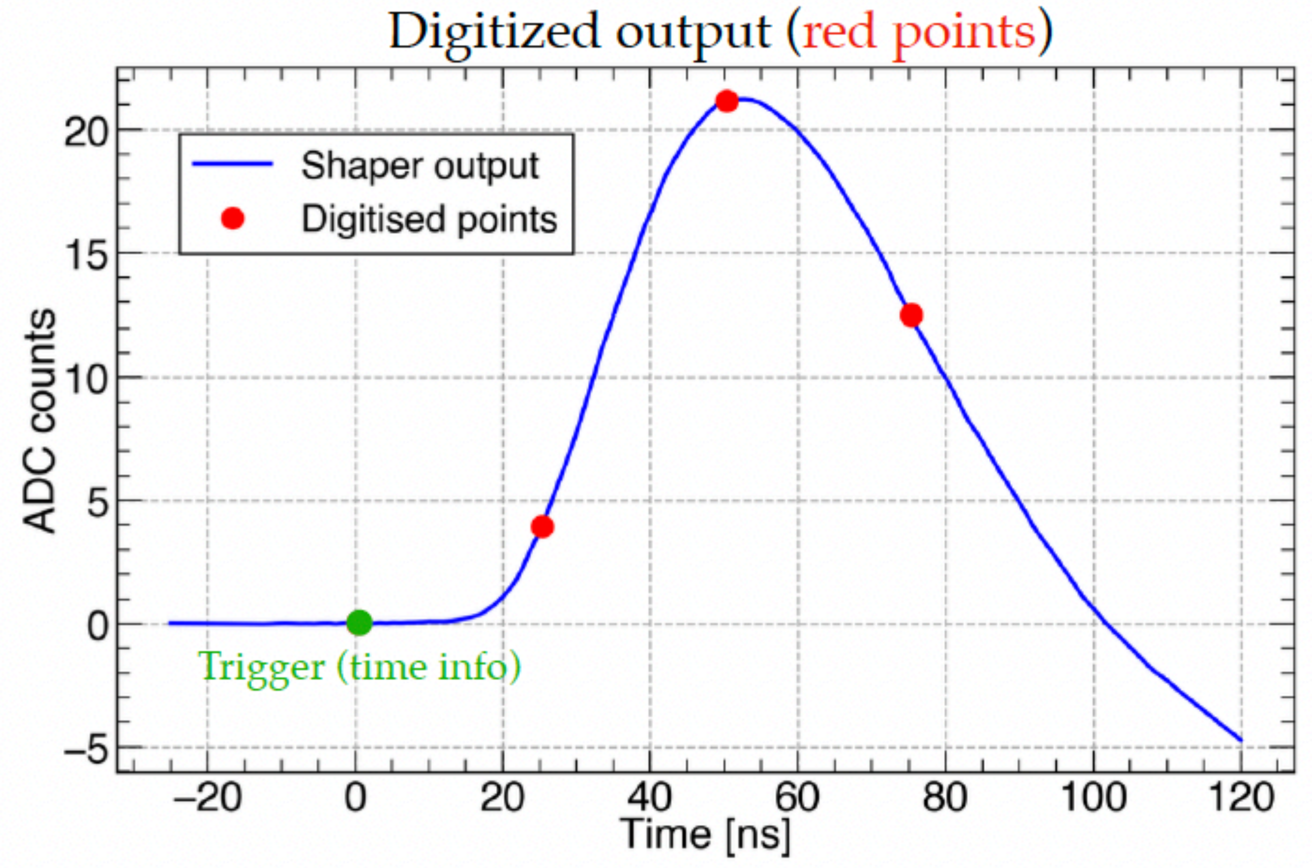
- HKROC has **3 operating modes for hit rate optimization**:
  - ➡ ***Normal mode***: 10 words of 32 bits.
  - ➡ ***Supernova mode*** (focus on HG only, i.e. low energy): 4 words of 32 bits.
  - ➡ ***Ultra-fast mode*** (characterization mode): 1 word of 32 bits.

Full snapshot



- HKROC is a **low-power waveform digitizer**: for each trigger, N points are sampled @ 40 MHz (= 25 ns timestamp) and saved in memory. N is tunable by slow control (1 to 7).





➡ Time + shape information (peaking time of shaper output ~30ns) give **pile-up discrimination** capabilities **for events separated by ~30ns** *(can go even lower if needed)*.

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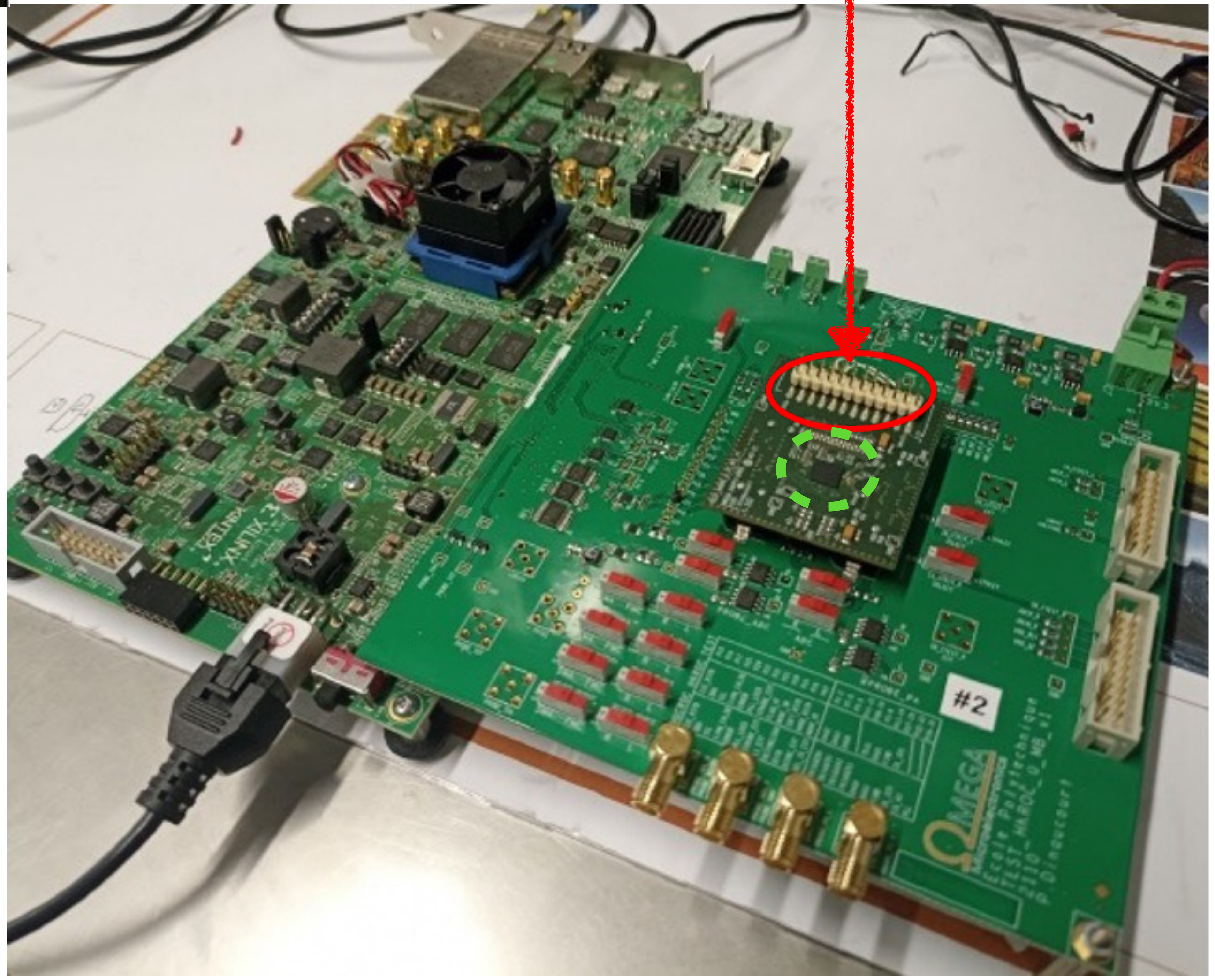
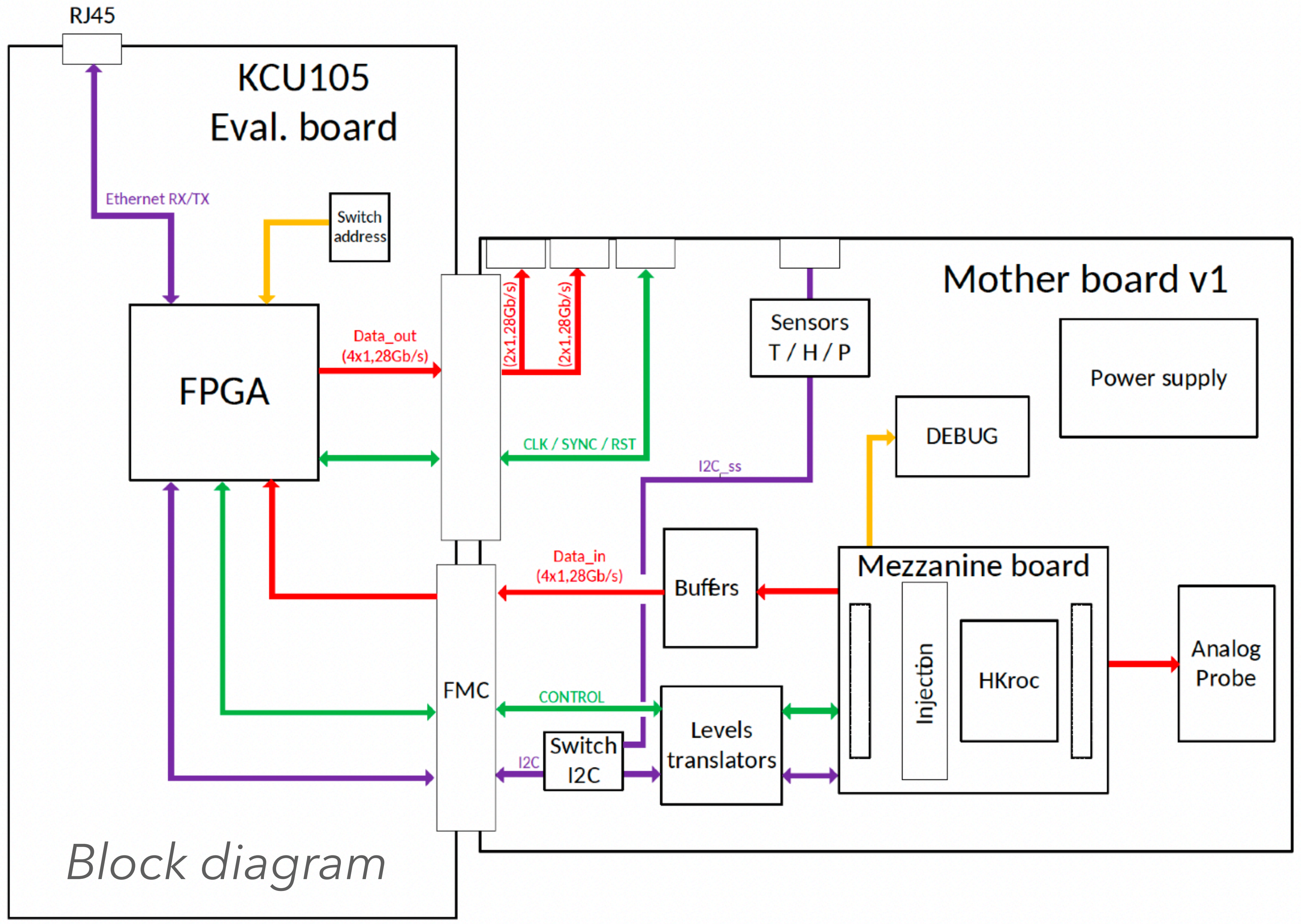
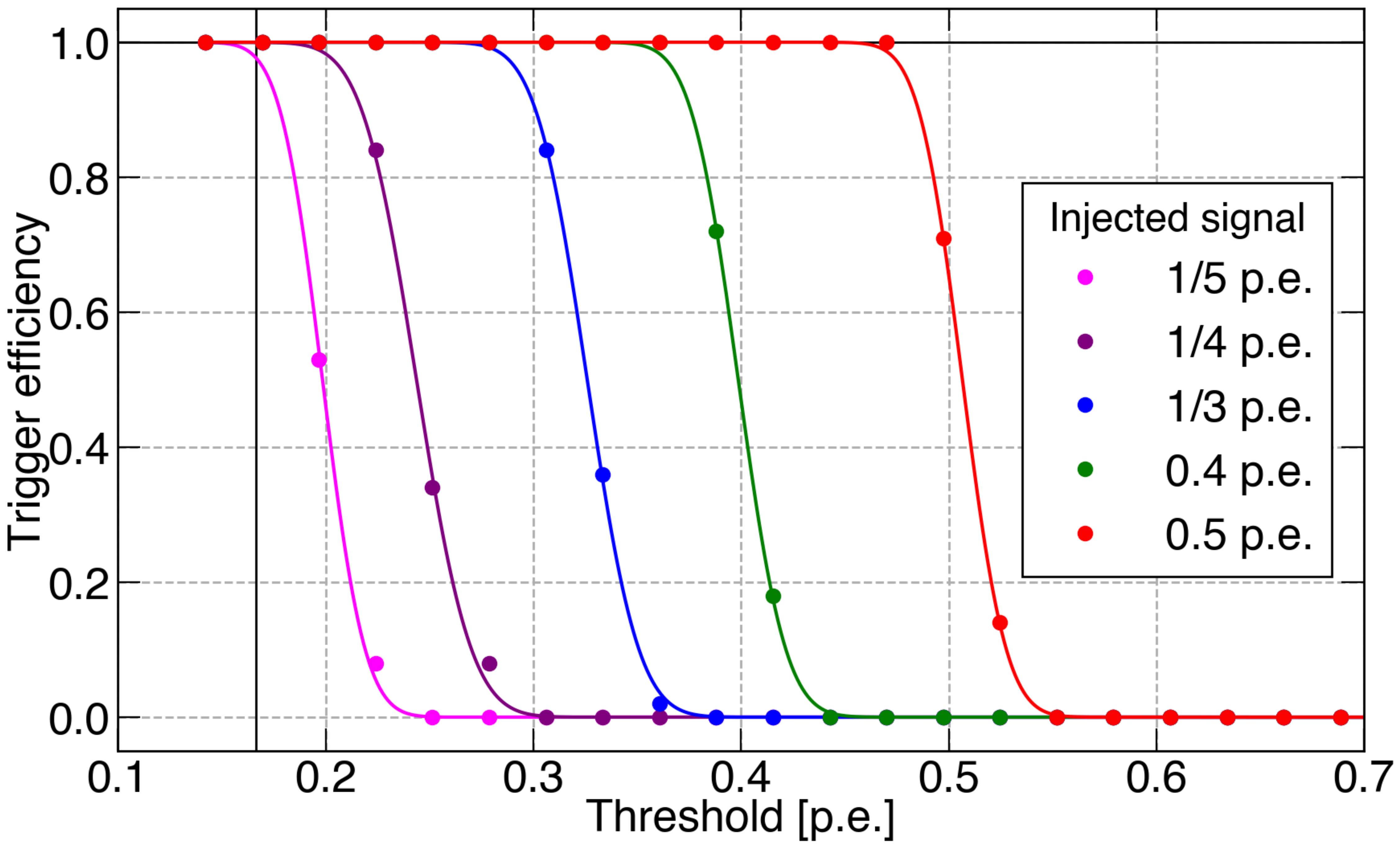
Test bench

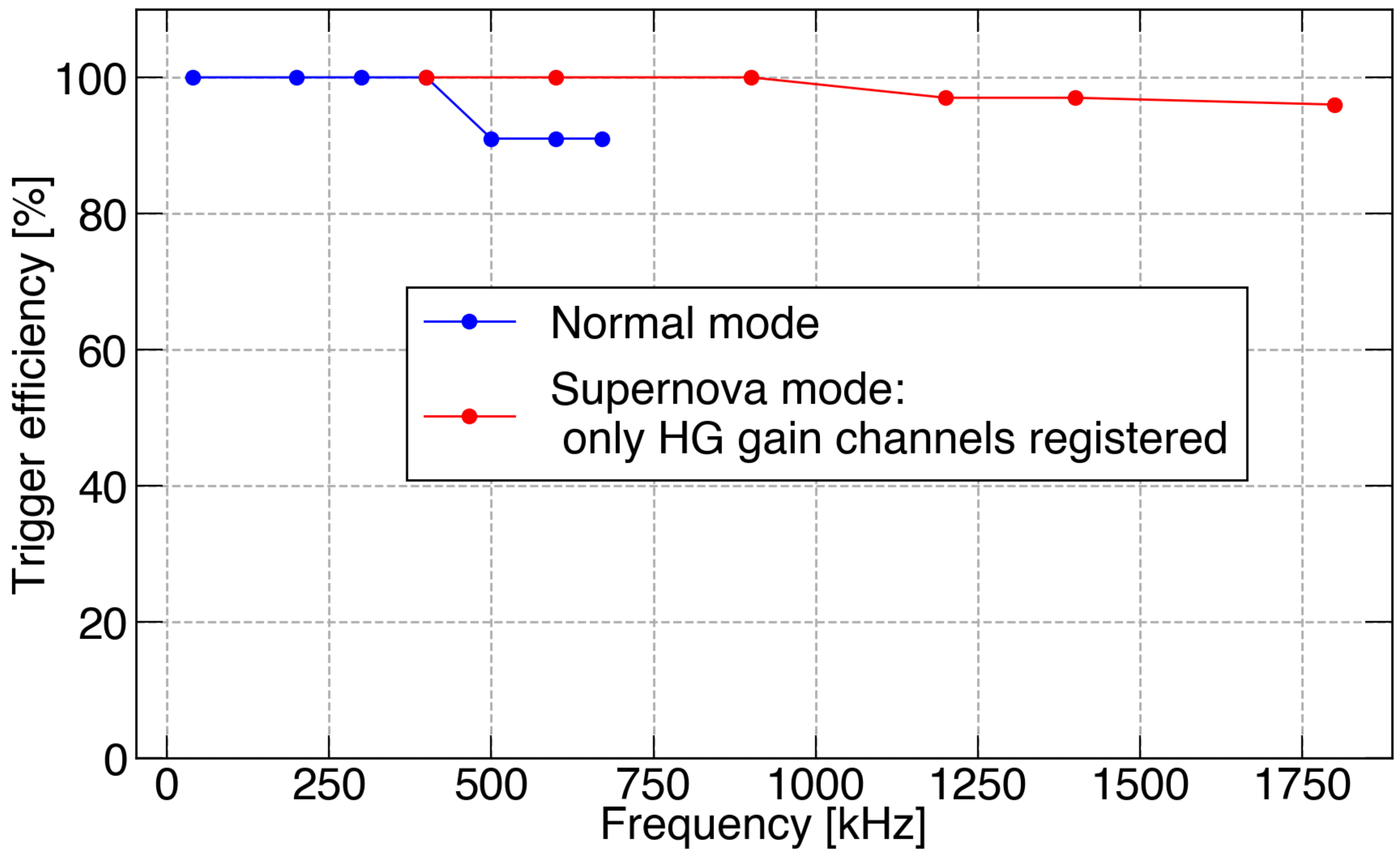
Test pulse input





Trigger performance

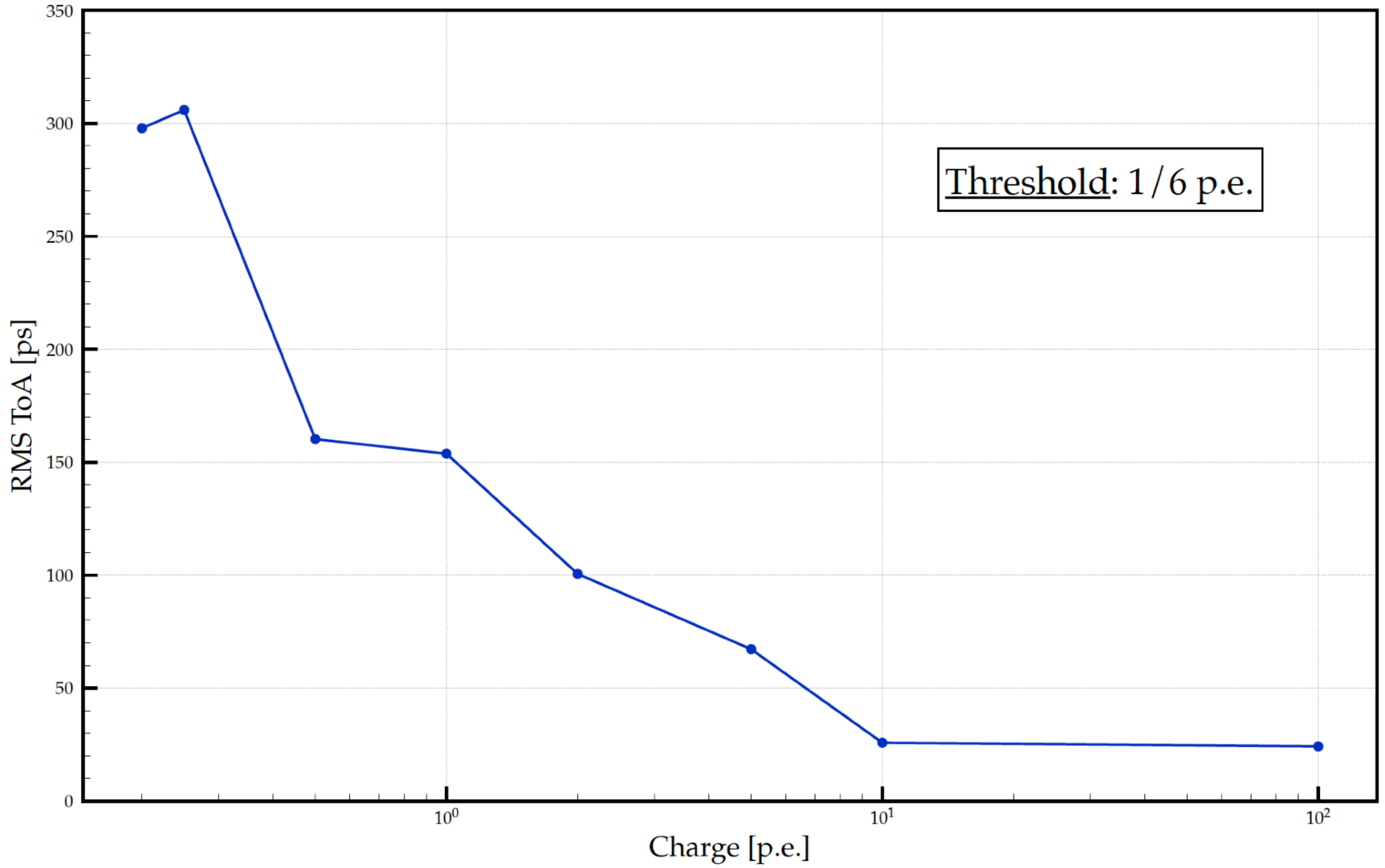




- Trigger threshold = 1/6 p.e. ⟶ **> 90% efficiency for signal as low as 1/5 p.e.**
- **Noise** amplitude **< 1/22 p.e.**

- Maximal hit-rate with 100% efficiency:
  ➡ ***Normal mode* → 415 kHz.**
  ➡ ***Supernova mode* → 950 kHz.**
- **Automatic switch** between the two modes, when the memory is almost full (tunable).

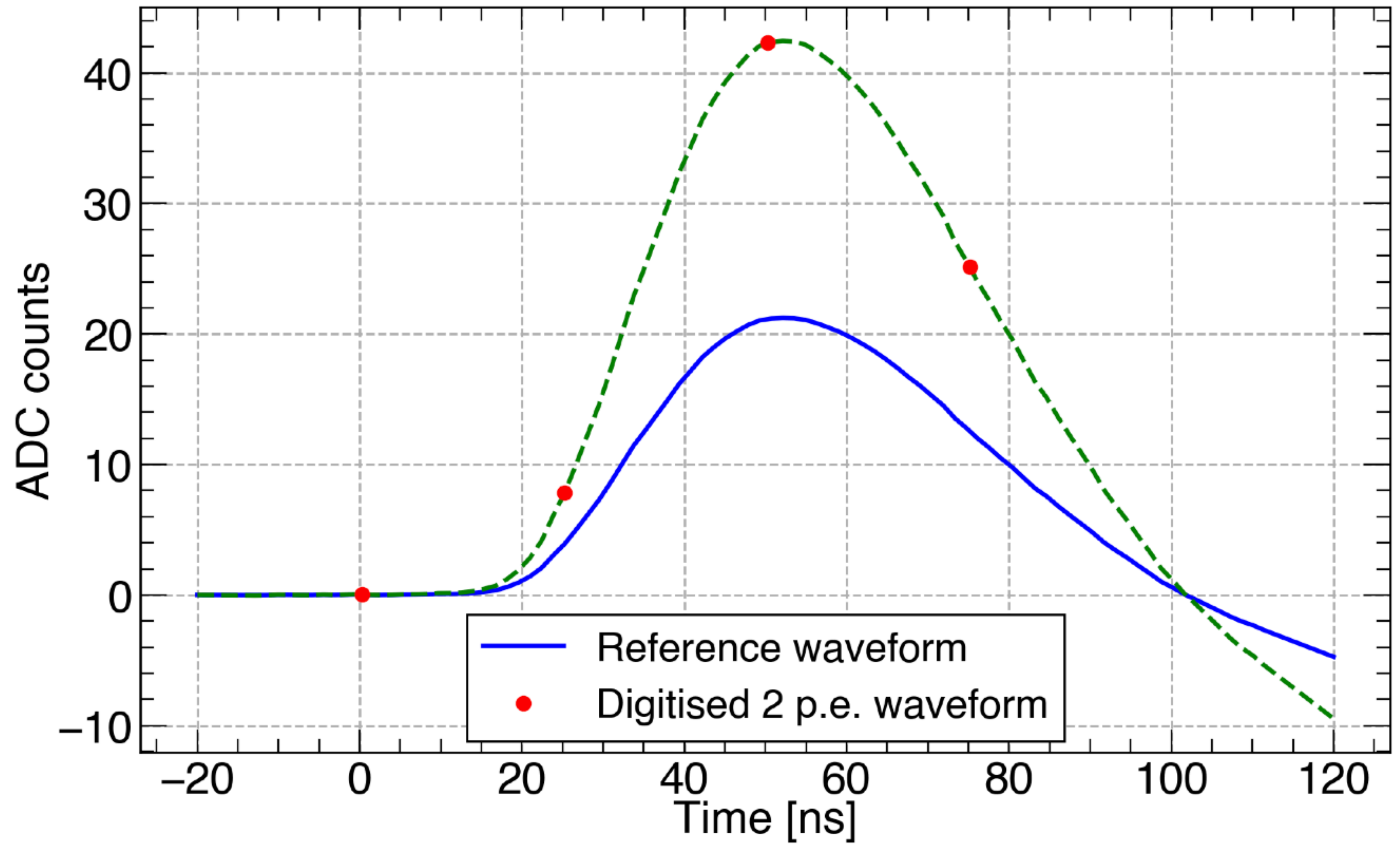
Time resolution



TDC resolution (1/6 p.e. threshold):

~150 ps std @ 1 p.e.
25 ps std @ > 10 p.e.

Charge reconstruction performance



Charge reconstruction in 2 steps **(FPGA-compliant)**

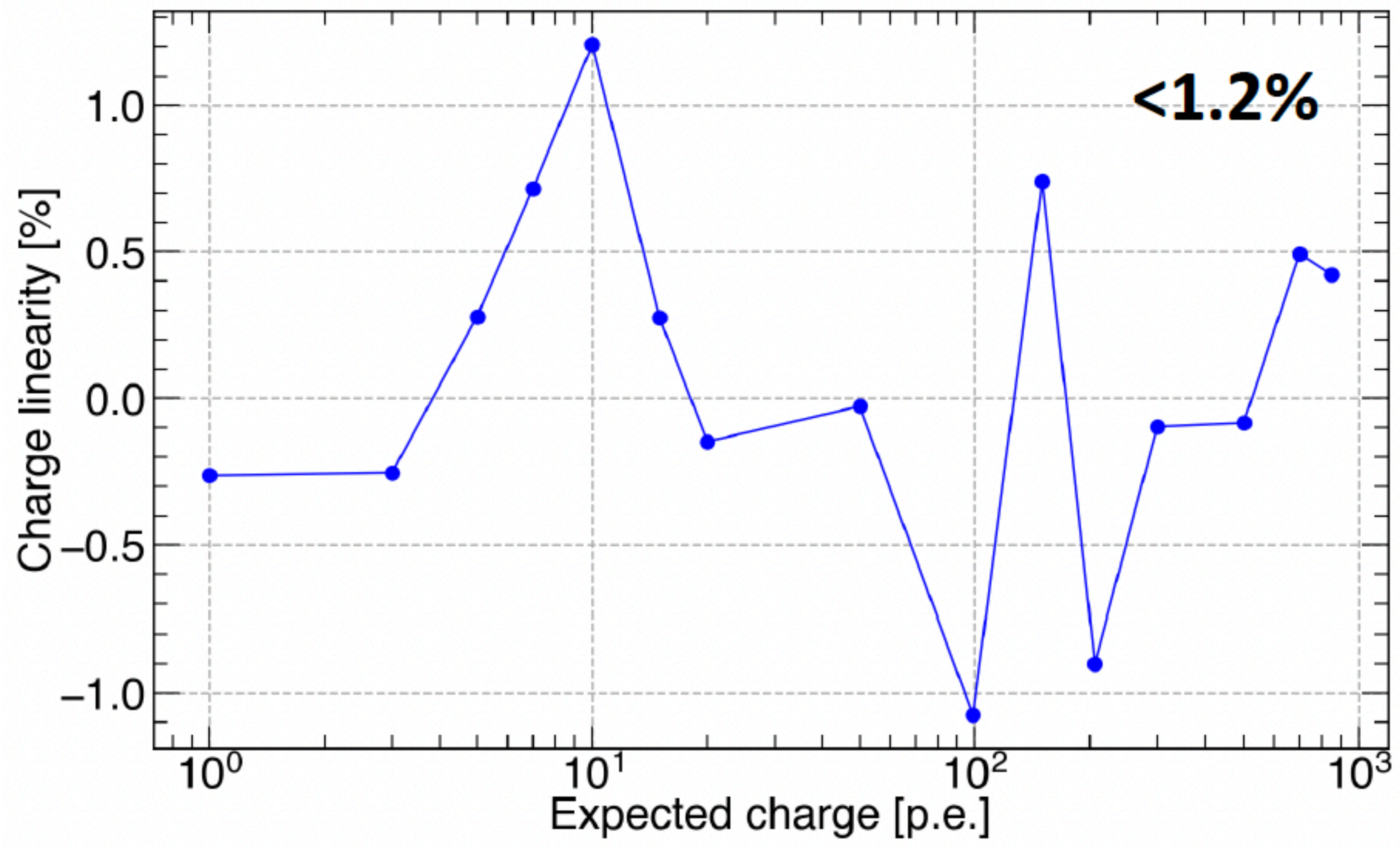
1. Build a **reference waveform** to calibrate each channel:
   - ➡ High gain channel : $q_{ref} = 1$. p.e.
   - ➡ Medium gain channel : $q_{ref} = 20$ p.e.
   - ➡ Low gain channel : $q_{ref} = 200$ p.e.
2. Given a **digitized waveform**, find the associated charge q:

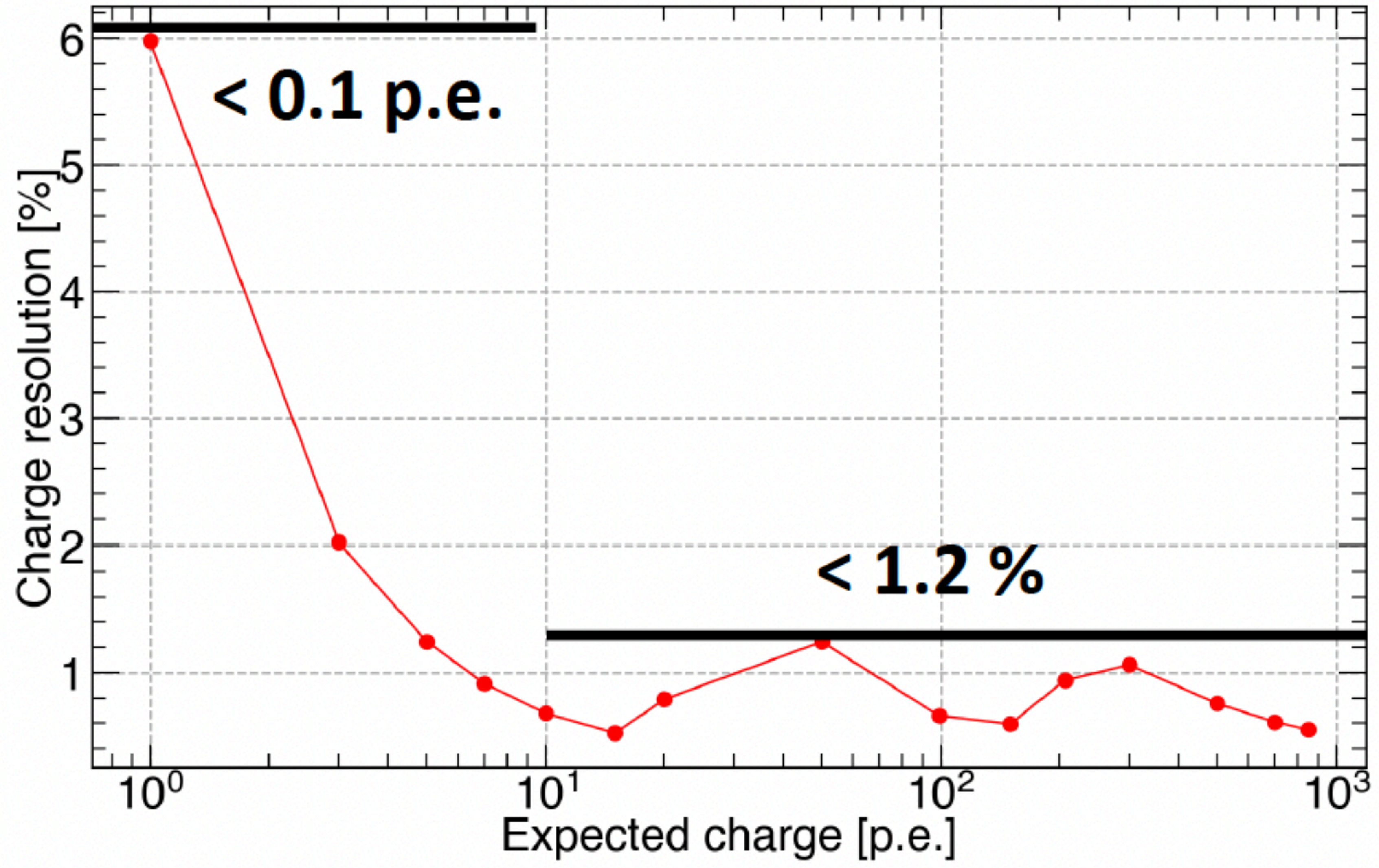
$$\chi^2(\alpha) = \sum_{i=1}^{N} \left(\frac{y_i - \alpha w_i}{\sigma_i} \right)^2$$

$$\rightarrow \frac{d\chi^2}{d\alpha} = 0 \iff \alpha = \frac{\sum_{i=1}^{N} \frac{y_i w_i}{\sigma_i^2}}{\sum_{i=1}^{N} \frac{w_i^2}{\sigma_i^2}} \implies q = \alpha q_{ref}$$

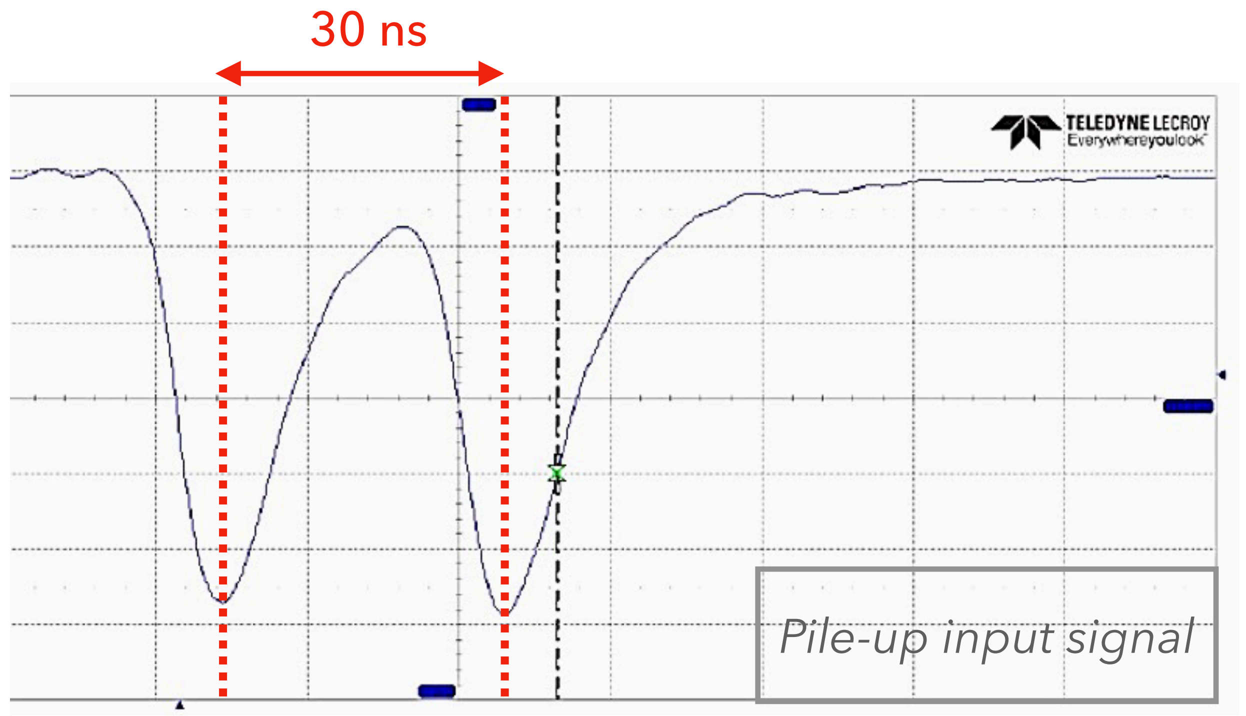
Charge linearity:
< 1.2 % for all charges

Charge resolution:
< 0.1 p.e. for charges < 10 p.e.
< 1.2 % for charges > 10 p.e.

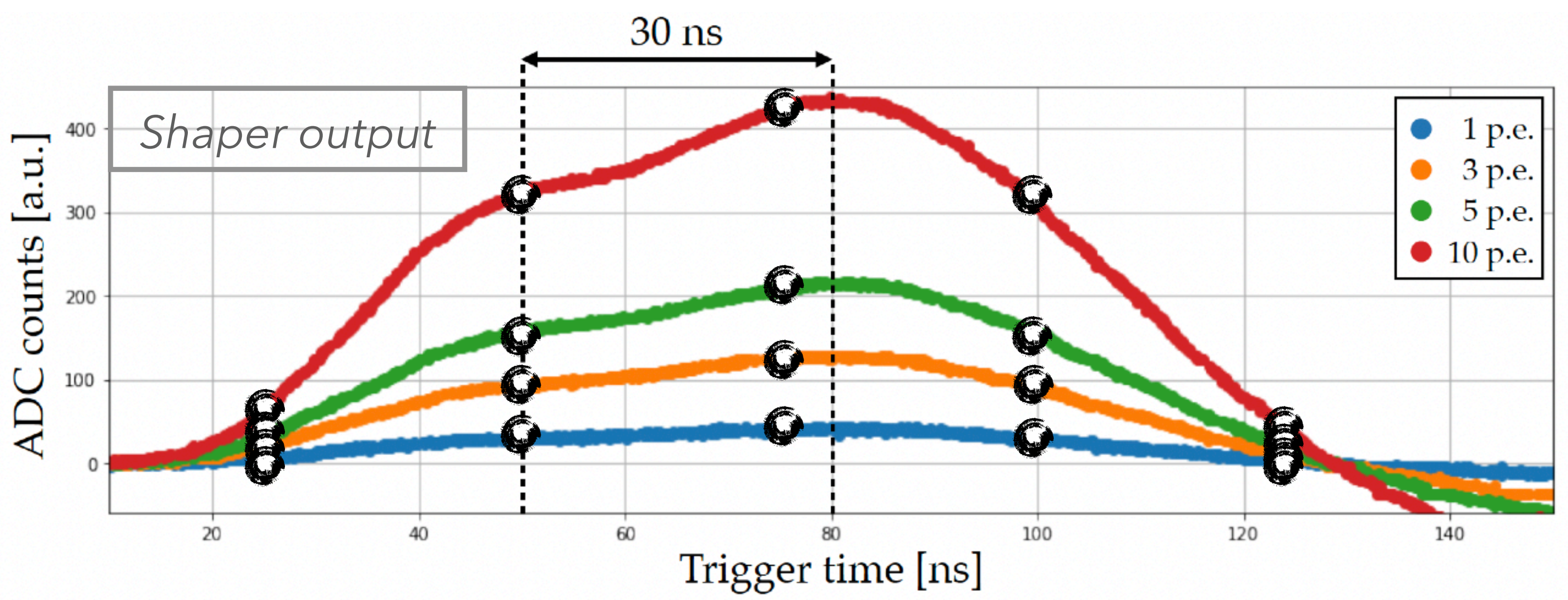




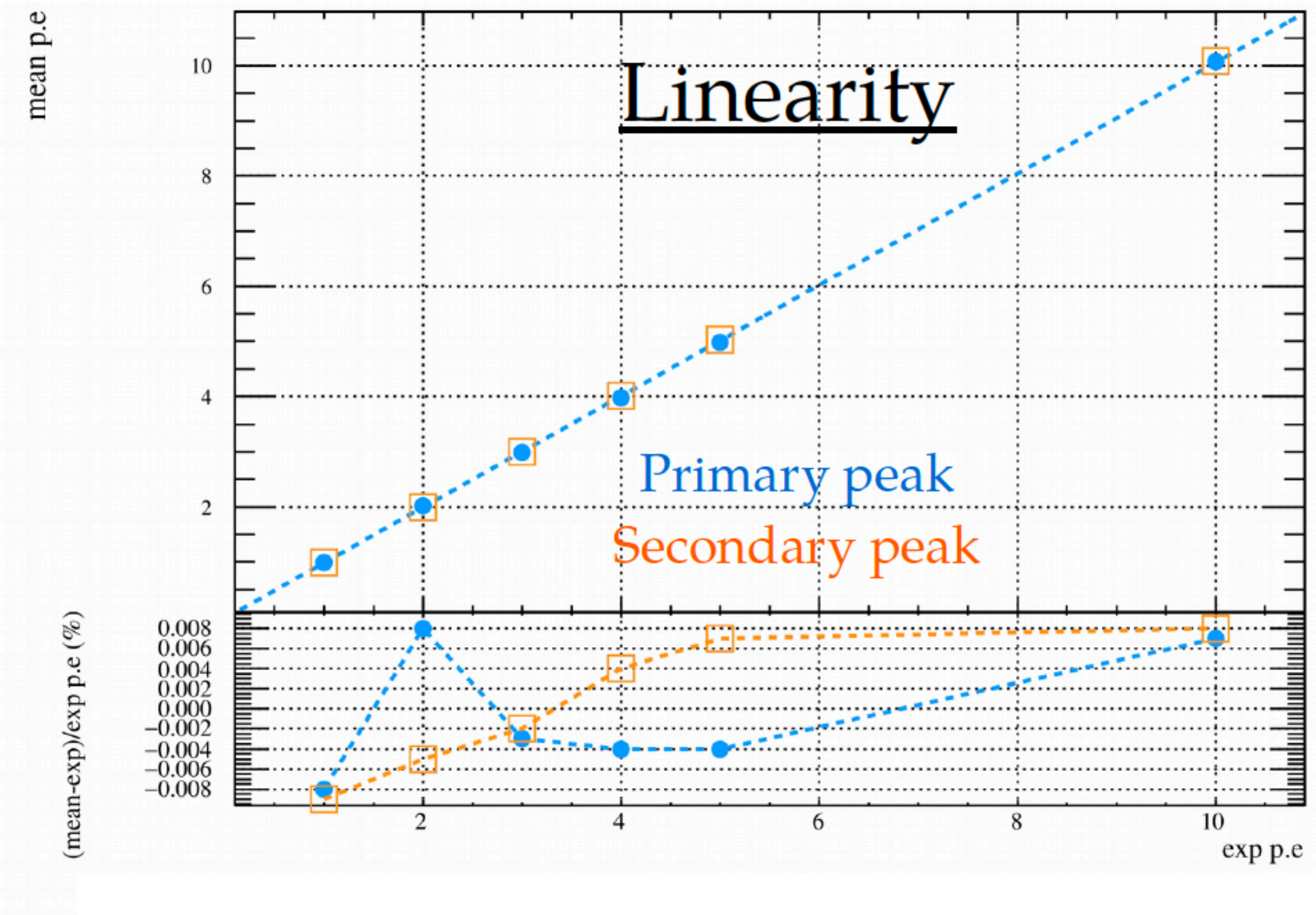
Pile-up & dead time

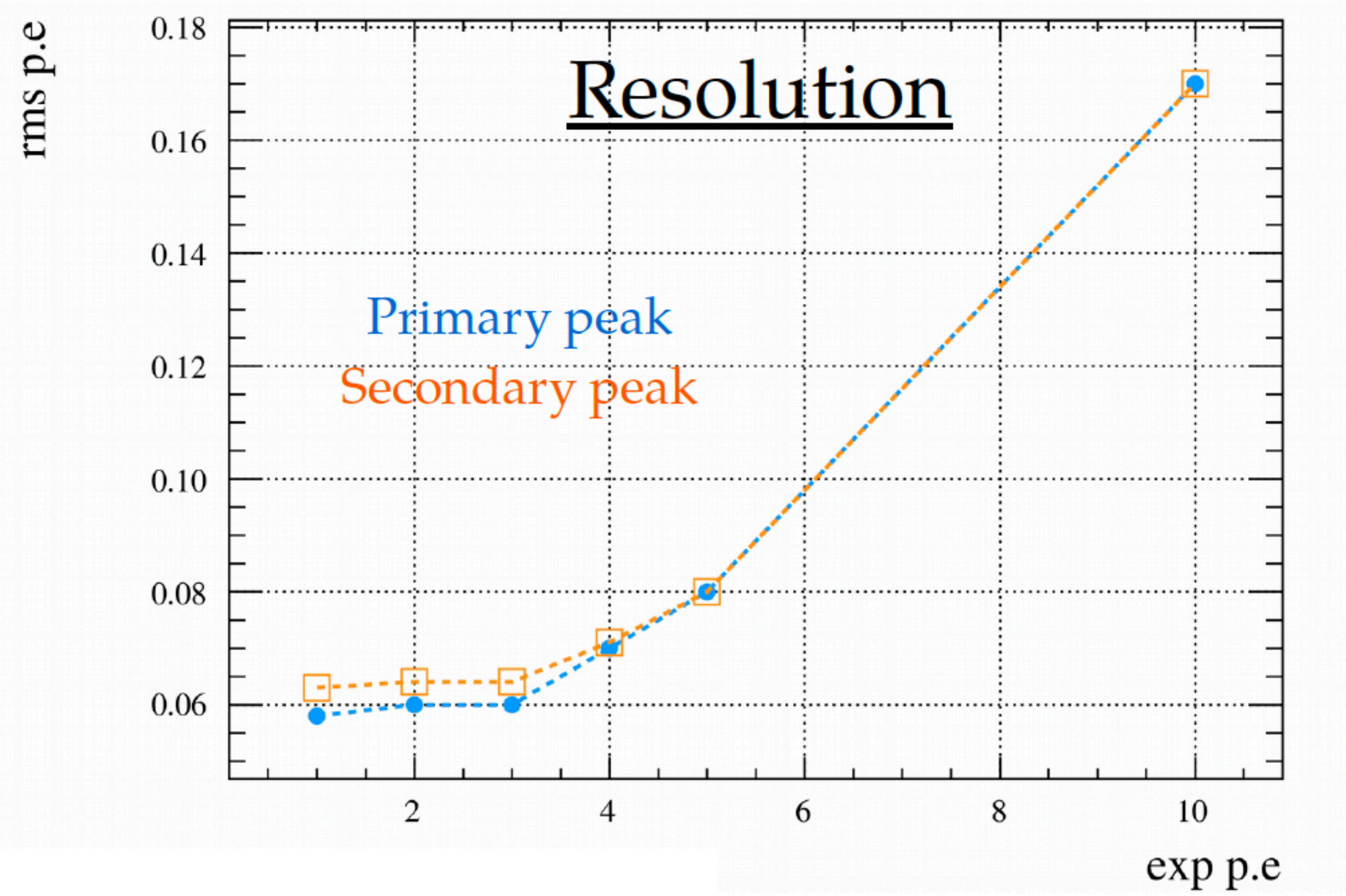


- Events on separate timestamps (25 ns-long) → **2 trigger times**.
- **Acquisition window dynamically extended** (N = 3 points / event).



- Charge reconstruction achieved with a joint fit: $\alpha w_i \leftarrow \alpha w_i + \beta w_{i-dt}$
- Accurate charge reconstruction of pile-up:
  - ➡ Charge linearity < $\sim 1\,\%$.
  - ➡ Charge resolution: < 0.1 p.e. for charges < 5 p.e.
    < 0.17 p.e. @ 10 p.e.





Capability to reconstruct events separated down to **30 ns** (**intrinsic dead time**).

IV. Latest upgrades and prospects

HKROC R&D

4 versions of the packaging ASIC + acquisition board so far, with:

- 2 ASIC versions:
  1. HKROC0.
  2. HKROC1b.
- 2 board versions:
  1. Flip chip on mezzanine daughter board (one conductive layer).
  2. BGA package on mother acquisition board (two conductive layers).

⟶ **For cross-talk mitigation (2023).**

HKROC0
2021/12

HKROC0-BGA
(x80) - 2022/06

HKROC1b-BGA
(x80) - 2022/12

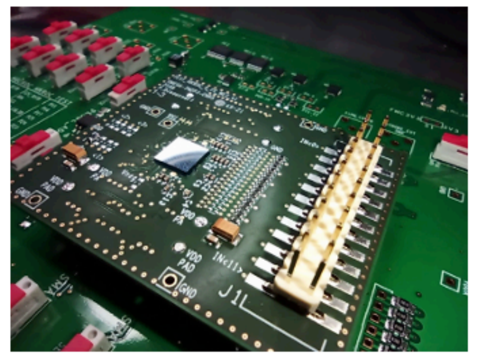
HKROC production
(x4000) - 2023/09

Mezzanine
daughter board

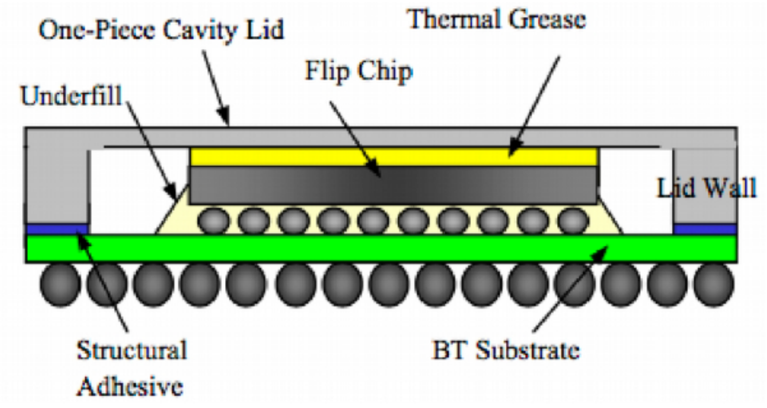
Acquisition
board

Acquisition board
with reconstruction

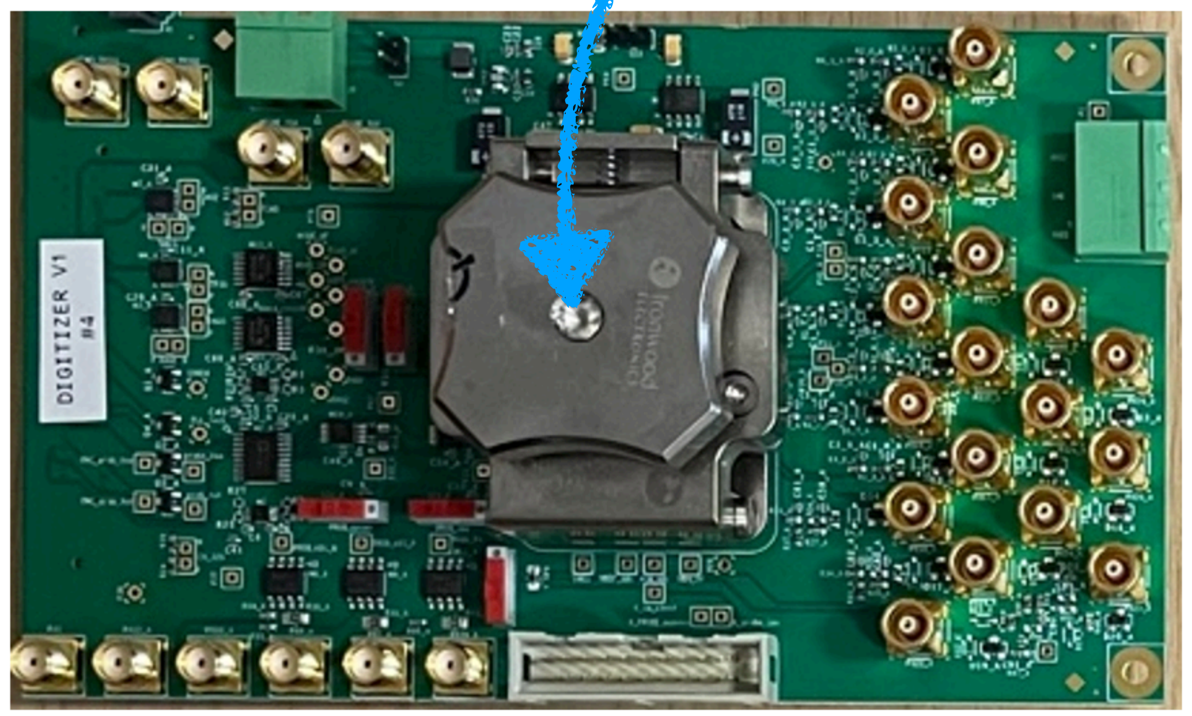
2021



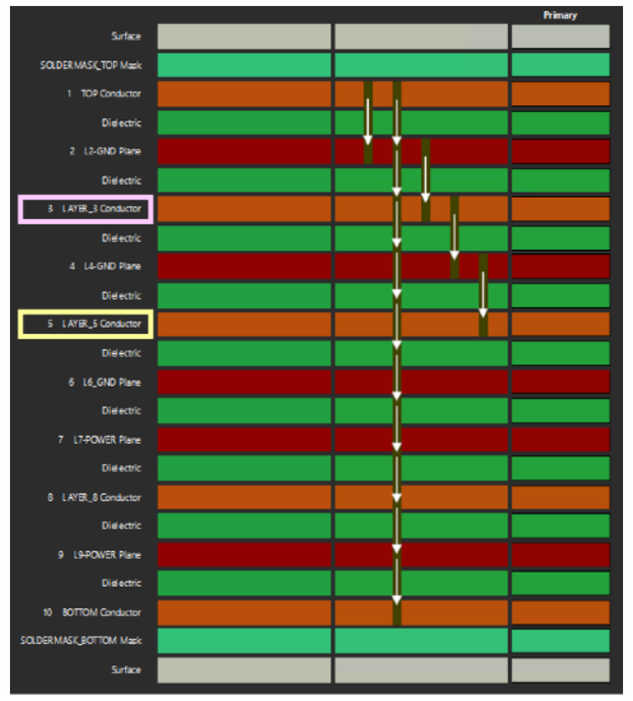
Naked HKROC
on mezzanine



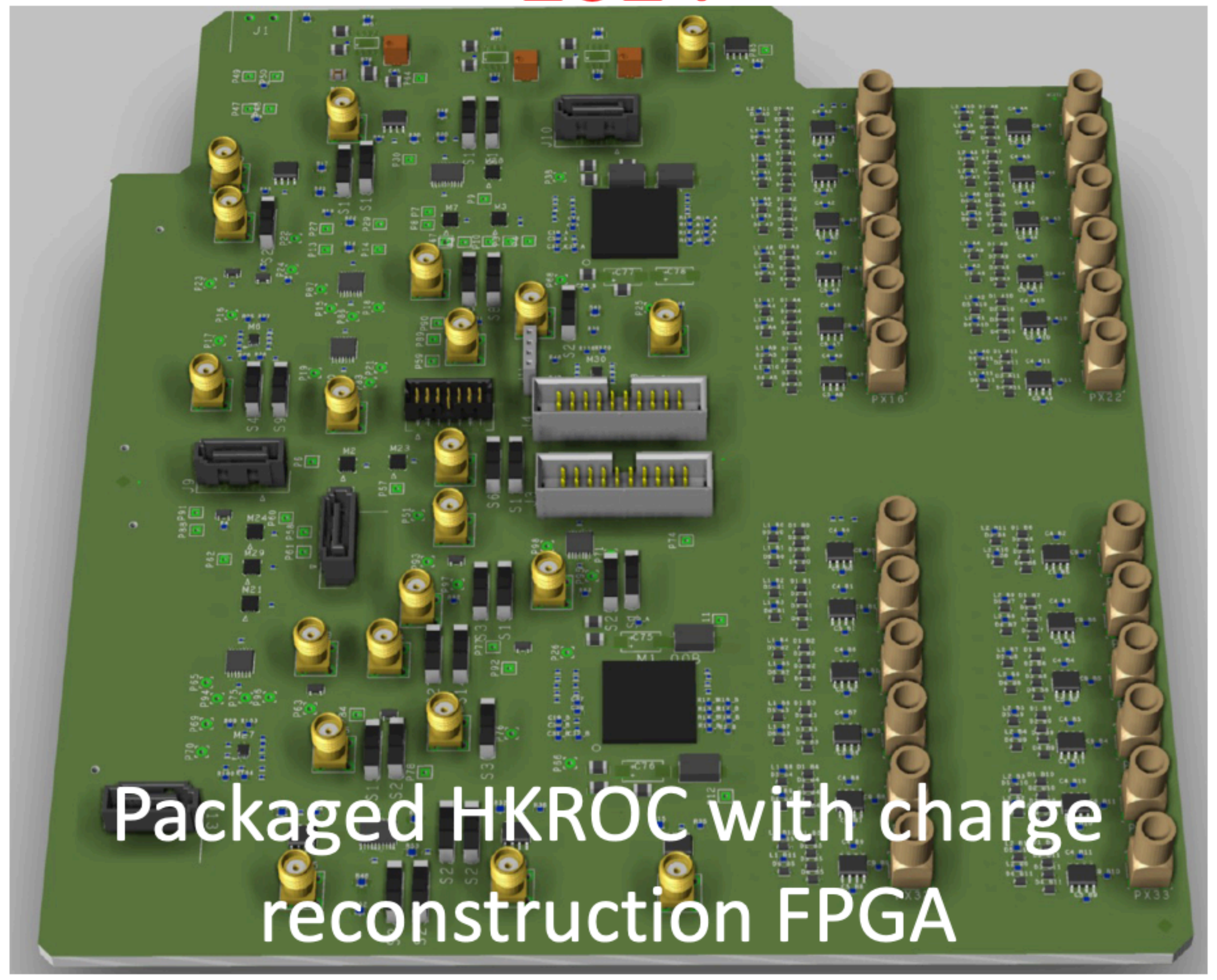
2022



Packaged HKROC with
acquisition board



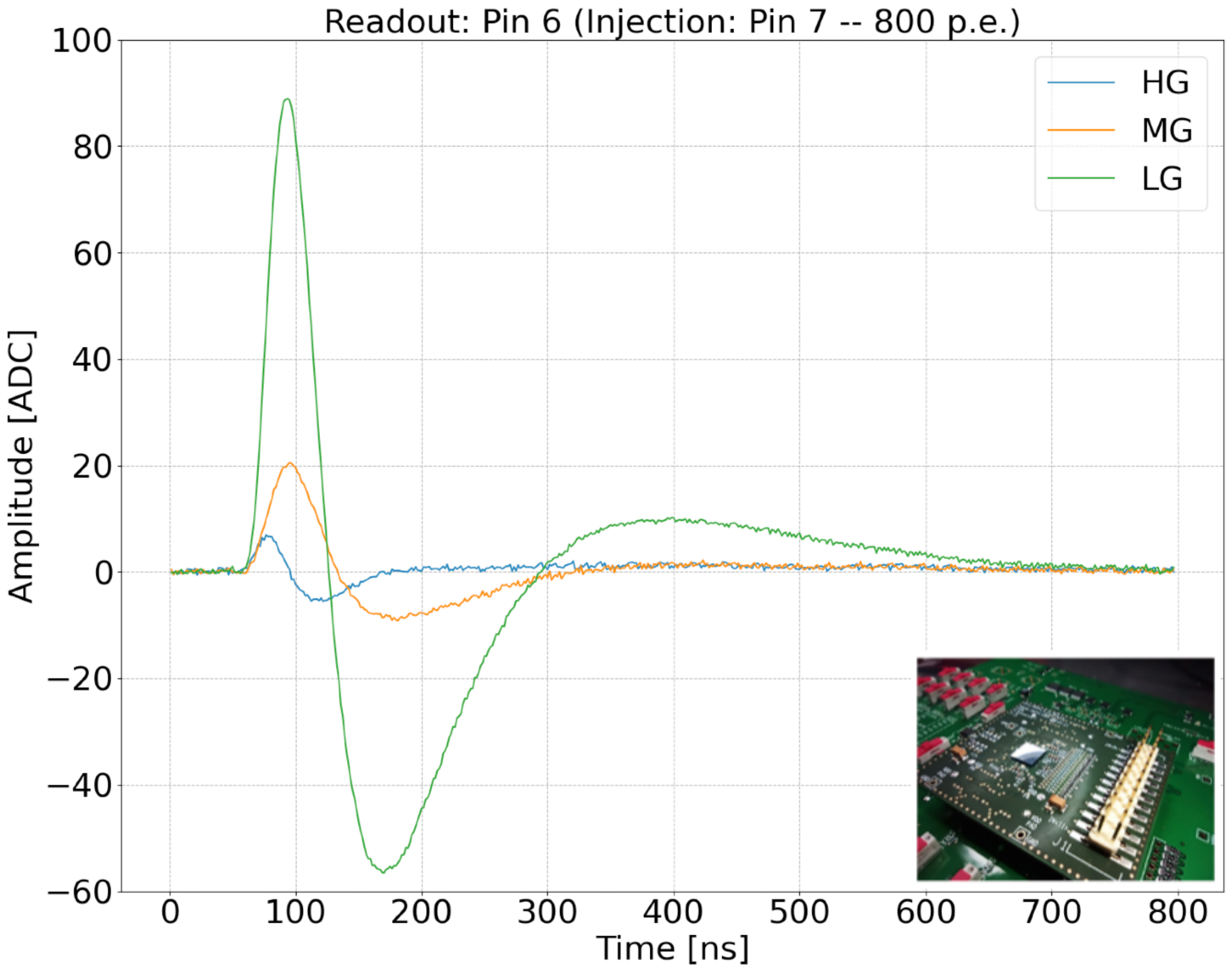
⟶ 2024

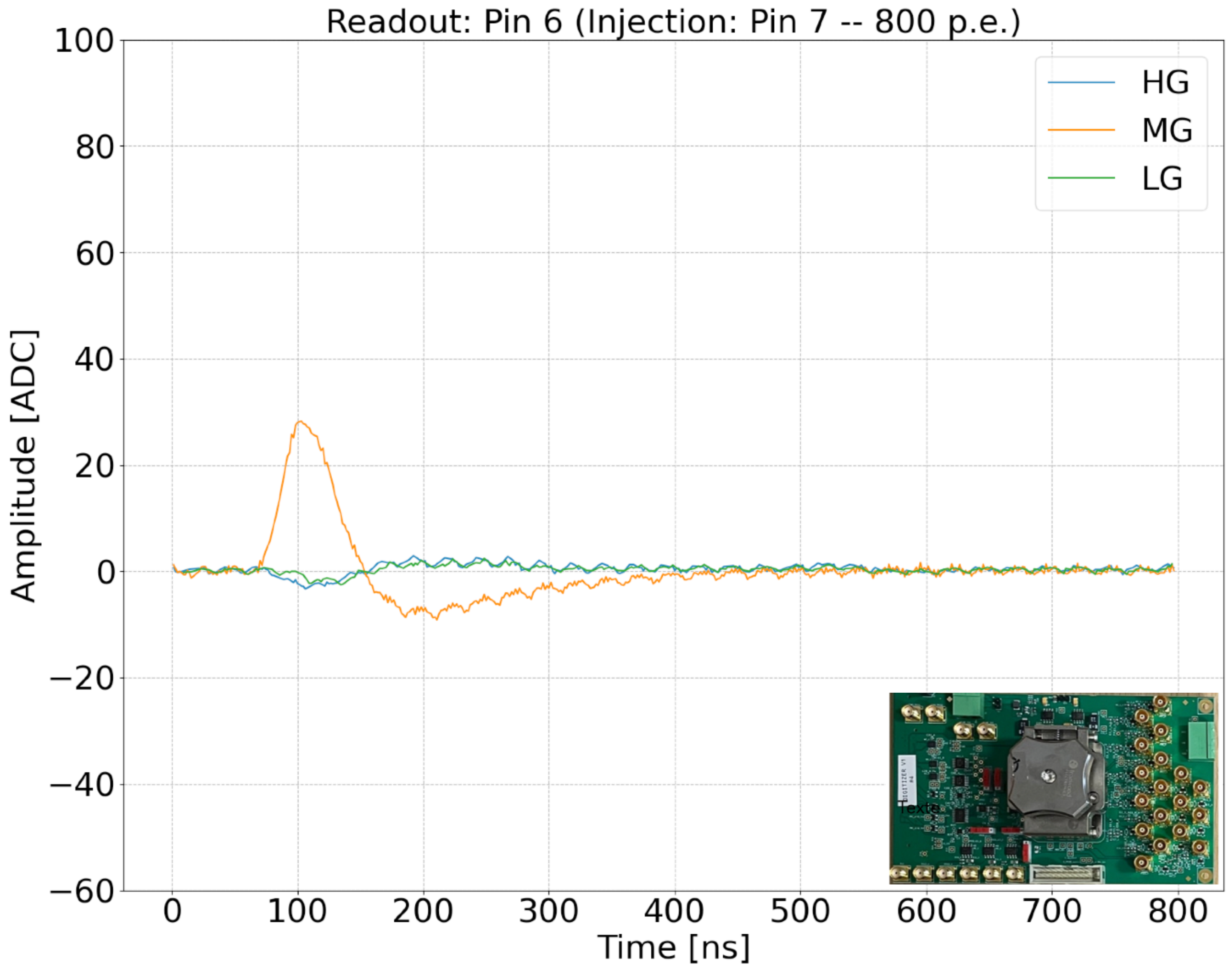


Packaged HKROC with charge reconstruction FPGA

Close cross-talk coupling suppression

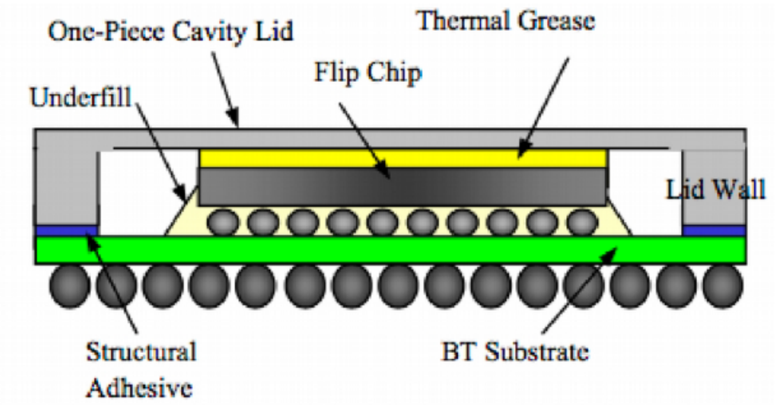
Positive coupling → Importance of the **board stack-up**.





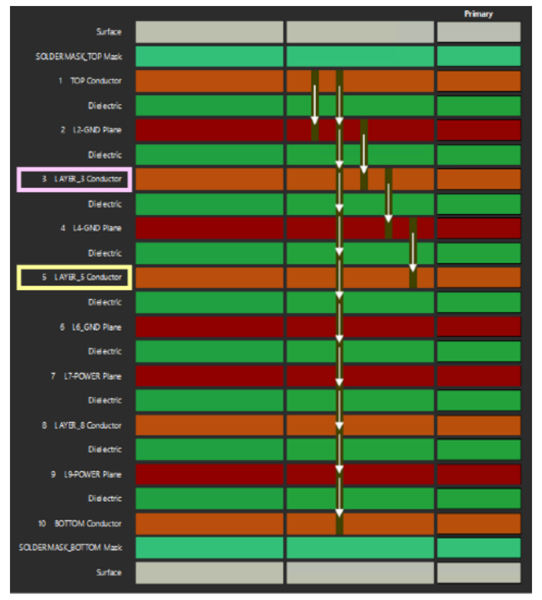
Board v0 - Mezzanine (HKROC1b)

➡1 conductive layer.



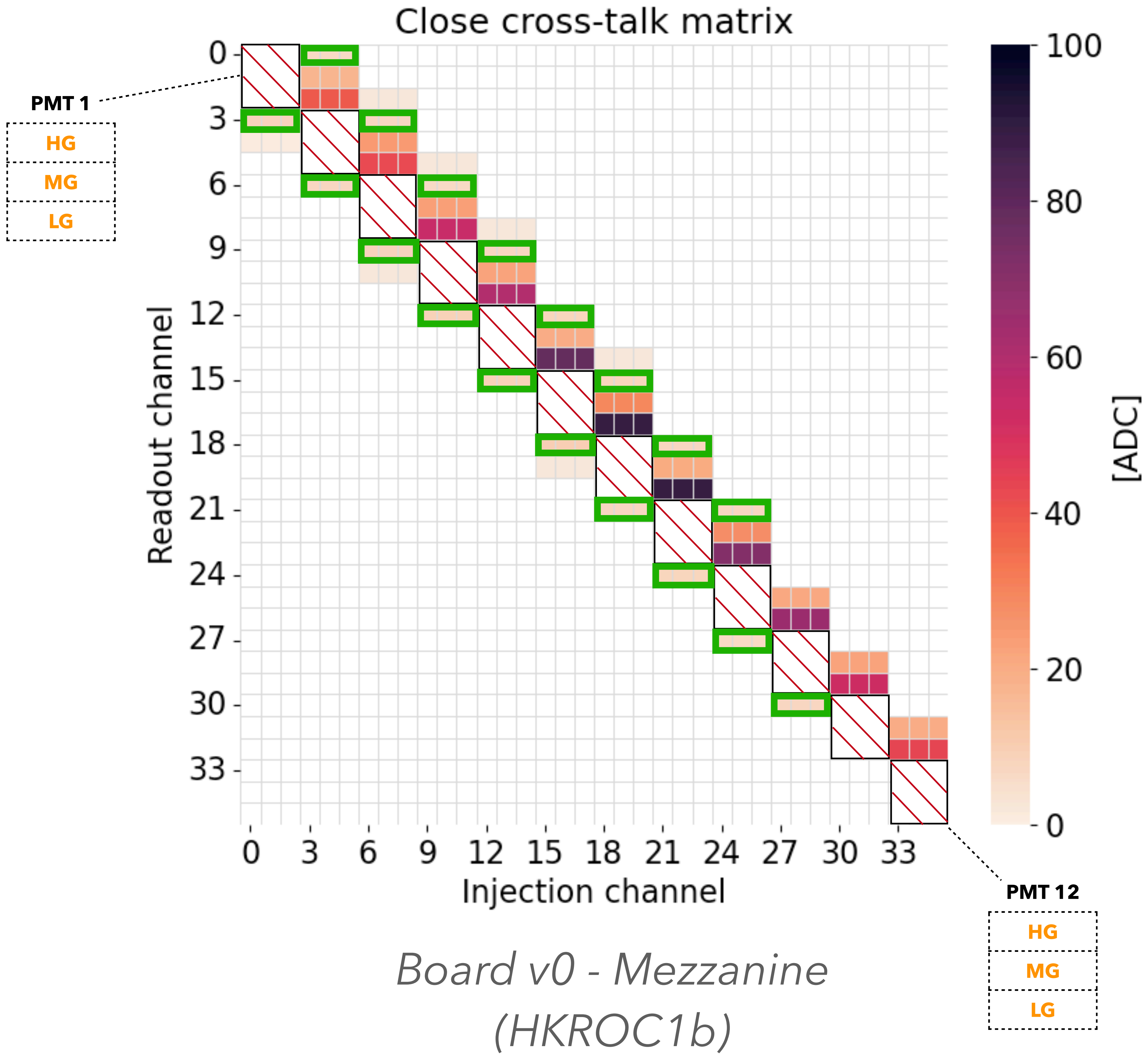
Board v1 - BGA (HKROC1b)

➡2 conductive layers.

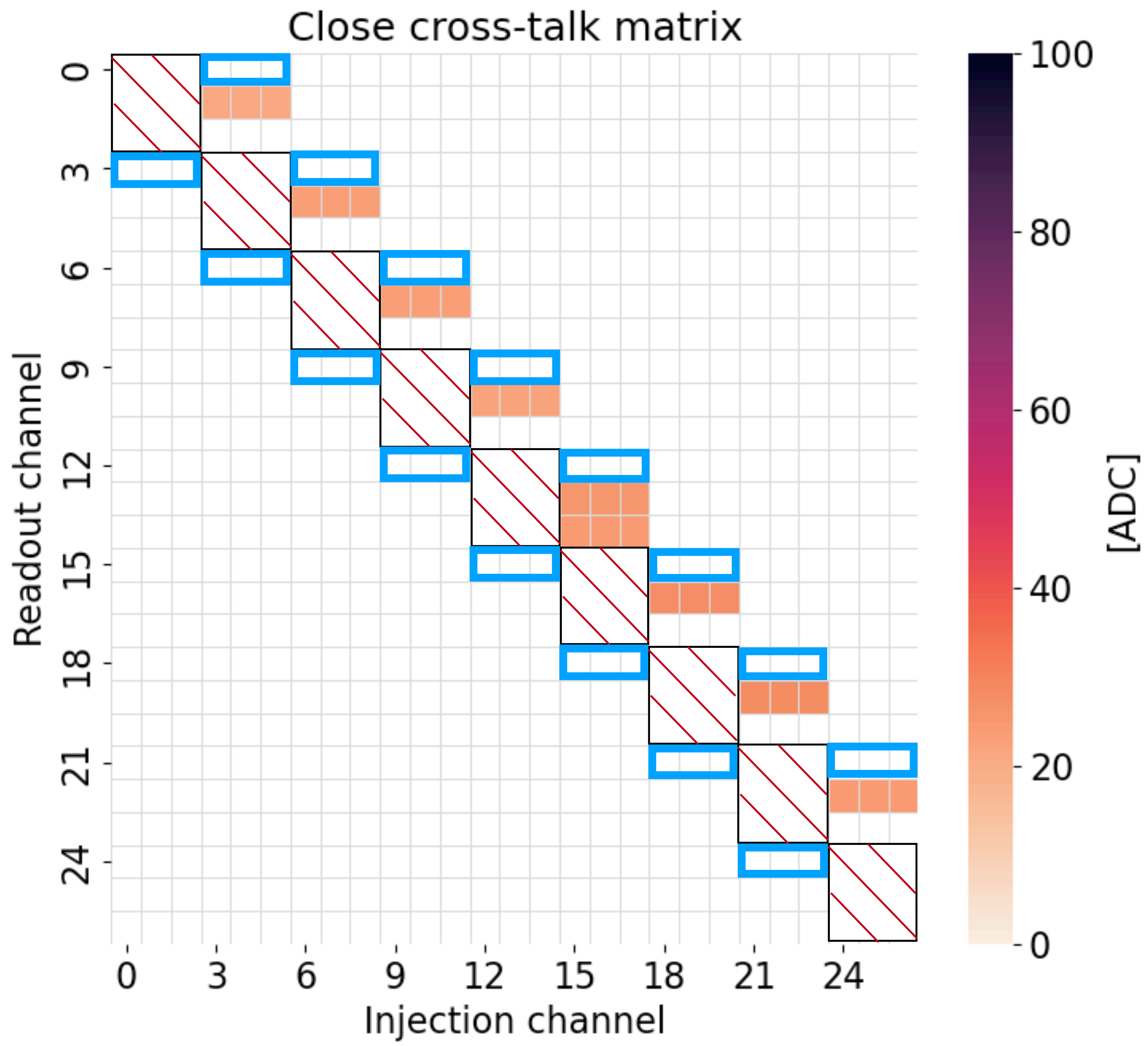


Close cross-talk coupling suppression

HG immunity to coupling → **Fake triggers** due to coupling can be **vetoed by FPGA**.



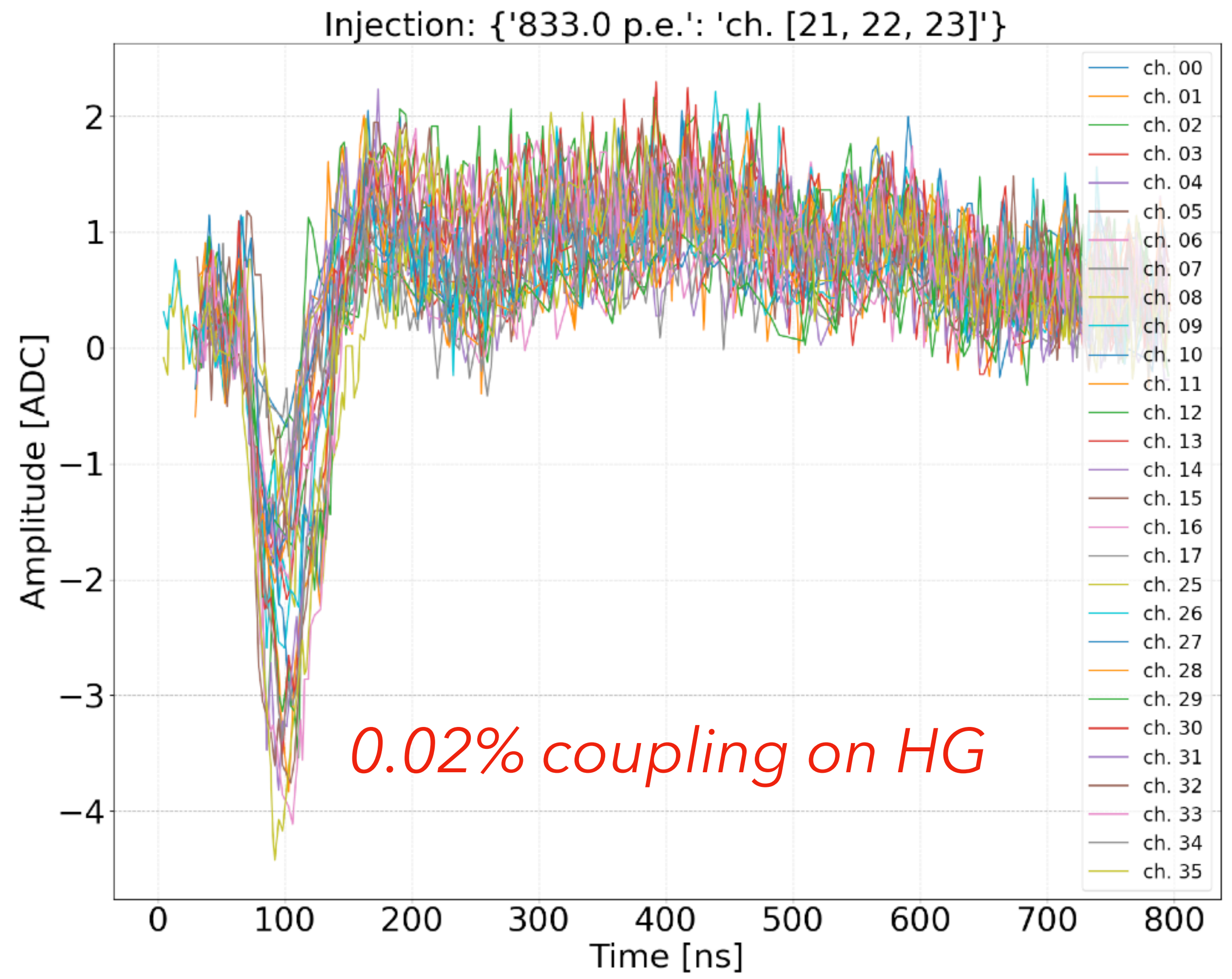
Board v0 - Mezzanine (HKROC1b)



Board v1 - BGA (HKROC1b)

In acquisition board v2 (2024), coupling fully suppressed with splitting into more layers.

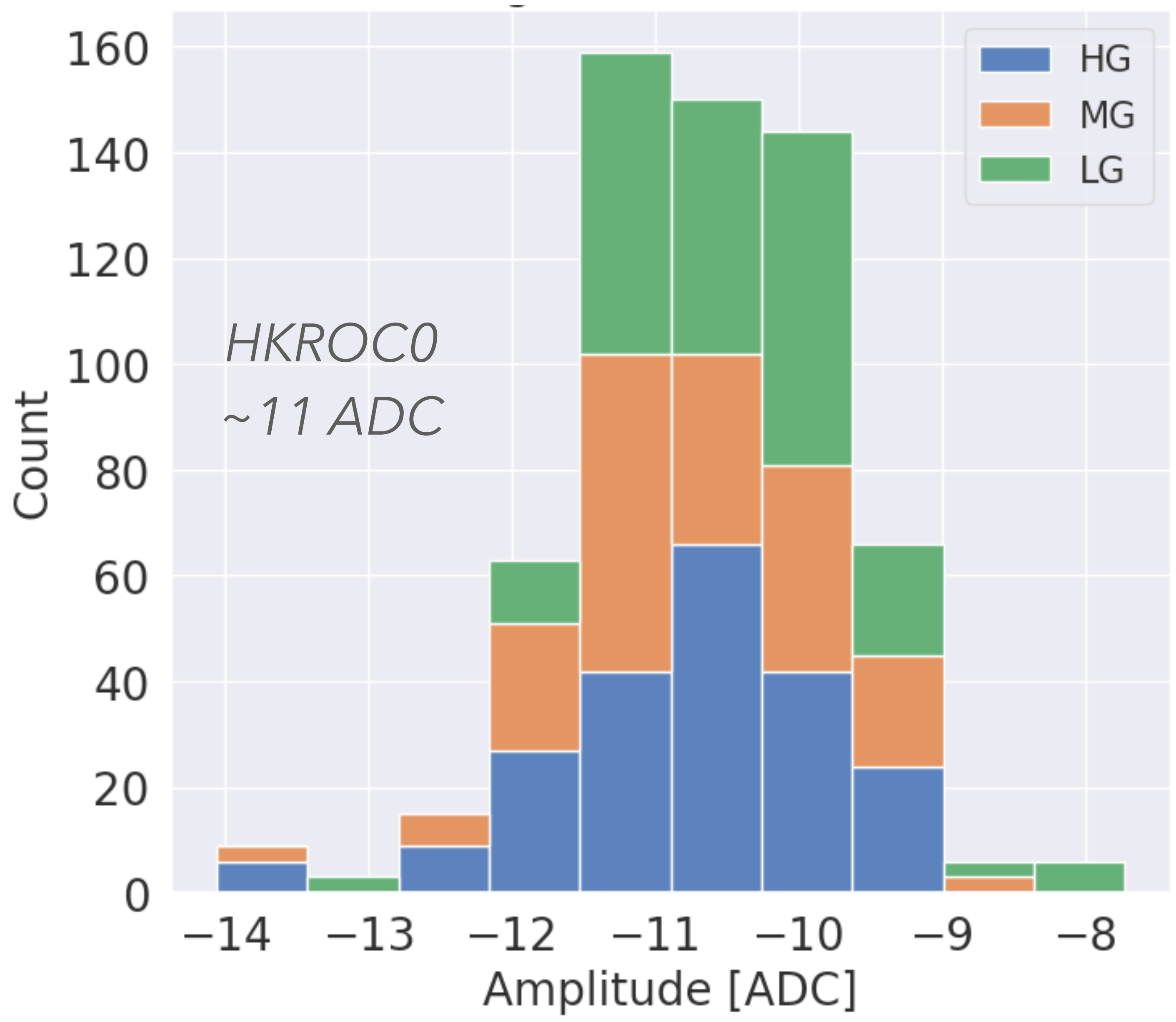
Diffuse cross-talk coupling mitigation



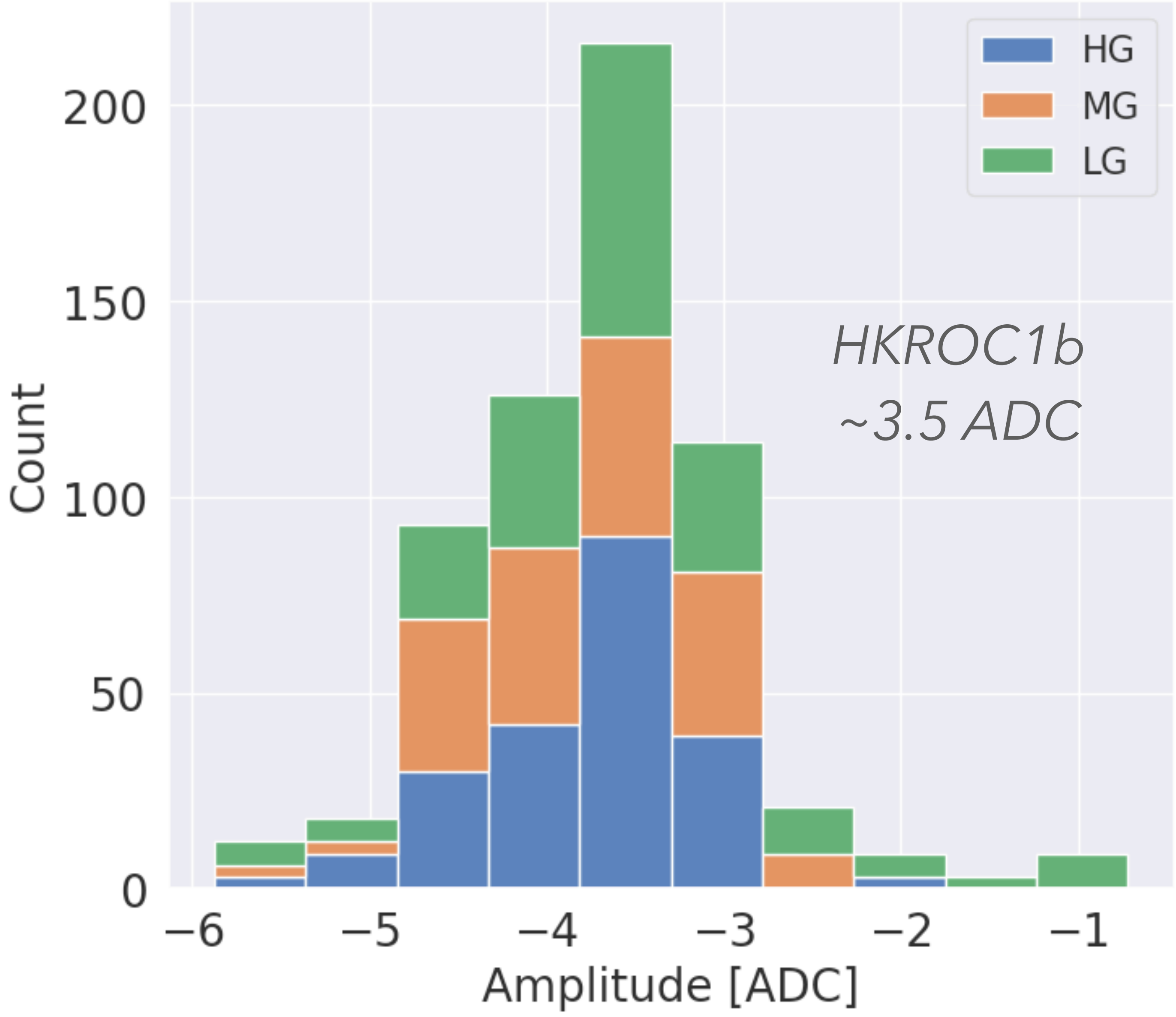
Negative coupling:

- ➡ Comes from the bias, reference voltage shared by all channels.
- ➡ Significant work on the ASIC design (decoupling capacitances) from HKROC0 to HKROC1b.

→ Diffuse cross-talk divided by a factor 3.



Reduction by a factor ~ 3



Charge reconstruction performance not impacted.

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Conclusions

1p.e. ↔ 2pC

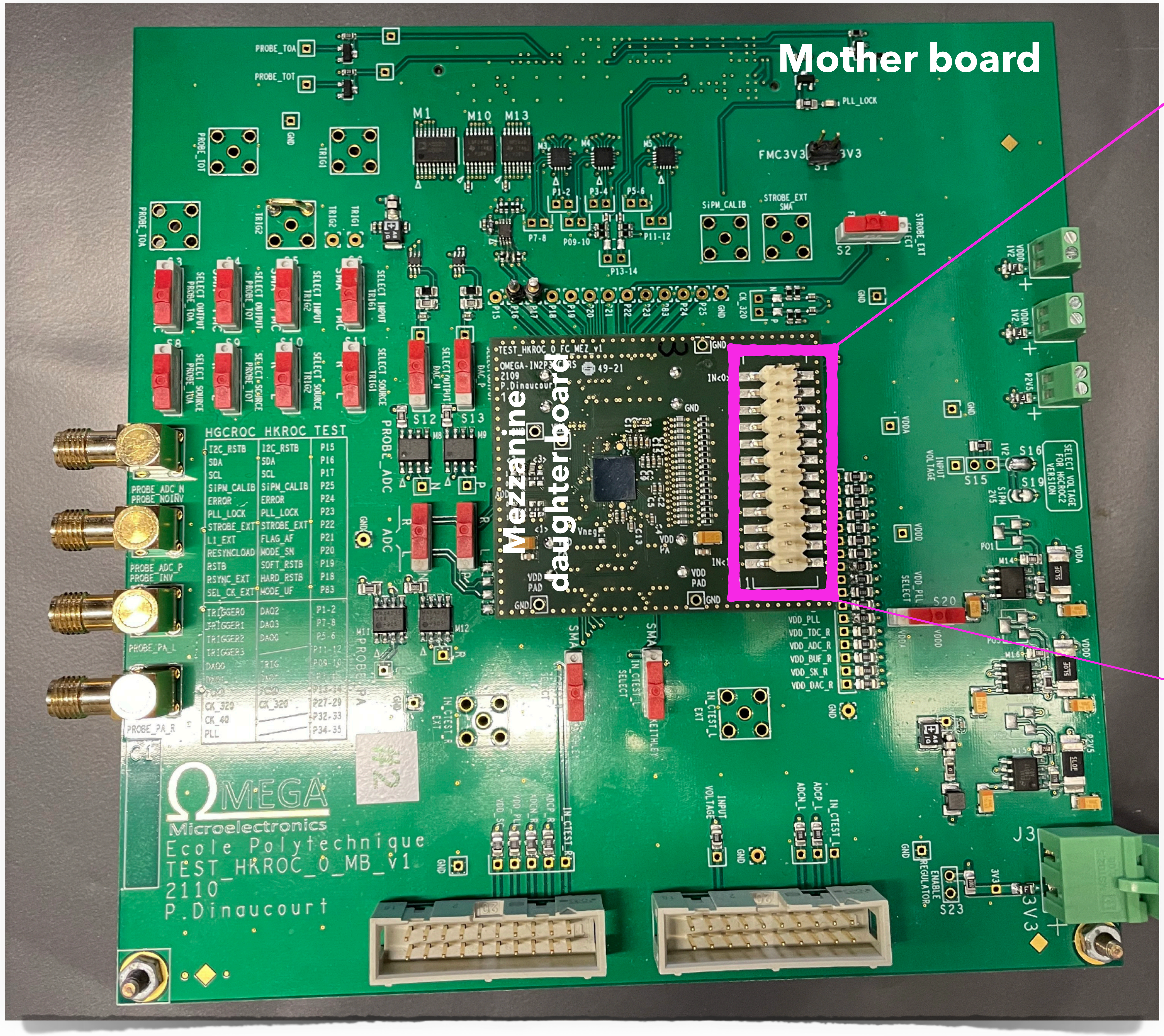
Physics constraints	Electronics requirements	HKROC features
Low power consumption	< 1 W / channel	10 mW / channel
Detect synchronous & asynchronous events	Auto-triggering capabilities	✔
Detect close supernova without event loss	Channel dead time < 1 μs	Dead time ~30ns Hit-rate with 100% efficiency: 950 kHz (SN mode)
Low energy events detection	Detection threshold: 1/6 p.e.	✔
Detection of events from the MeV to the TeV	Dynamic range up to 1250 p.e.	✔
Electronics time resolution < PMT time resolution (1.3 ns)	Time resolution < 300 ps for 1 p.e.	~150 ps for 1 p.e.
Excellent energy reconstruction capability	Charge linearity & resolution ~1%	✔

Paper in progress, based on HKROC v1b performance.

HKROC is an extremely precise & versatile waveform digitizer.
We provide a full HKROC-based ASIC + board to the community, adaptable to large PMT-based experiments.

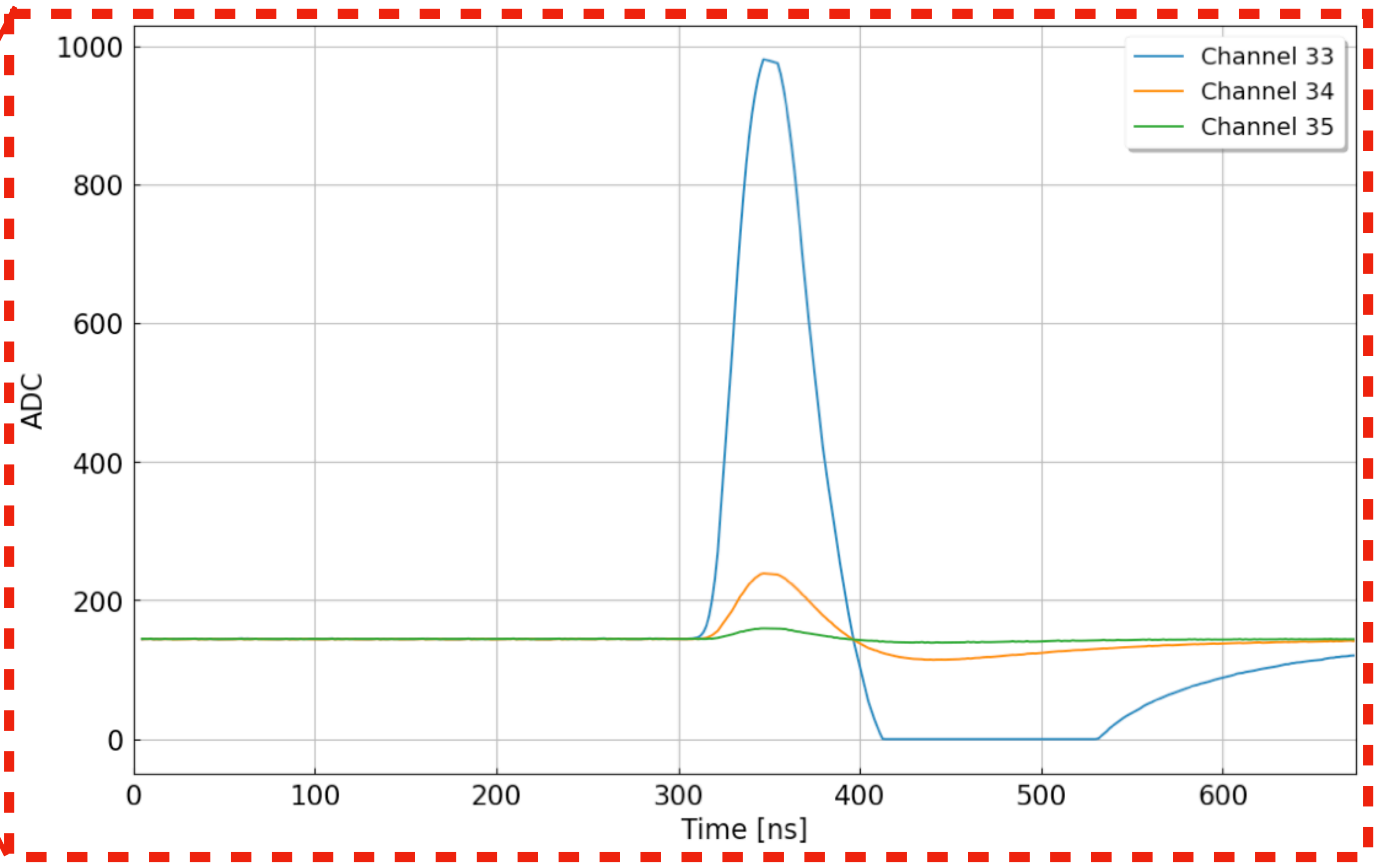
Back-up

HKROC on Mezzanine daughter board



HG - MG - LG

Pin 0 ↔ Ch. 0-1-2
Pin 1 ↔ Ch. 3-4-5
Pin 2 ↔ Ch. 6-7-8
Pin 3 ↔ Ch. 9-10-11
Pin 4 ↔ Ch. 12-13-14
Pin 5 ↔ Ch. 15-16-17
Pin 6 ↔ Ch. 18-19-20
Pin 7 ↔ Ch. 21-22-23
Pin 8 ↔ Ch. 24-25-26
Pin 9 ↔ Ch. 27-28-29
Pin 10 ↔ Ch. 30-31-32
Pin 11 ↔ Ch. 33-34-35



Hyper Kamiokande PMTs

PMT Properties	Super-K	Hyper-K
Dynode structure	Venetian blind	Box & Line
Quantum Efficiency (at 390 nm)	$\approx 22\%$	$\approx 30\%$
Collection Efficiency (at 10^7 gain)	$\approx 73\%$	$\approx 95\%$
Hit Efficiency (at 1/4 p.e. threshold)	$\approx 72\%$	$\approx 86\%$
Detection Efficiency (QE $\times$ CE $\times$ HE)	$\approx 12\%$ $\xrightarrow{\times \approx 2.1}$	$\approx 25\%$
Time resolution (TTS for 1 p.e.)	≈ 6.7 ns ($\sigma \approx 3.4$ ns)	≈ 2.6 ns ($\sigma \approx 1.3$ ns)
Charge resolution	$\approx 60\%$	$\approx 31\%$
Dark rate	≈ 4 kHz	≈ 4 kHz

Hamamatsu R12860-HQE

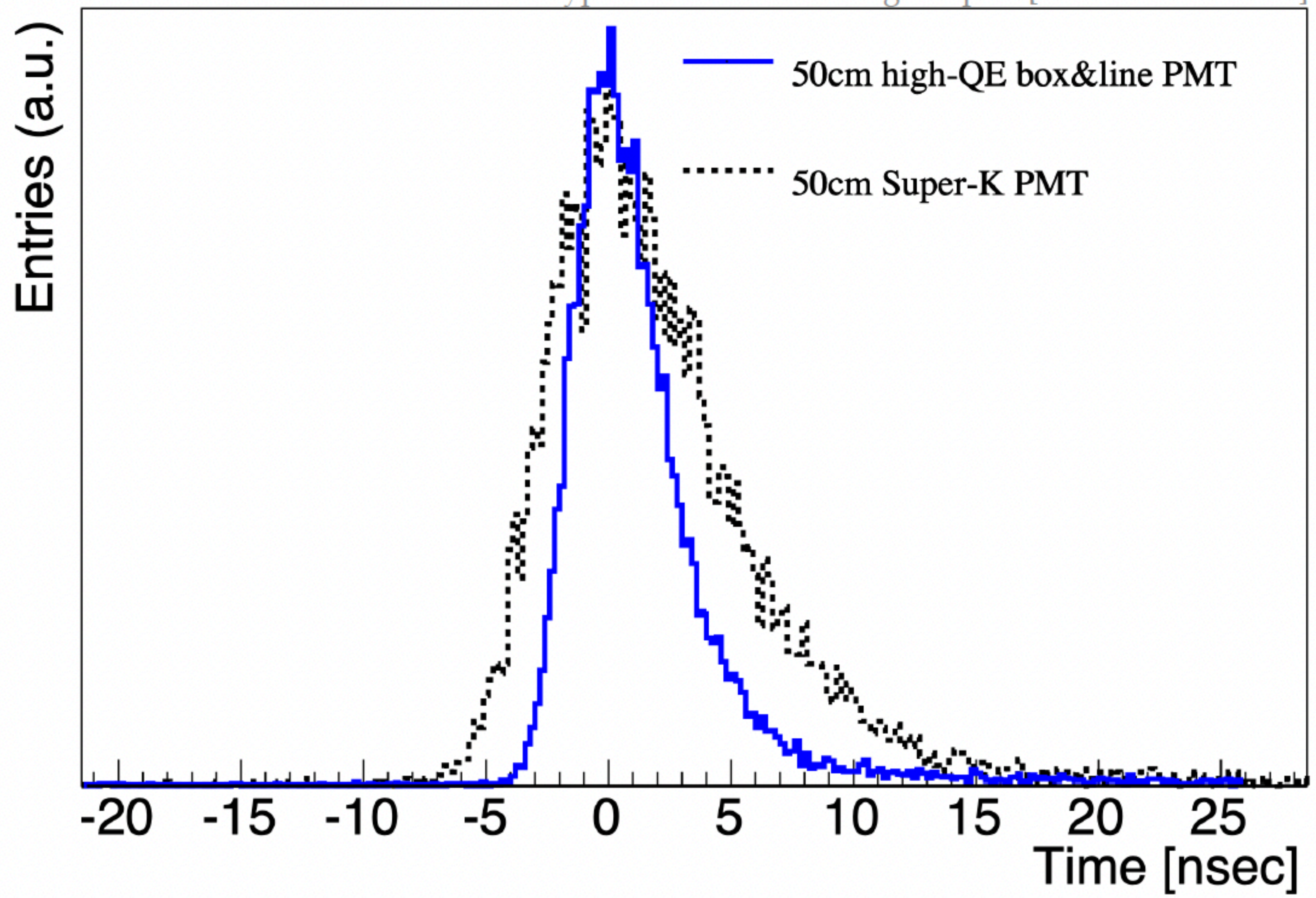
Better vertex reconstruction

Better energy reconstruction

Hyper Kamiokande PMTs

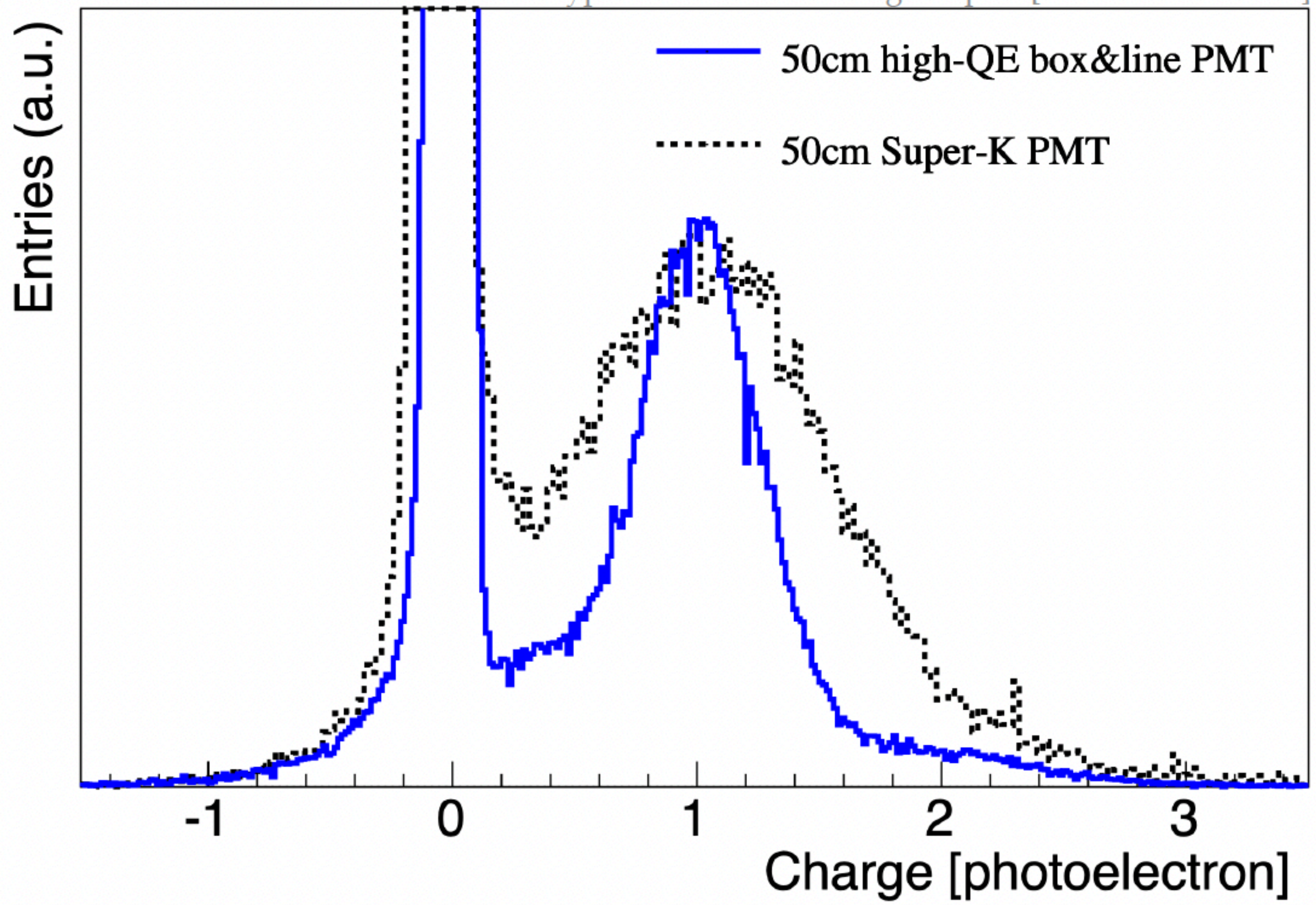
Time resolution
(TTS for 1 p.e.)
≈ 6.7 ns (σ ≈ 3.4 ns) → ≈ 2.6 ns (σ ≈ 1.3 ns)

Hyper-Kamiokande Design Report [*arXiv:1805.04163v2*]

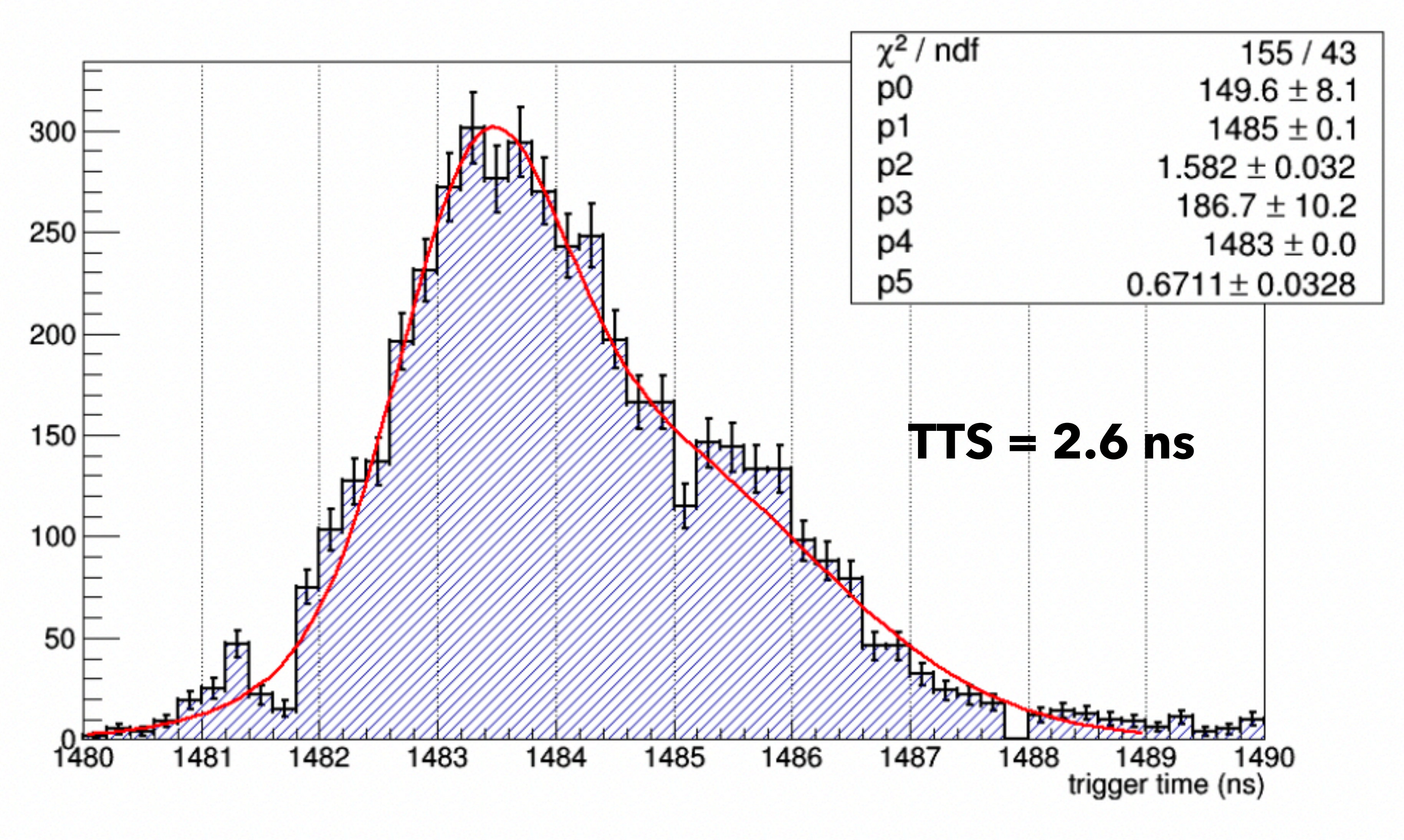


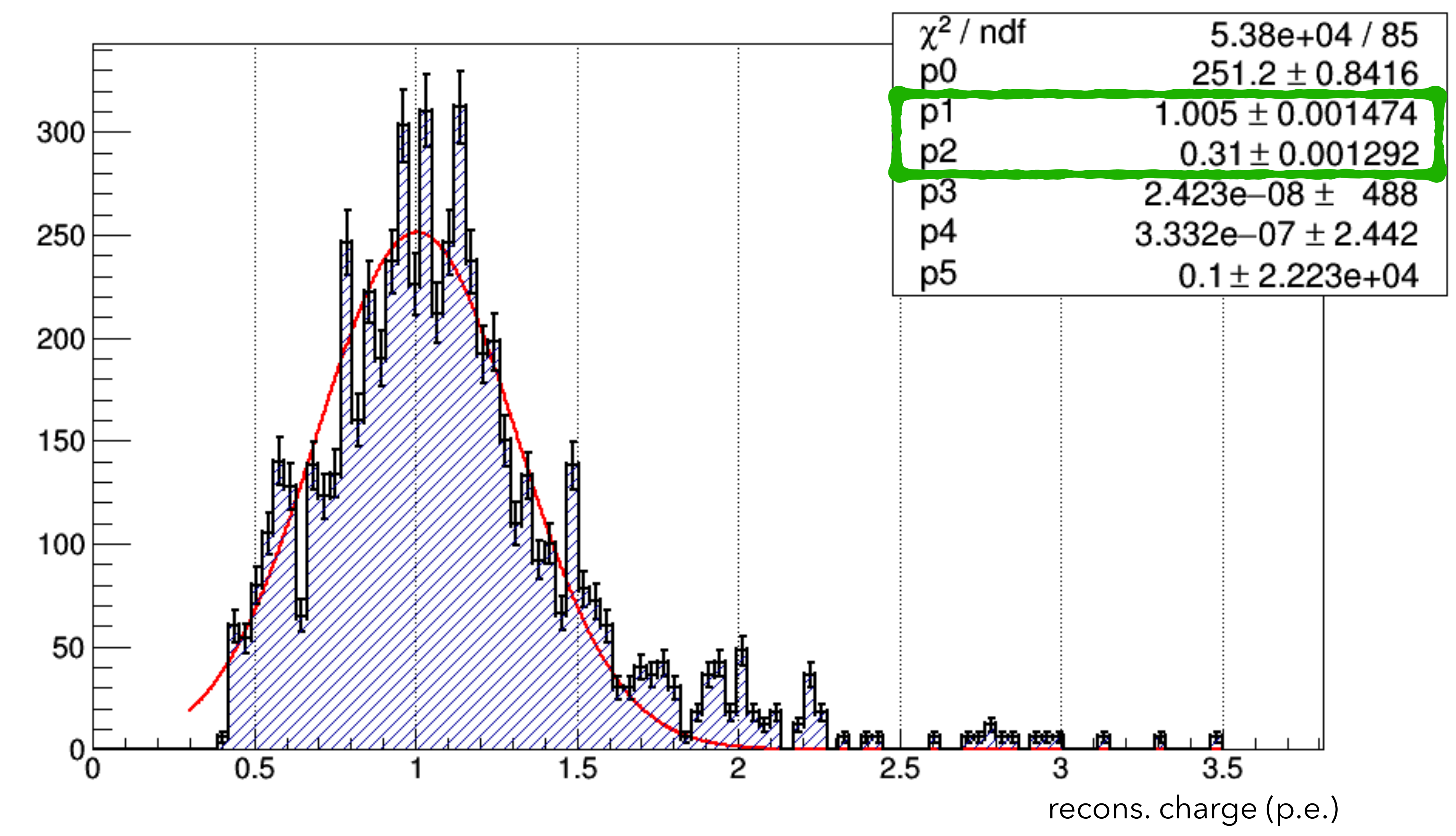
Charge resolution
≈ 60% → ≈ 31%

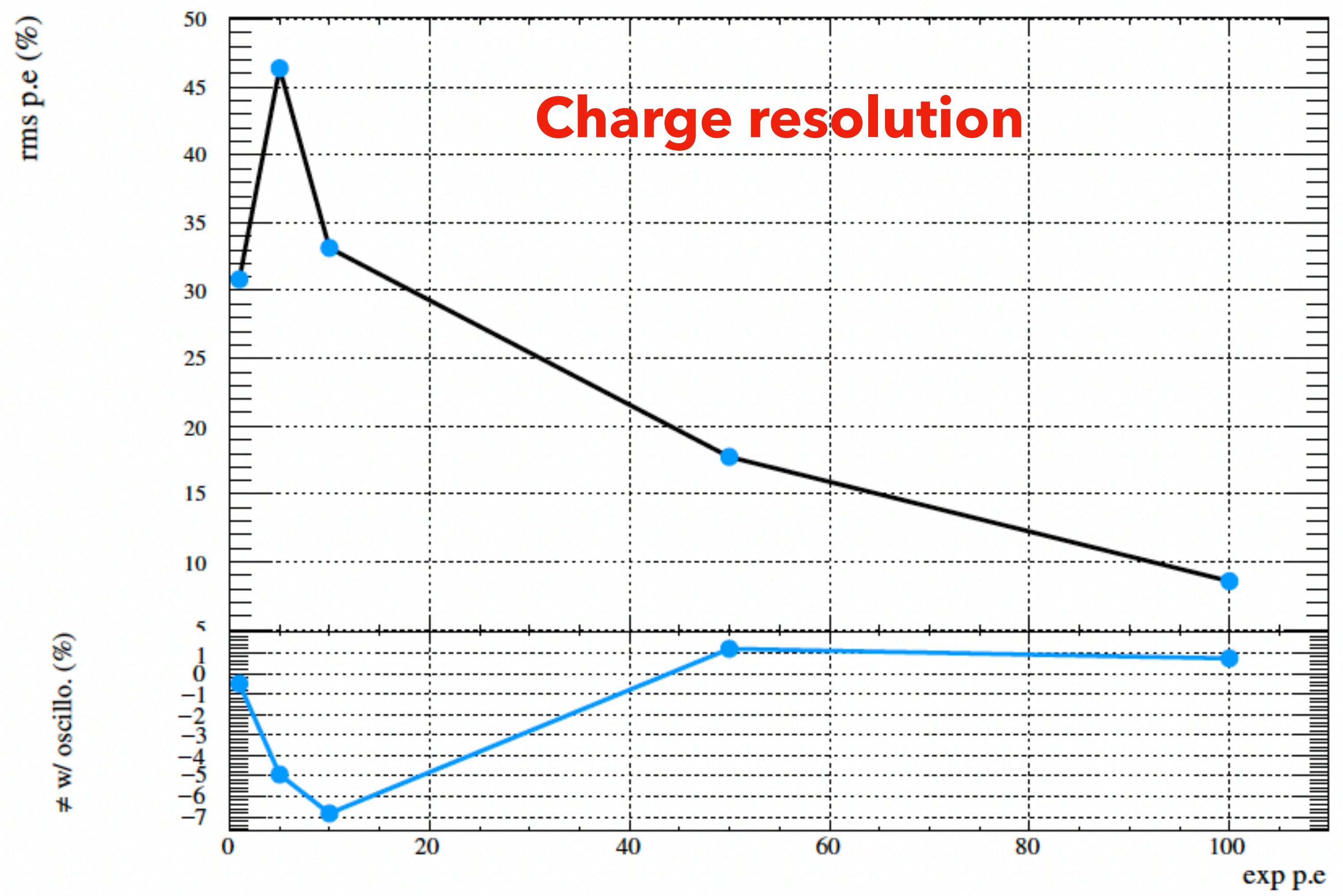
Hyper-Kamiokande Design Report [*arXiv:1805.04163v2*]

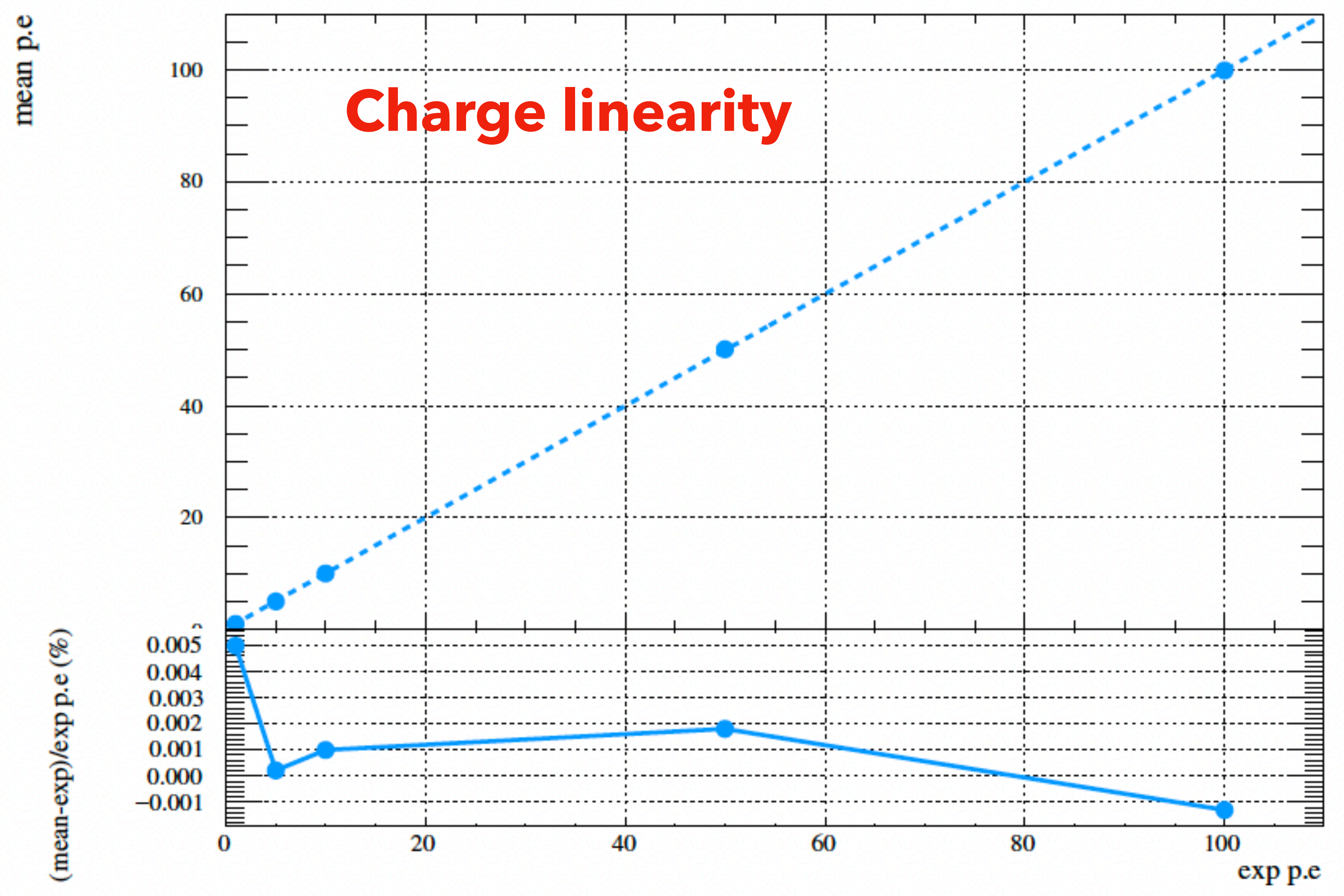


HKROC performance using PMT

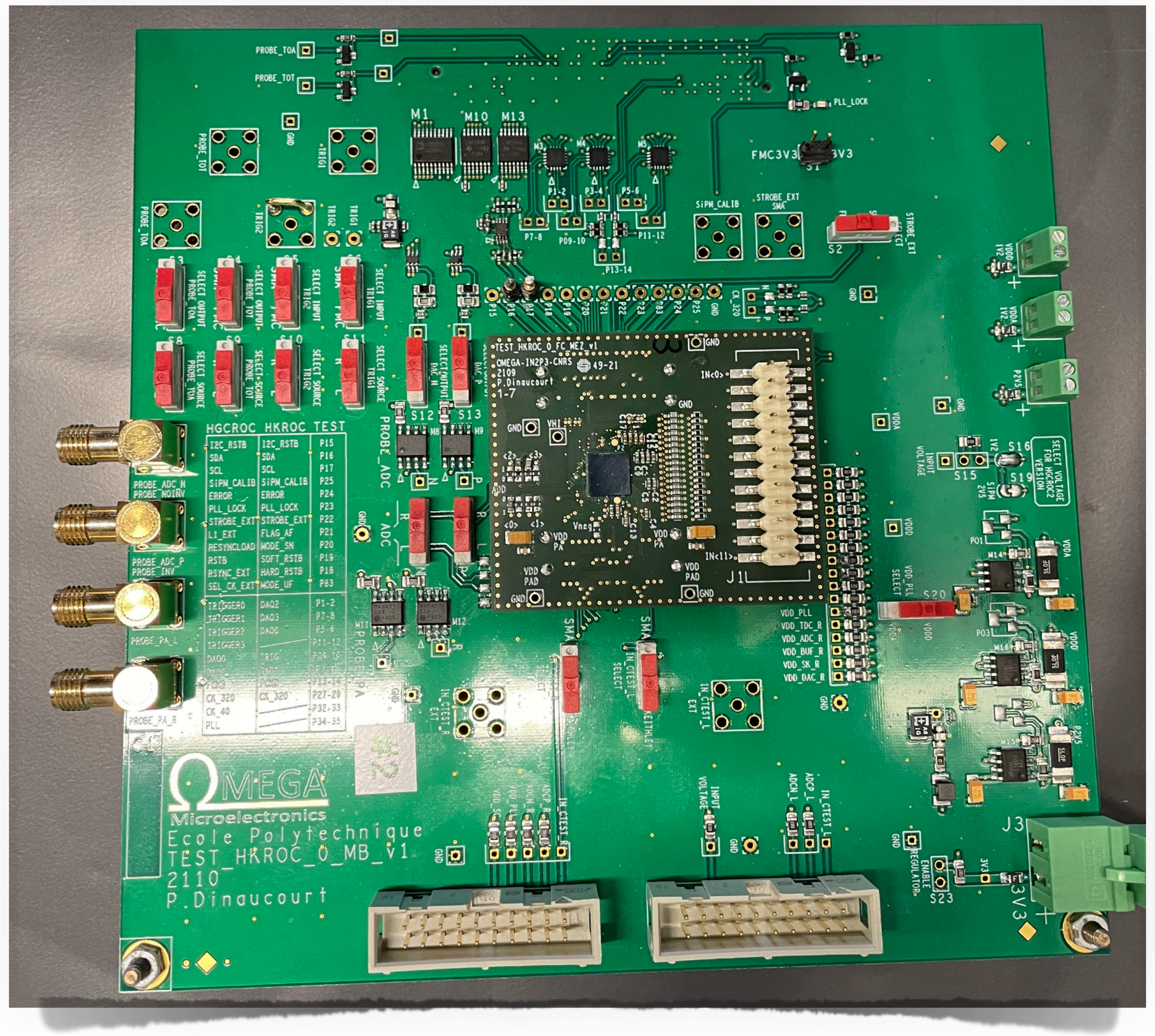




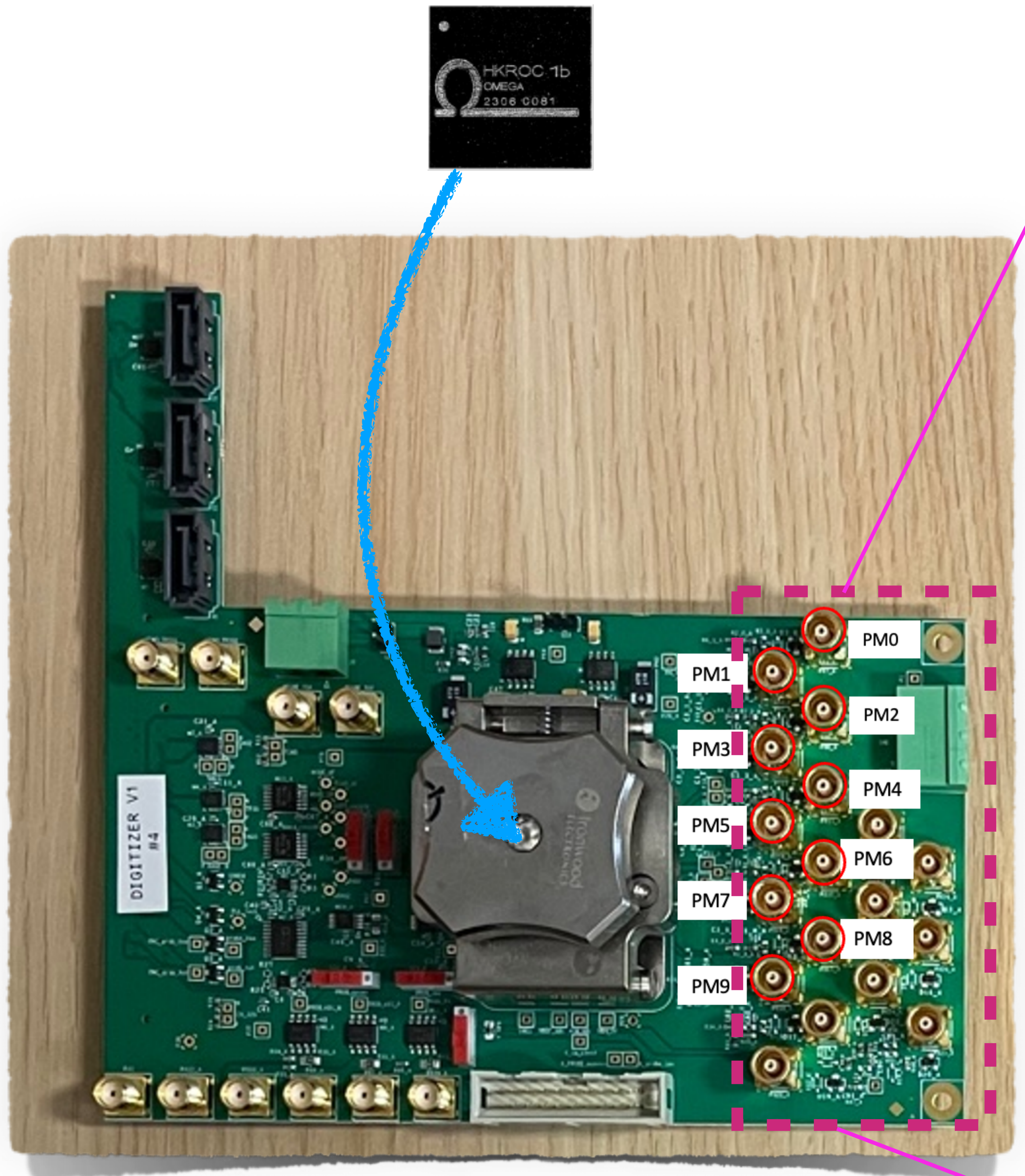


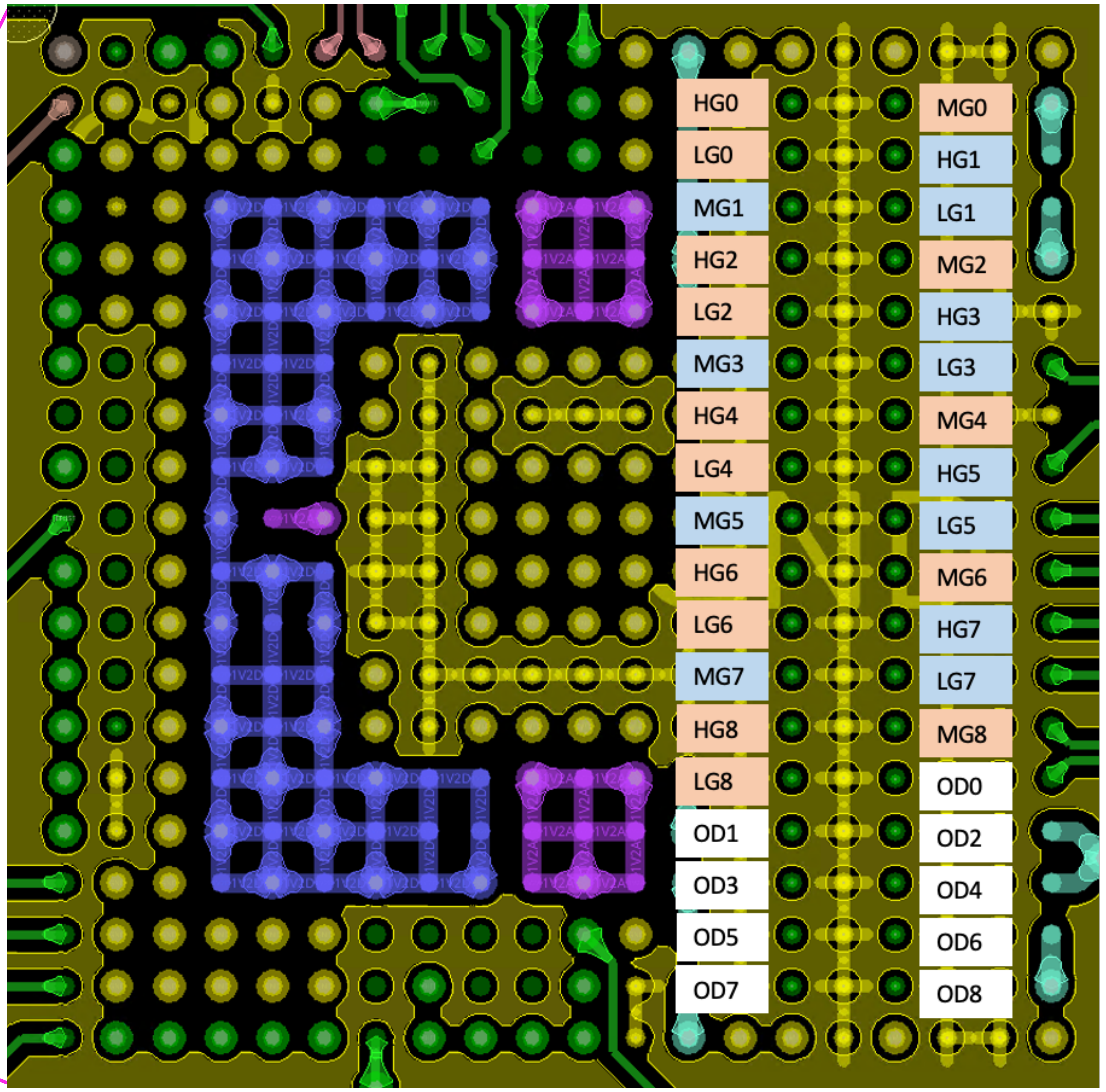


From single-layer to multi-layer front-end board



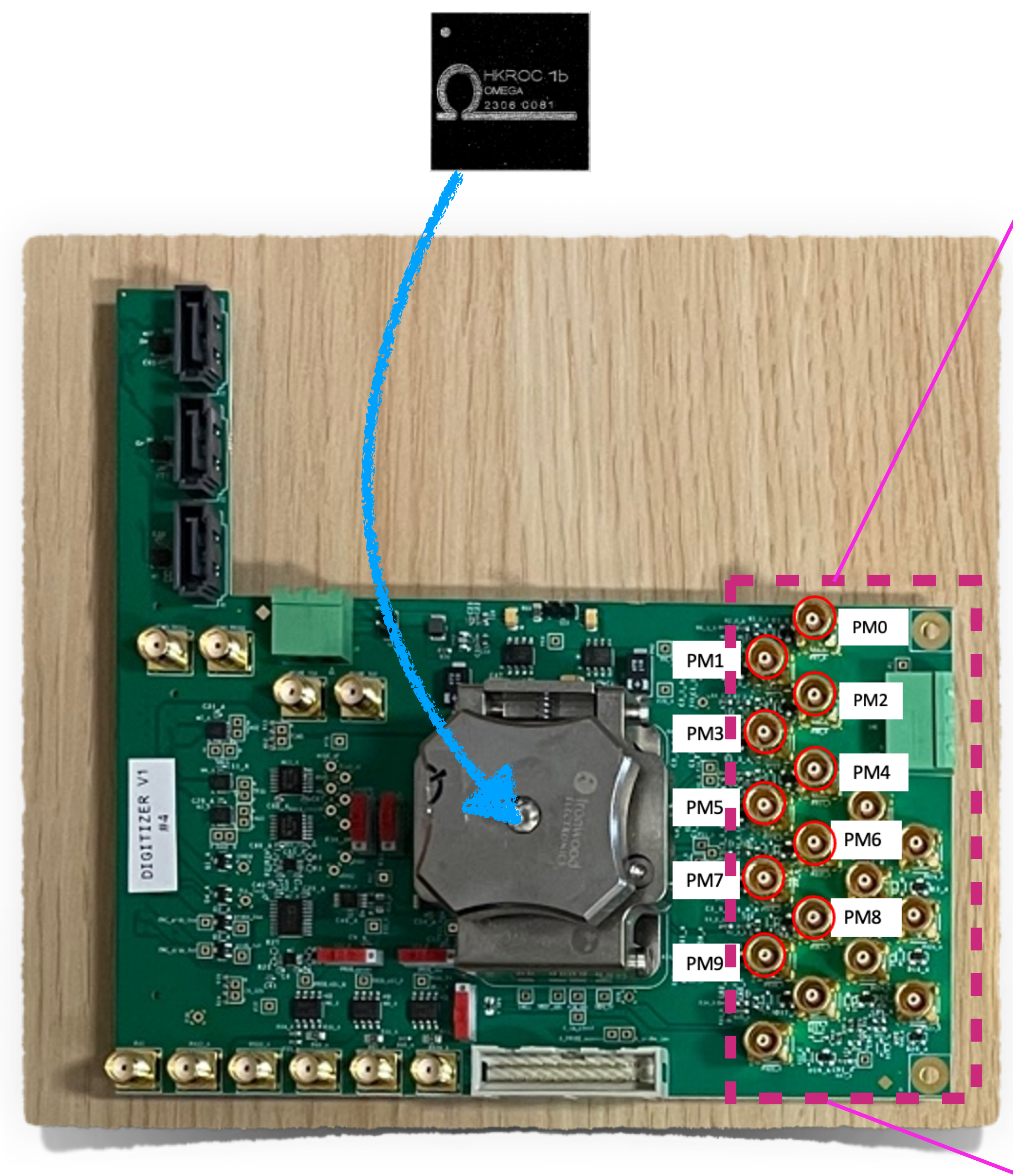
Mezzanine daughter board on mother board

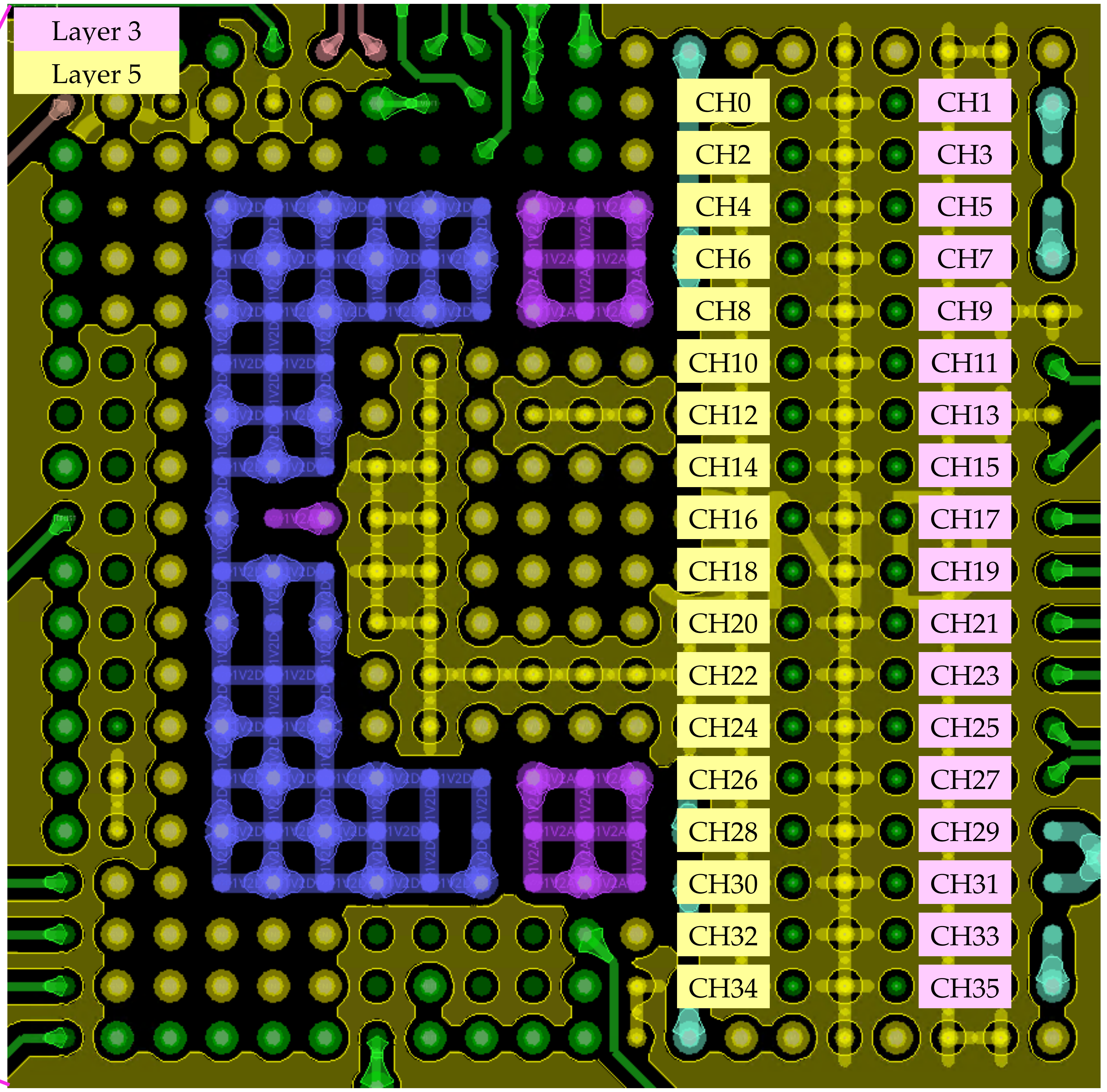


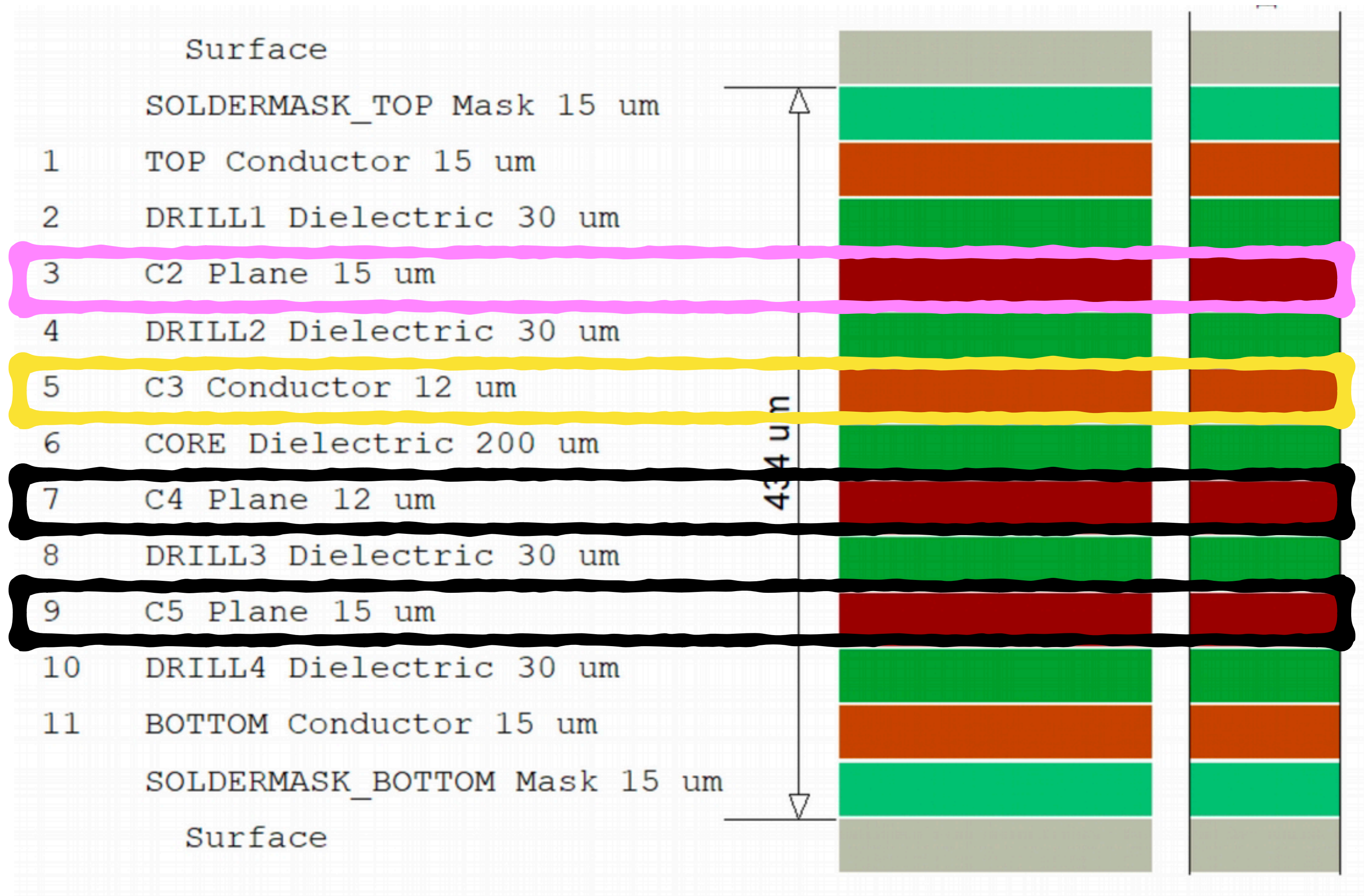


BGA on mother board

From single-layer to multi-layer front-end board

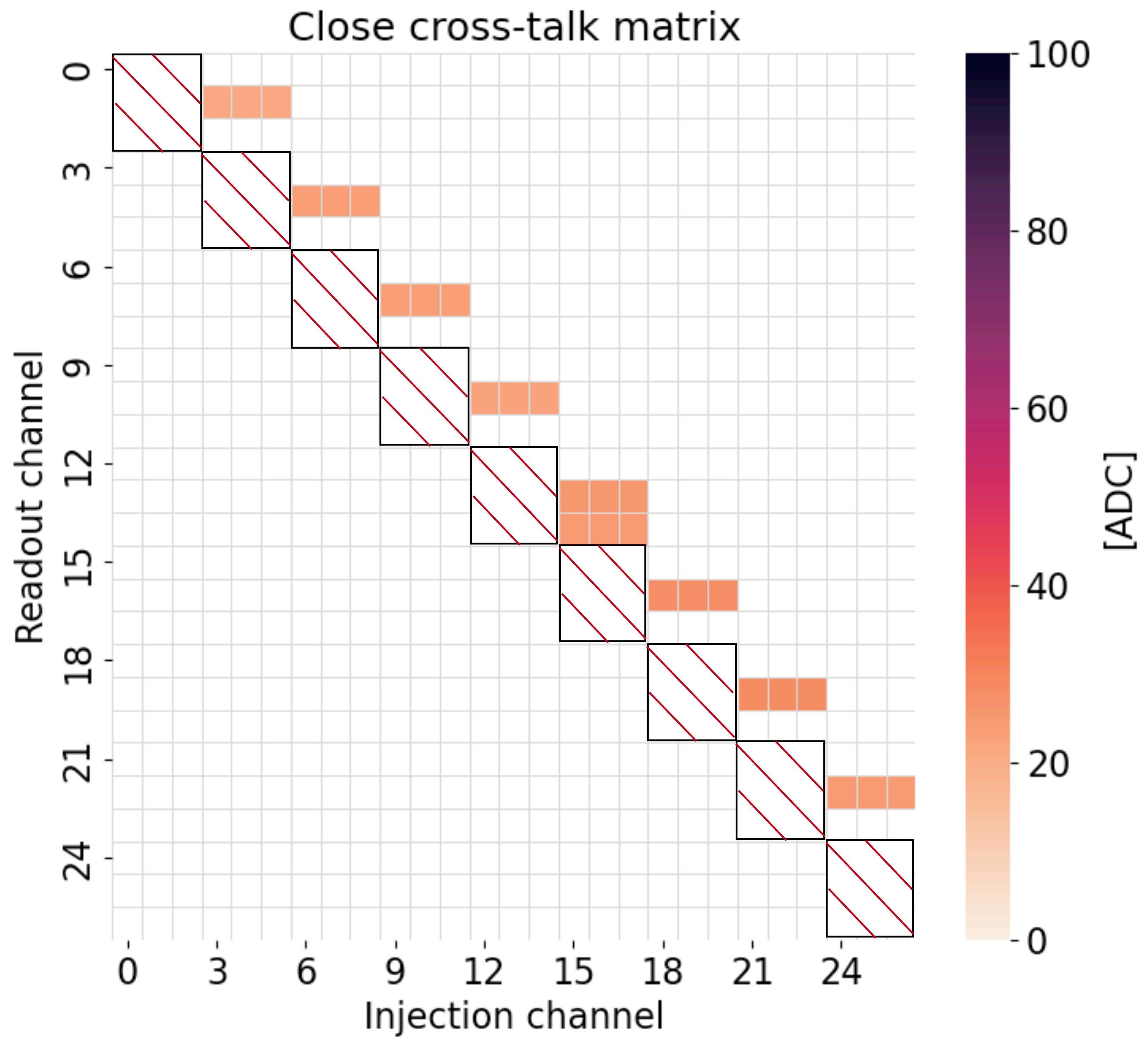


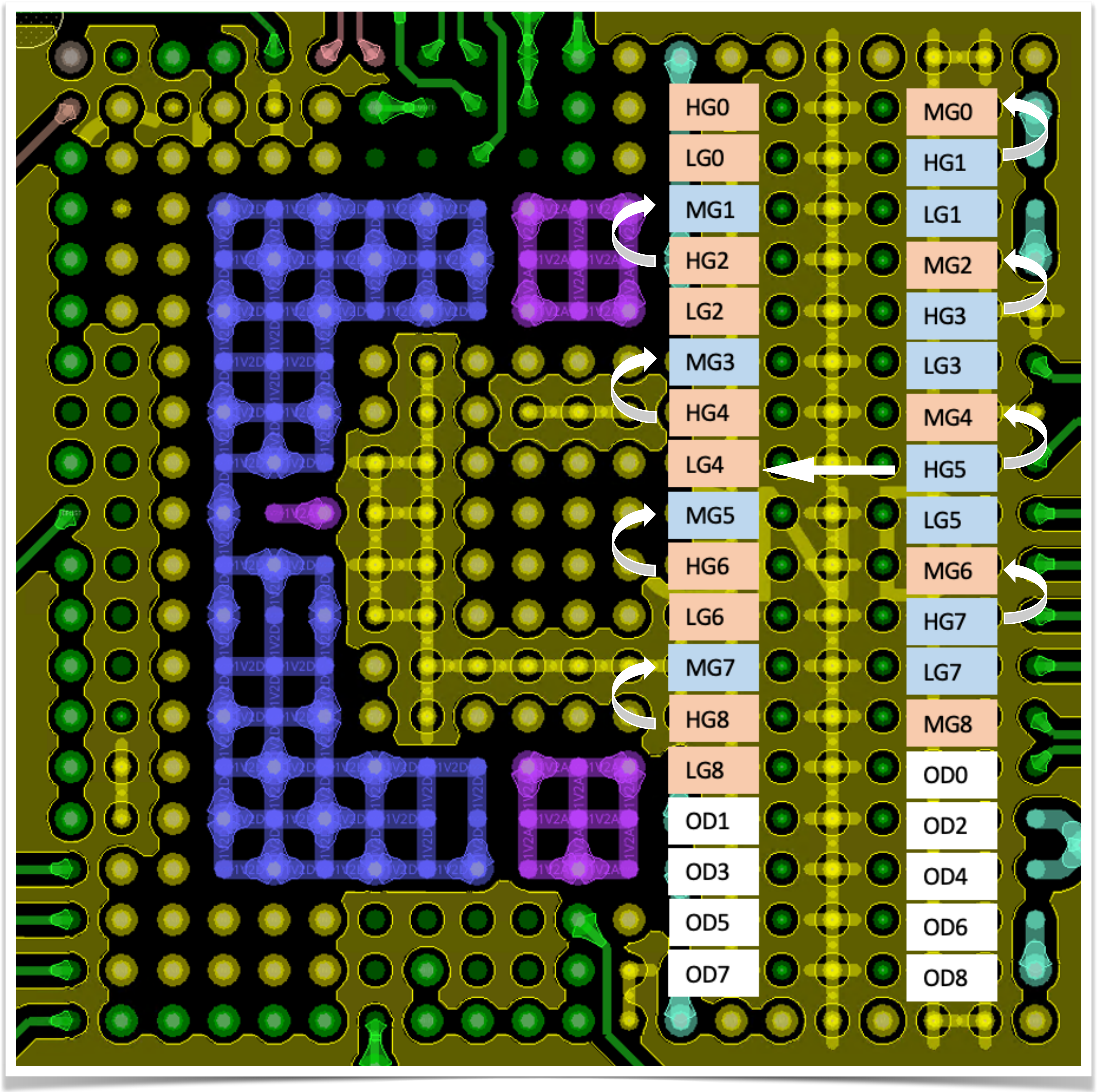




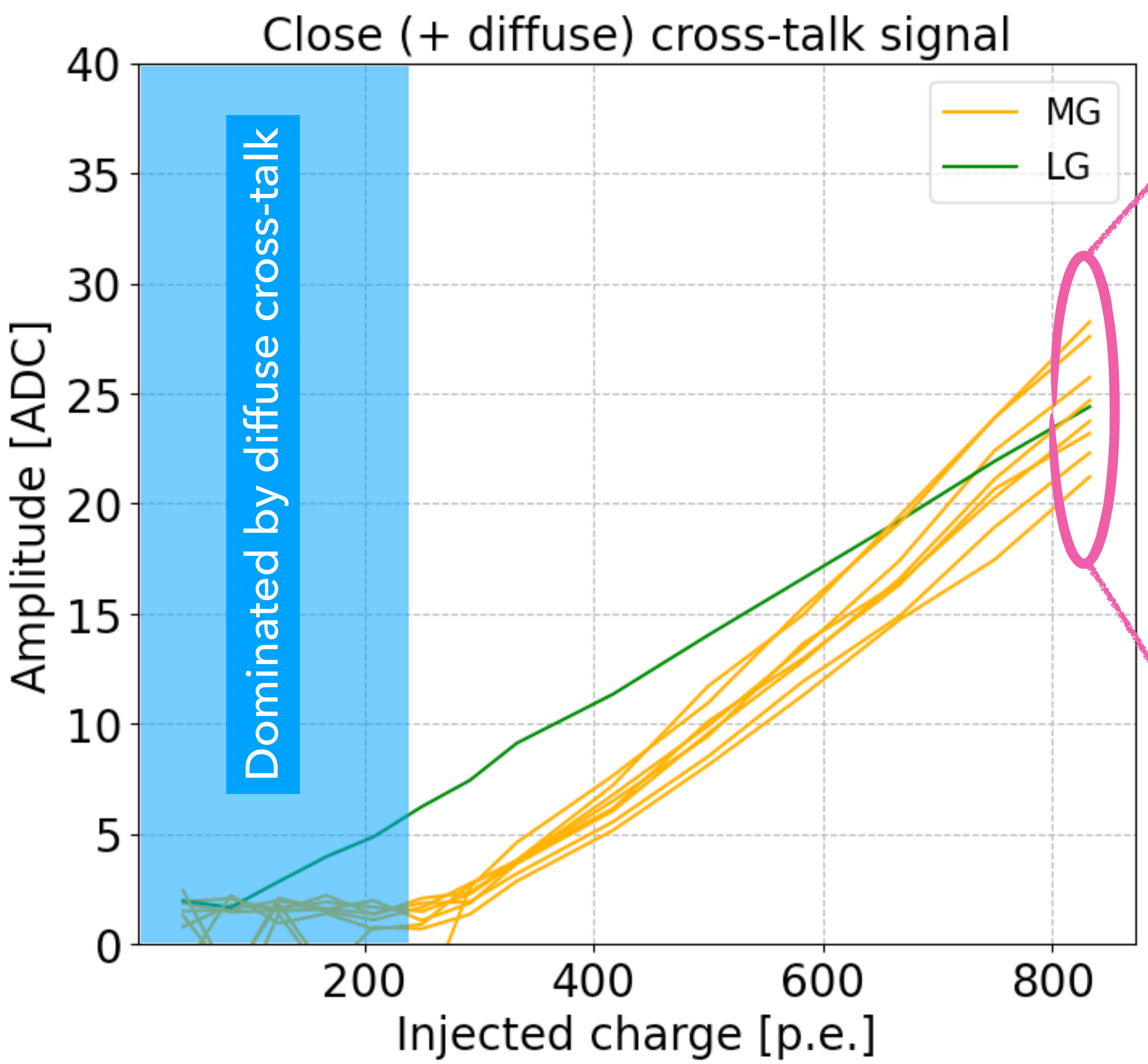
BGA on mother board

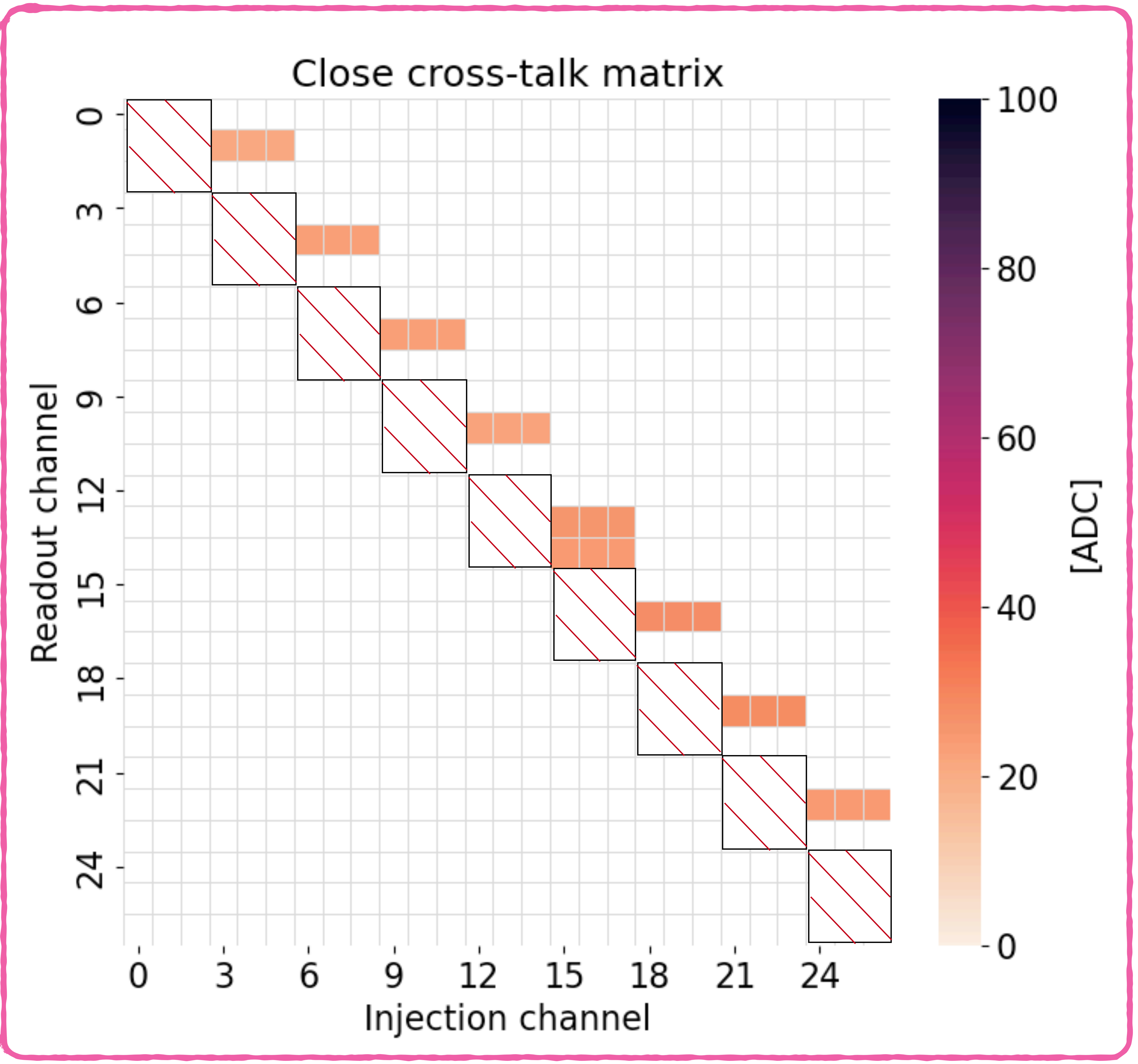
Close Crosstalk Matrix - HKROC v1b + BGA



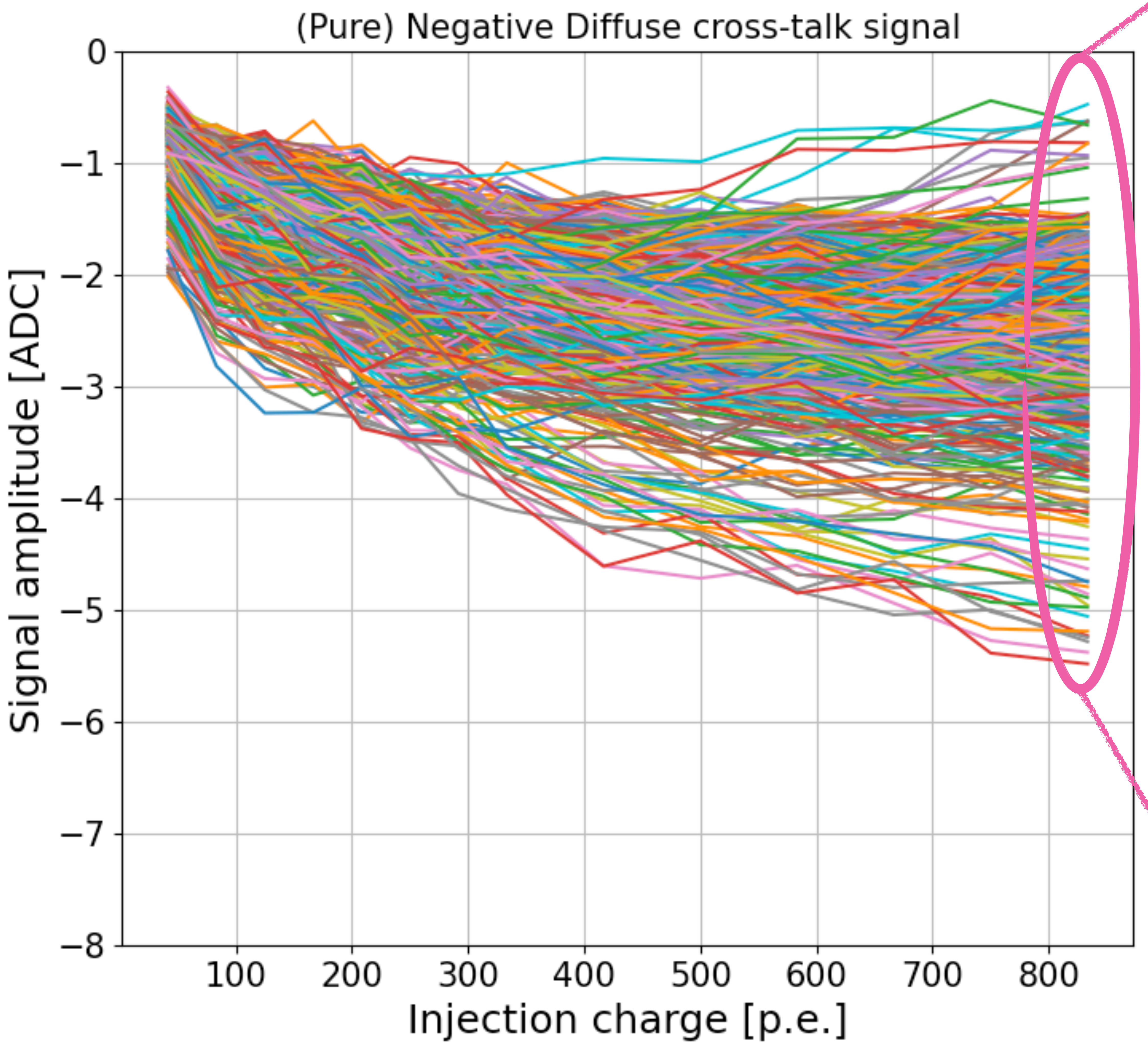


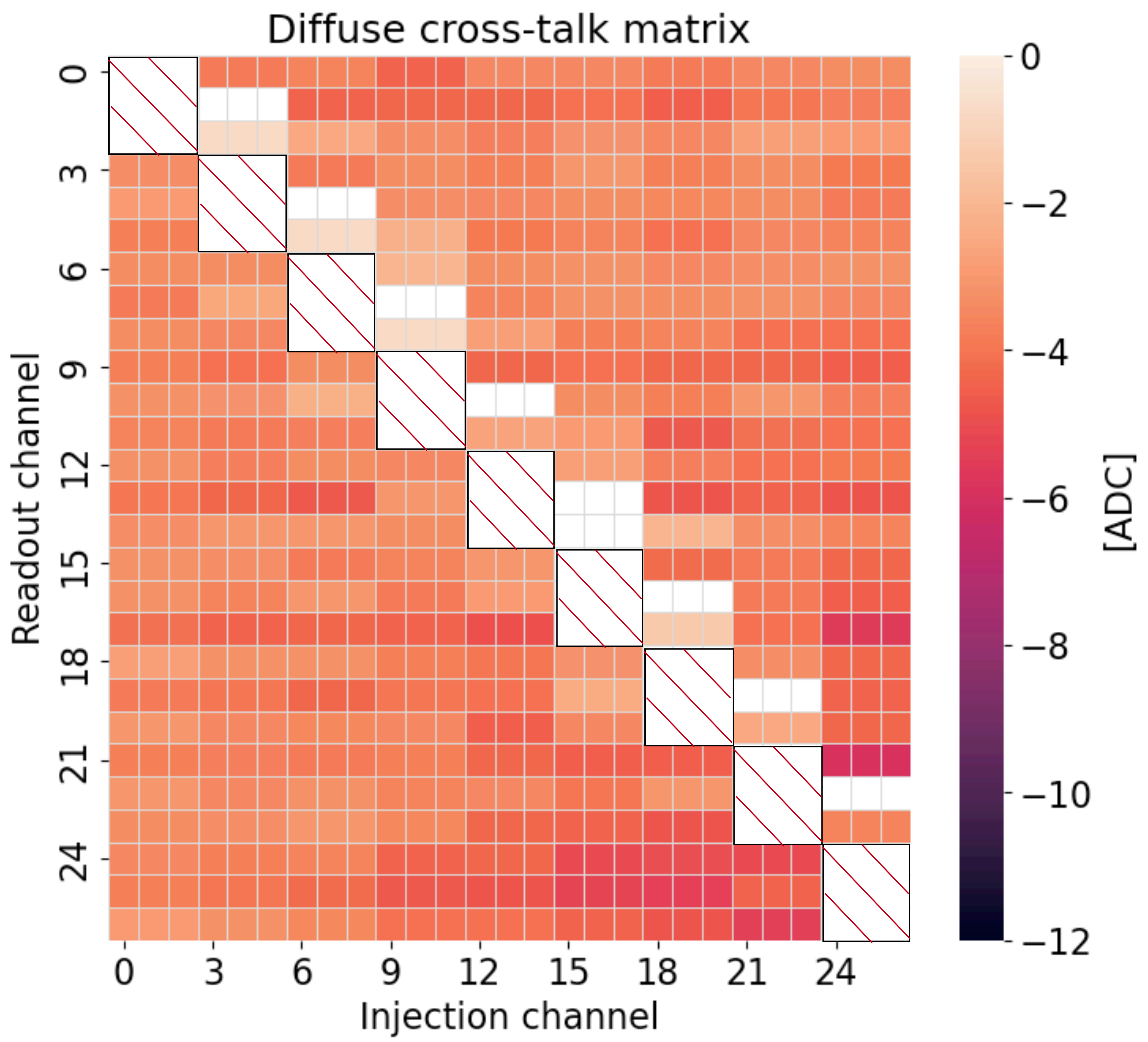
Linearity measurements - Close cross-talk



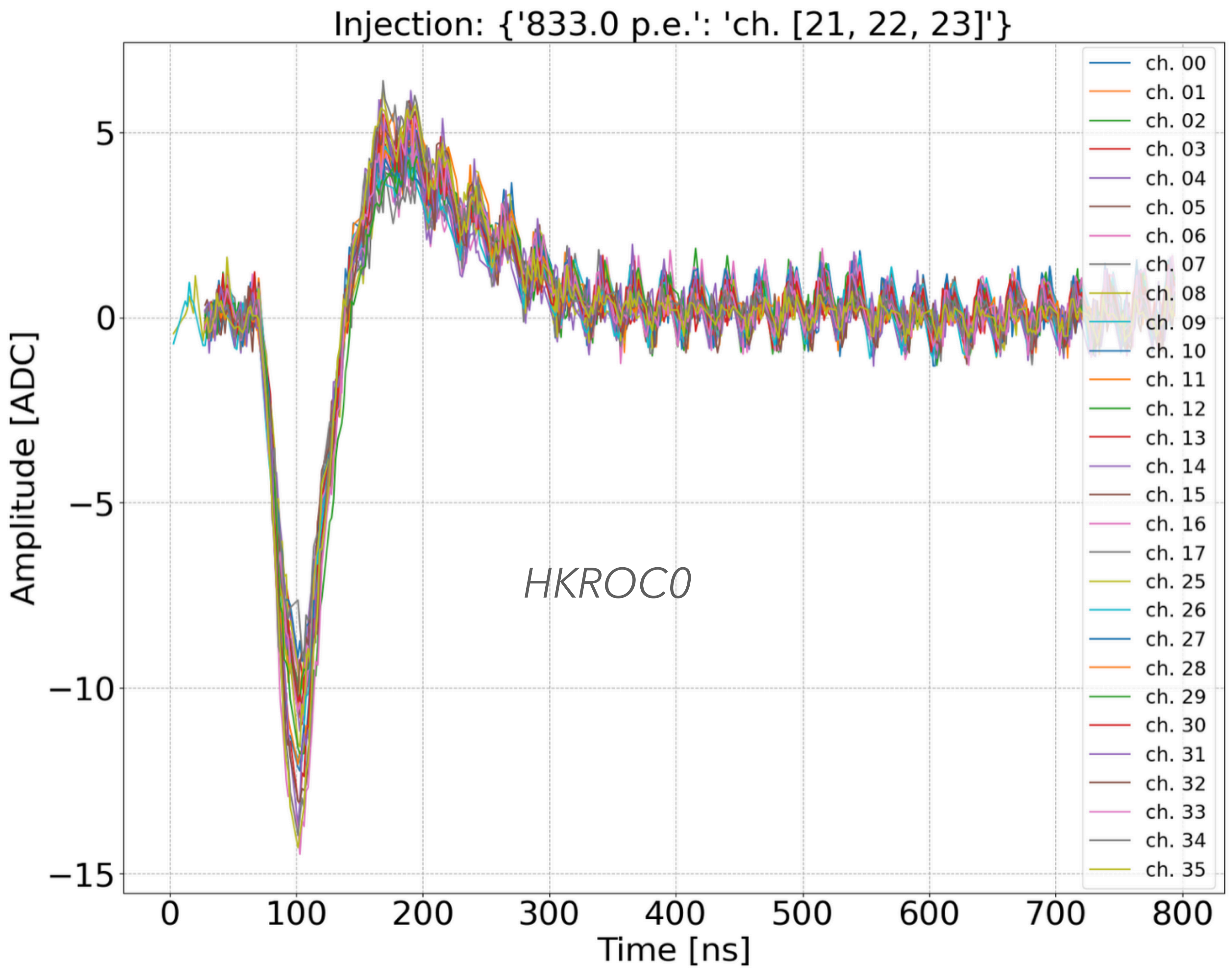


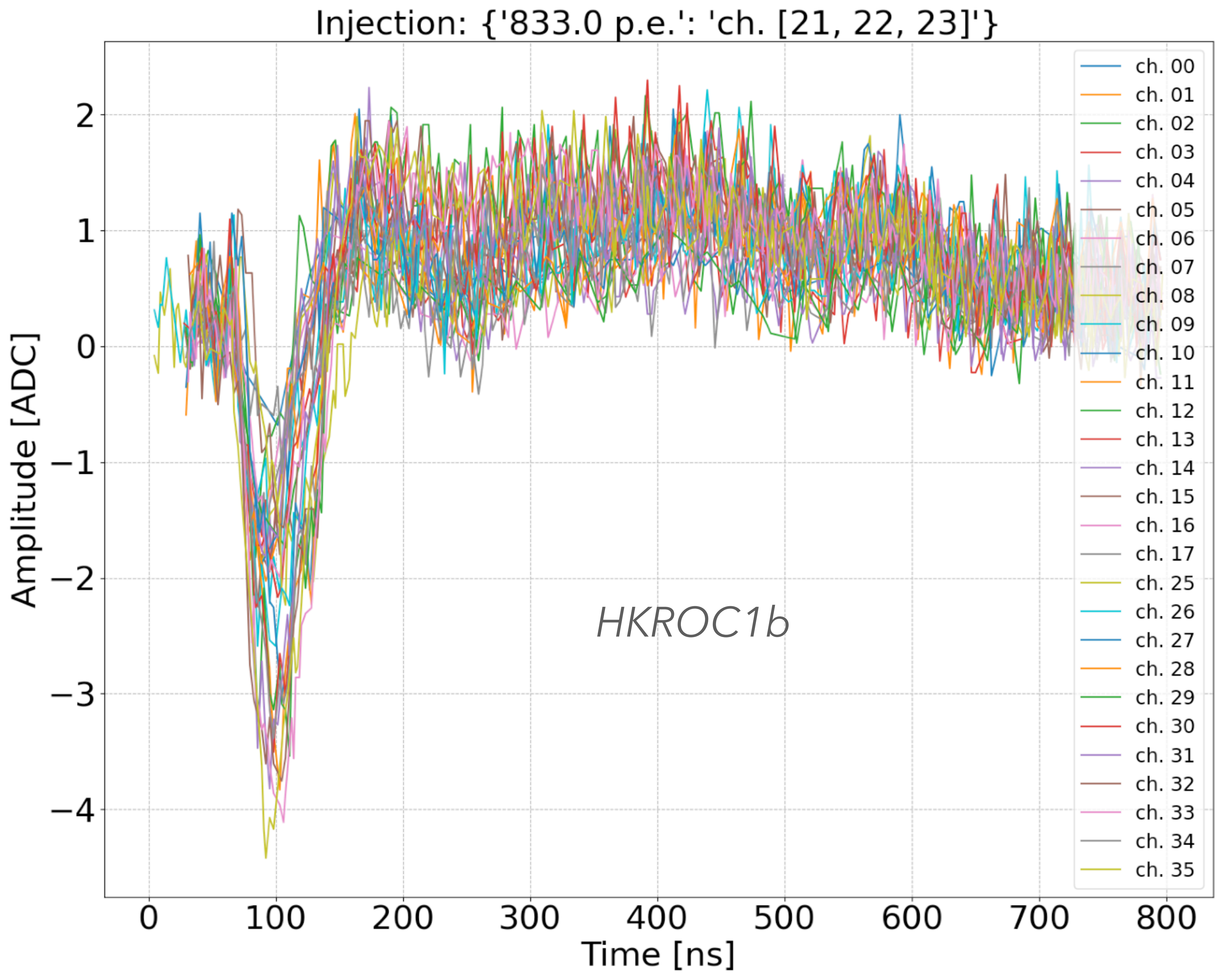
Linearity measurements - Diffuse cross-talk



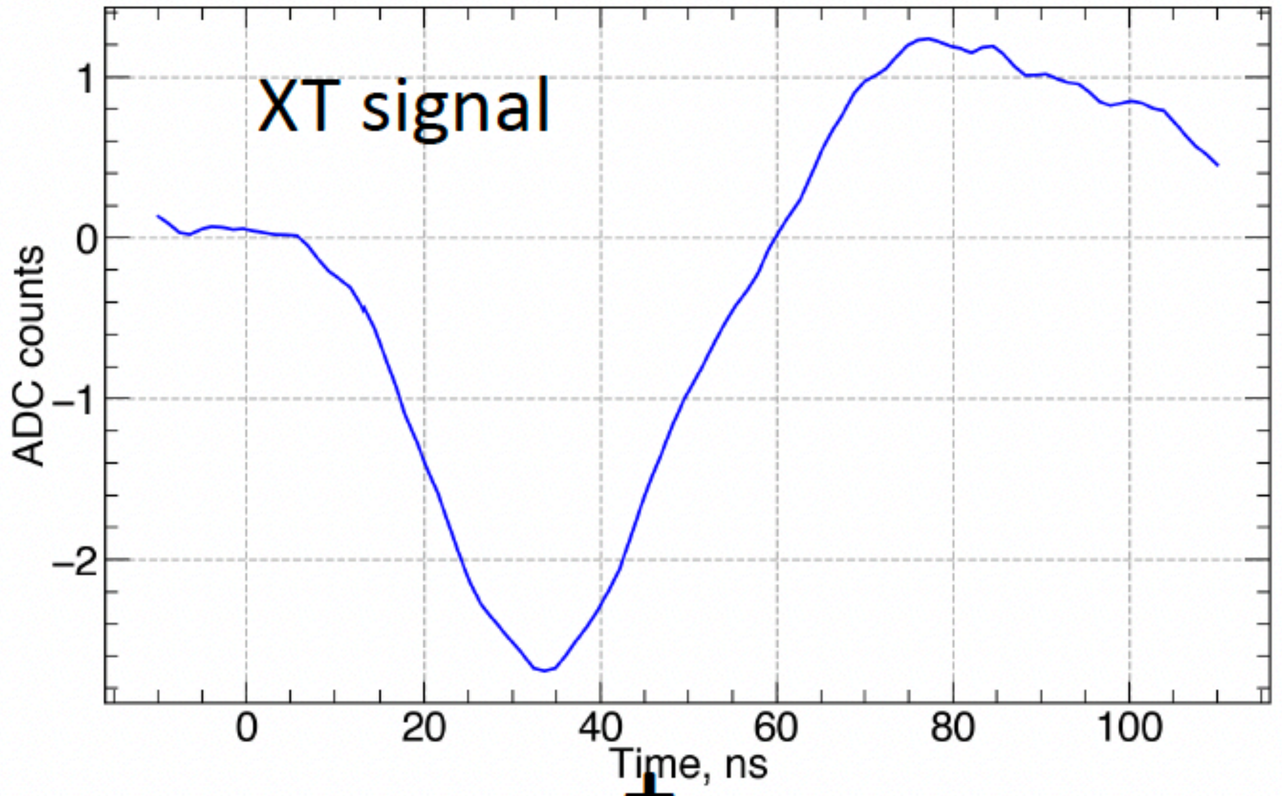


Diffuse-cross talk signal





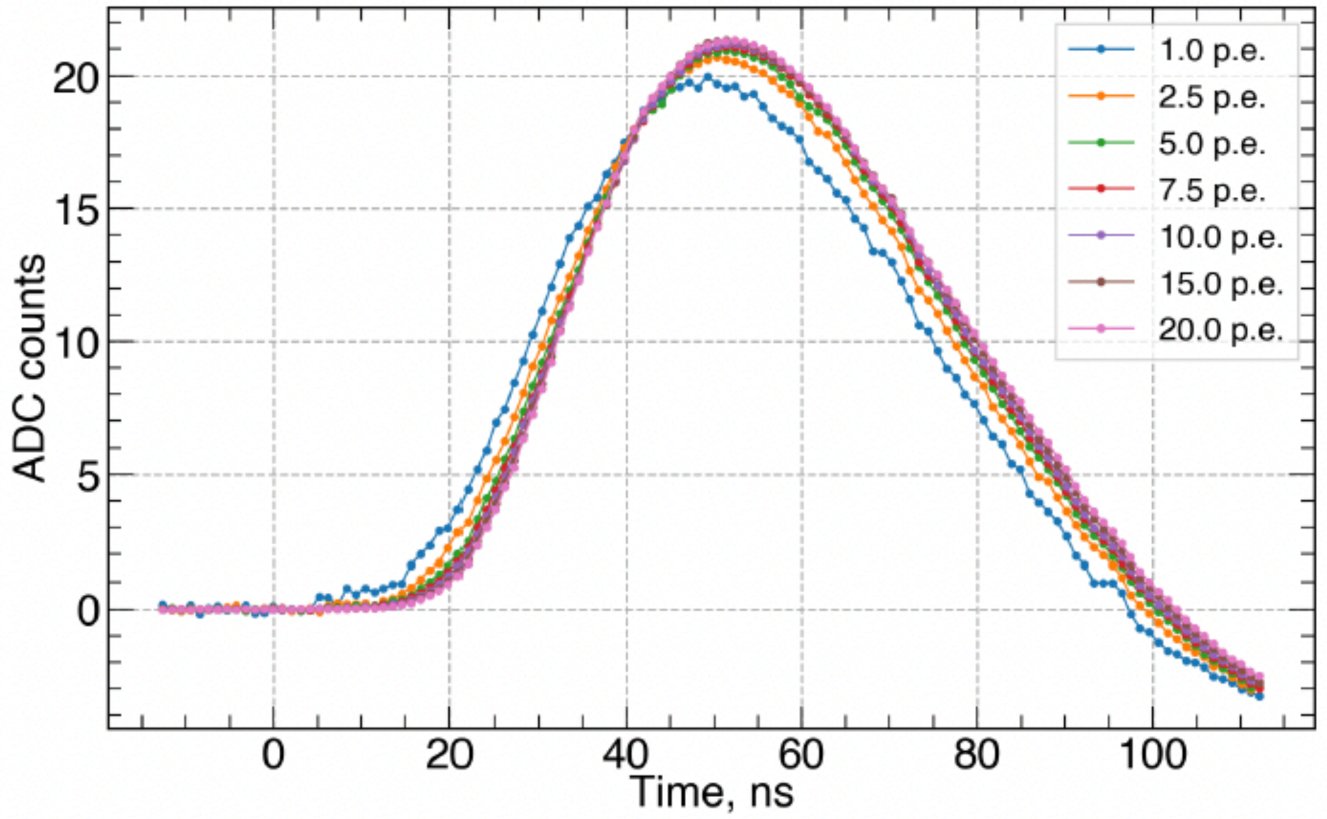
Charge reconstruction & Diffuse cross-talk

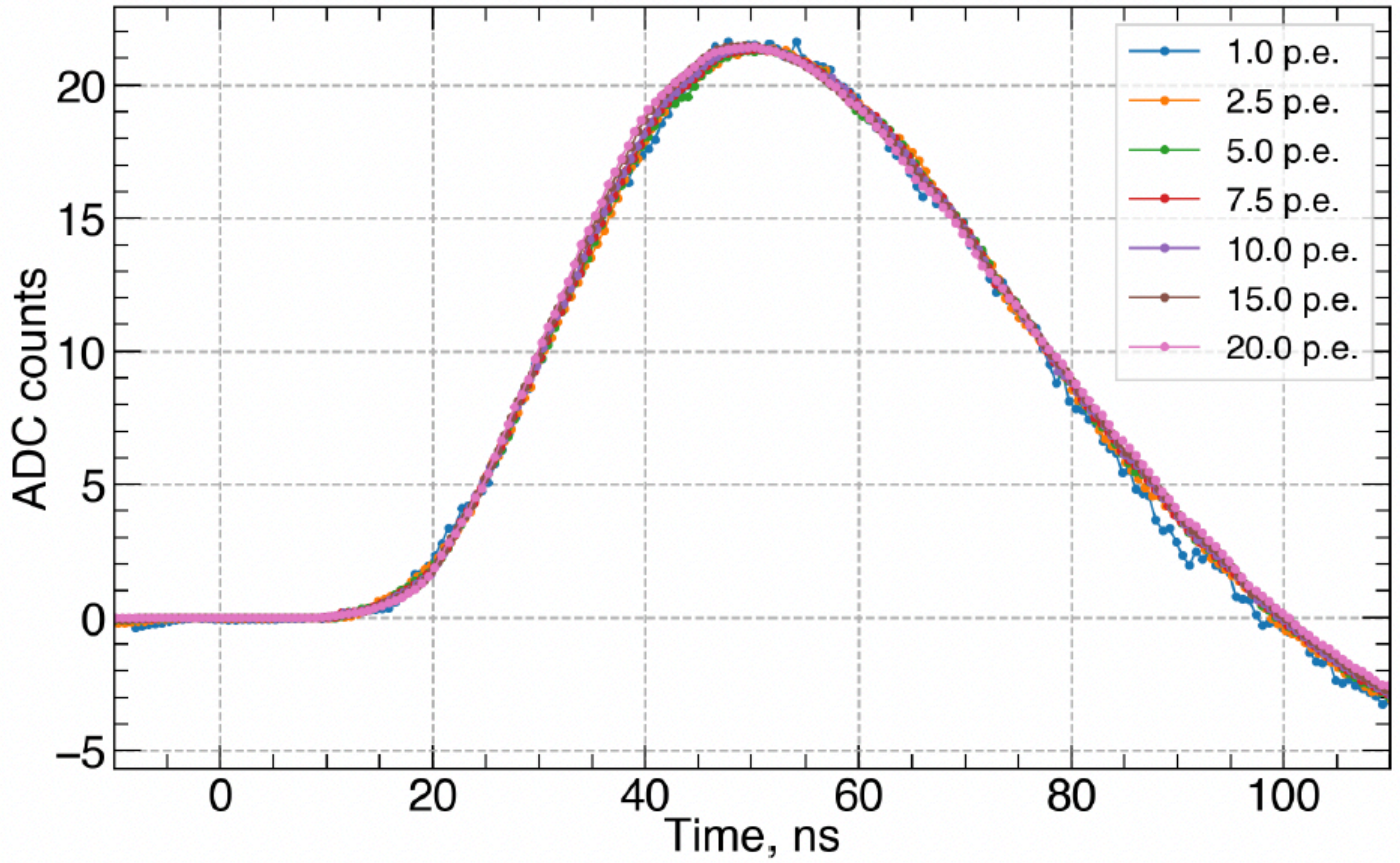


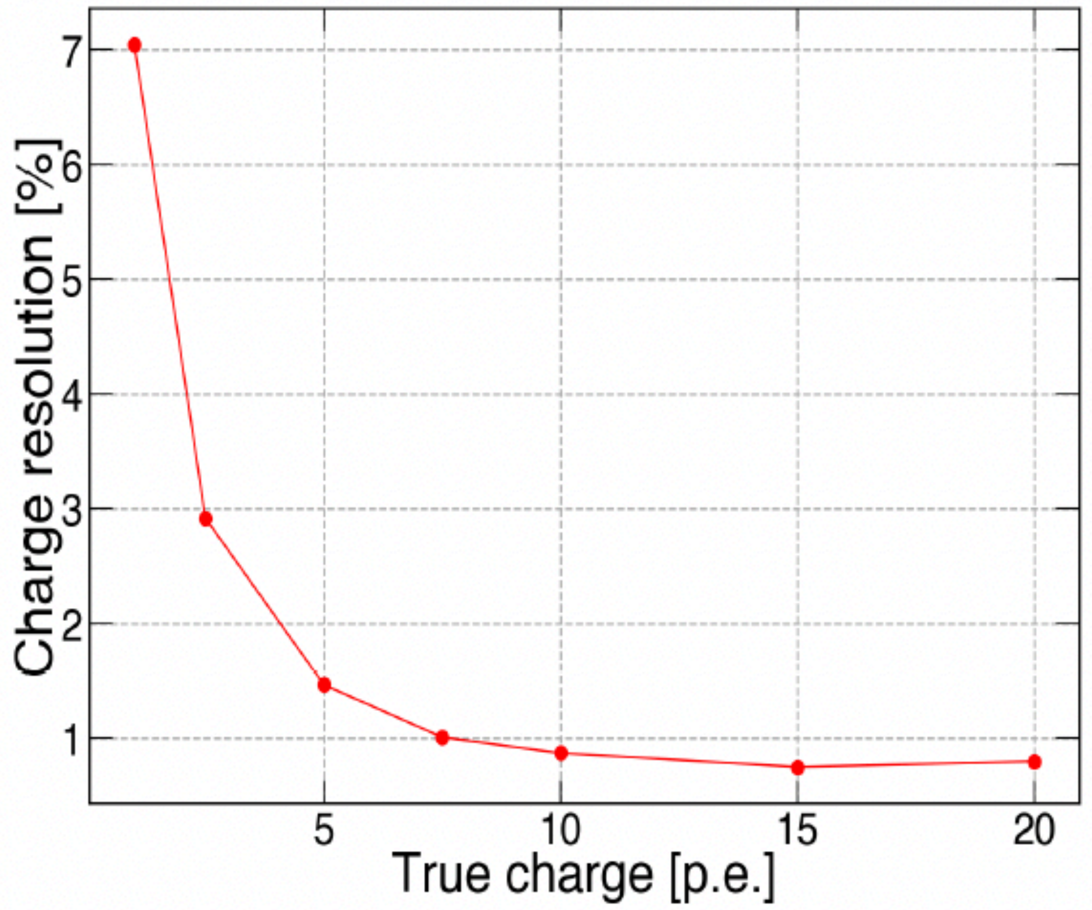
Performing joint fit

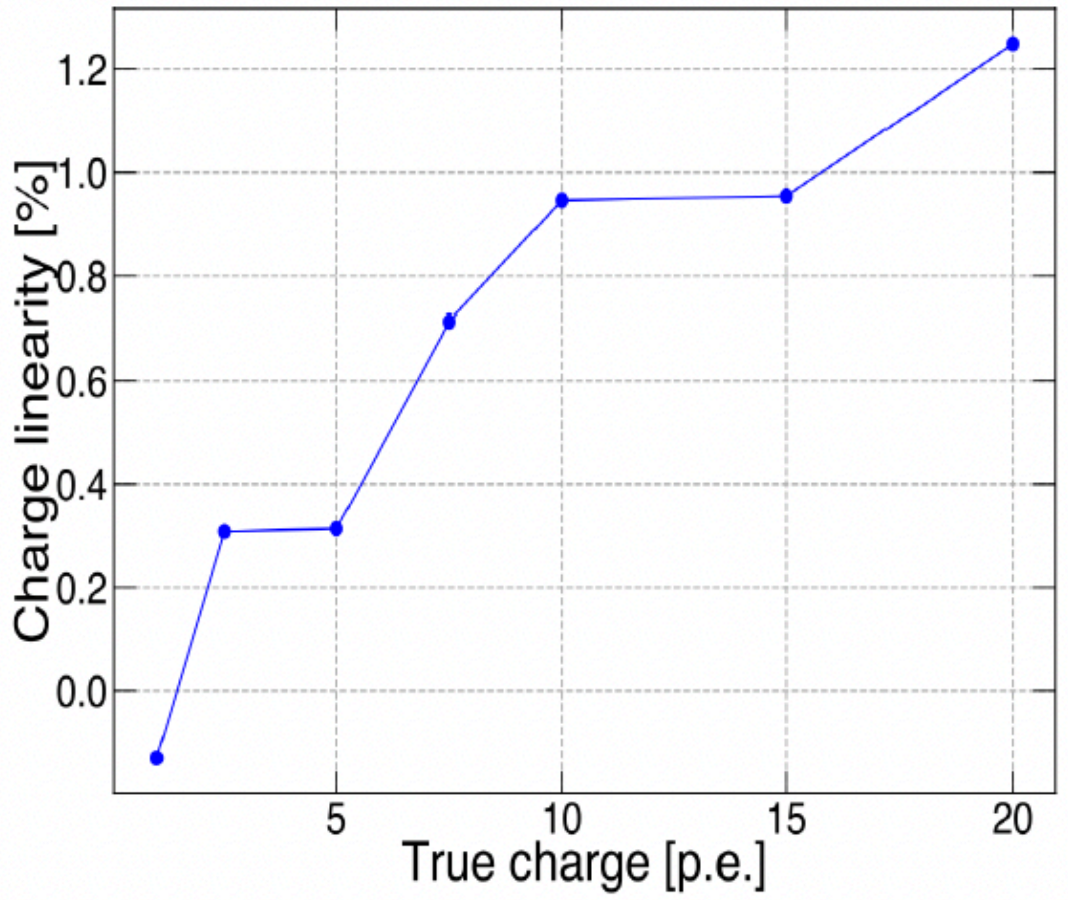
+

Normalised waveforms - direct measurments









- Diffuse XT impact can be removed/corrected thanks to waveform digitizer opportunities
- The same linearity and resolution as without XT

Noise trigger rate