# Overview of the ATLAS High-Granularity Timing Detector (HGTD): Project status and results


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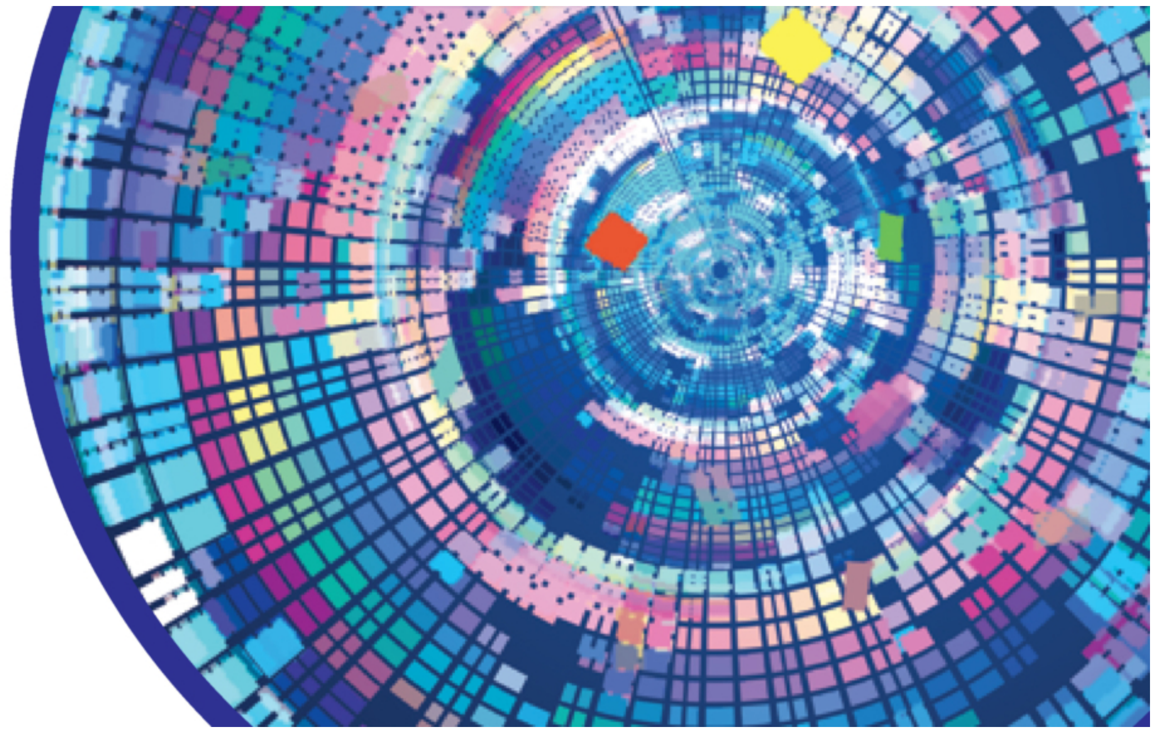
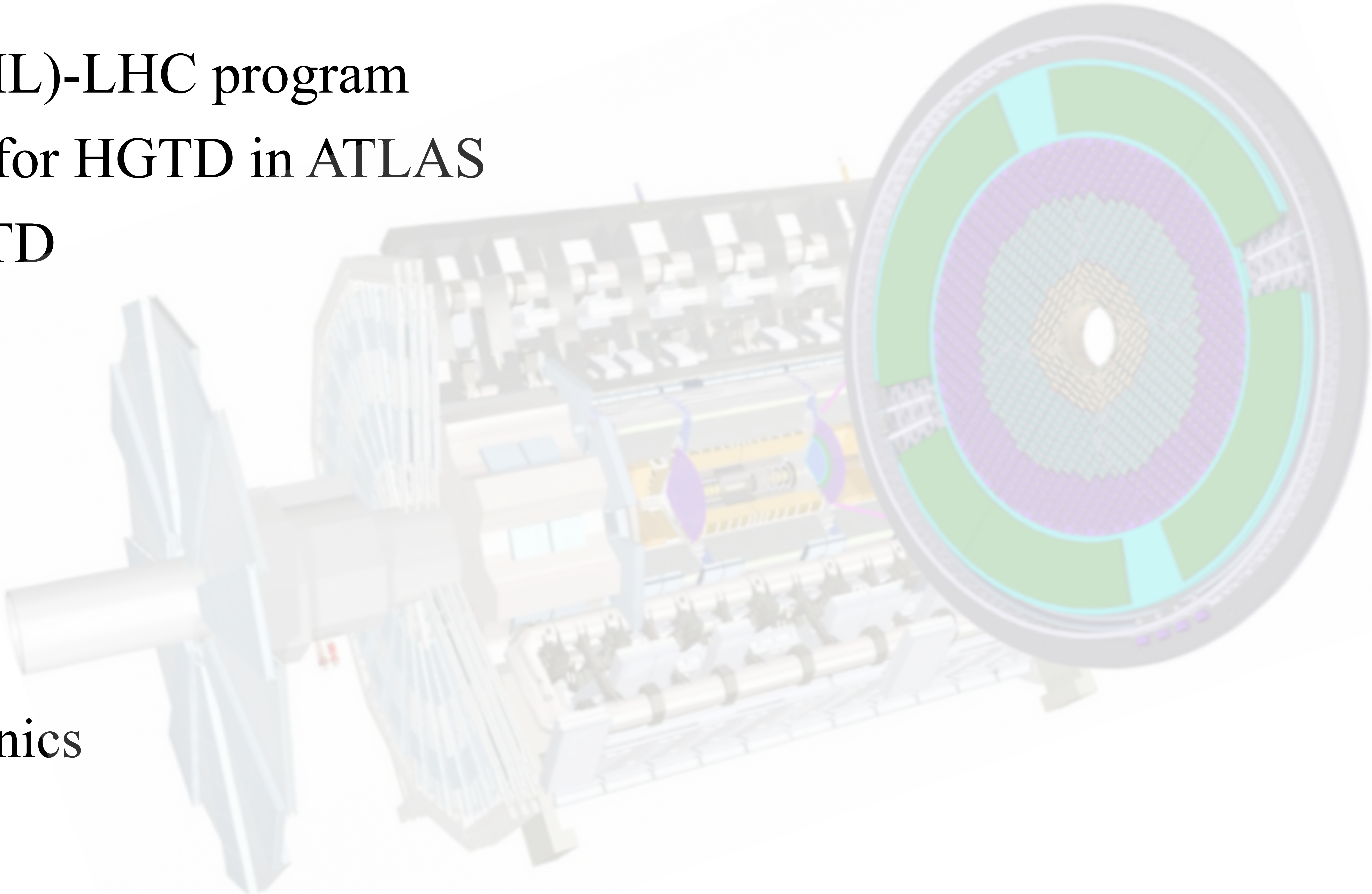
On behalf of ATLAS HGTD group



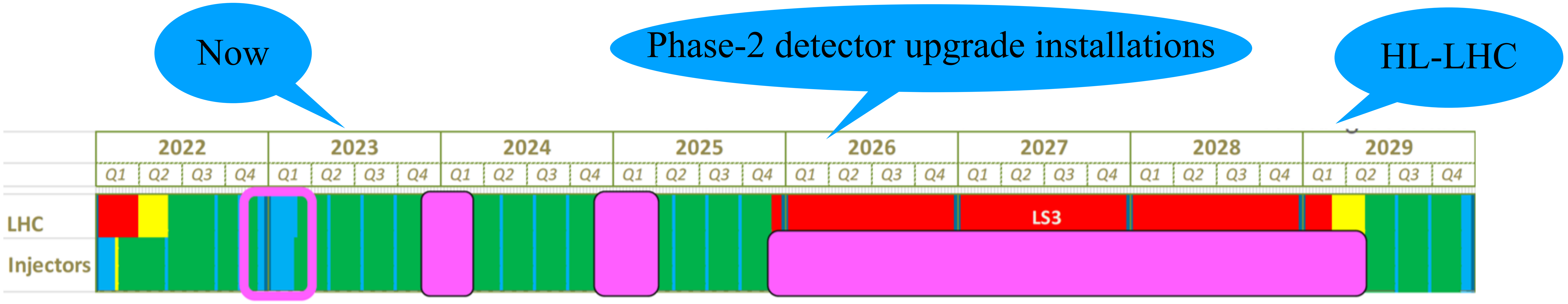


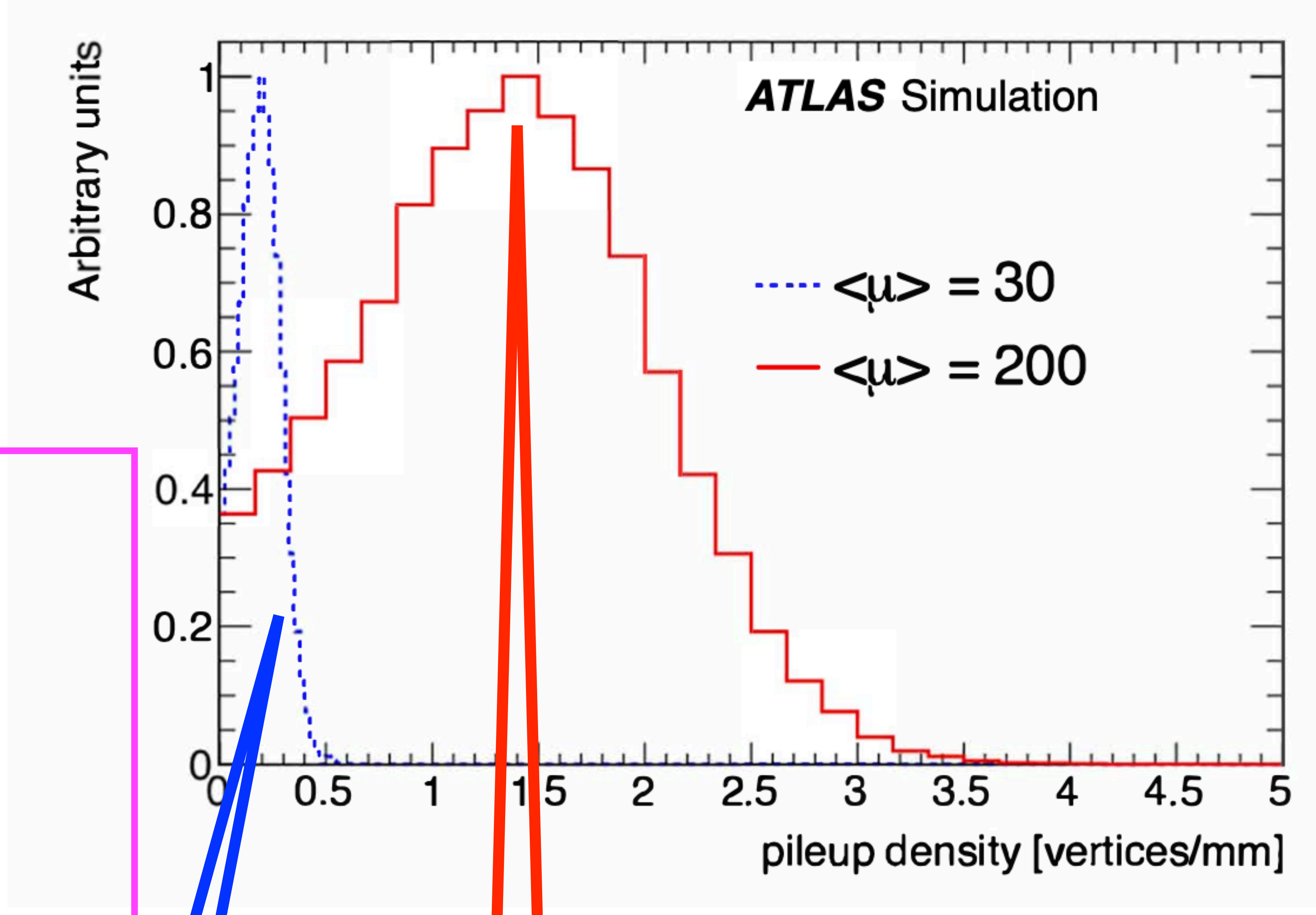
# Overview

- High Luminosity (HL)-LHC program
- Physics motivation for HGTD in ATLAS
- Introduction to HGTD
- HGTD Highlights
  - HGTD module
  - LGAD sensors
  - ASIC electronic
  - Demonstrator
  - Peripheral Electronics

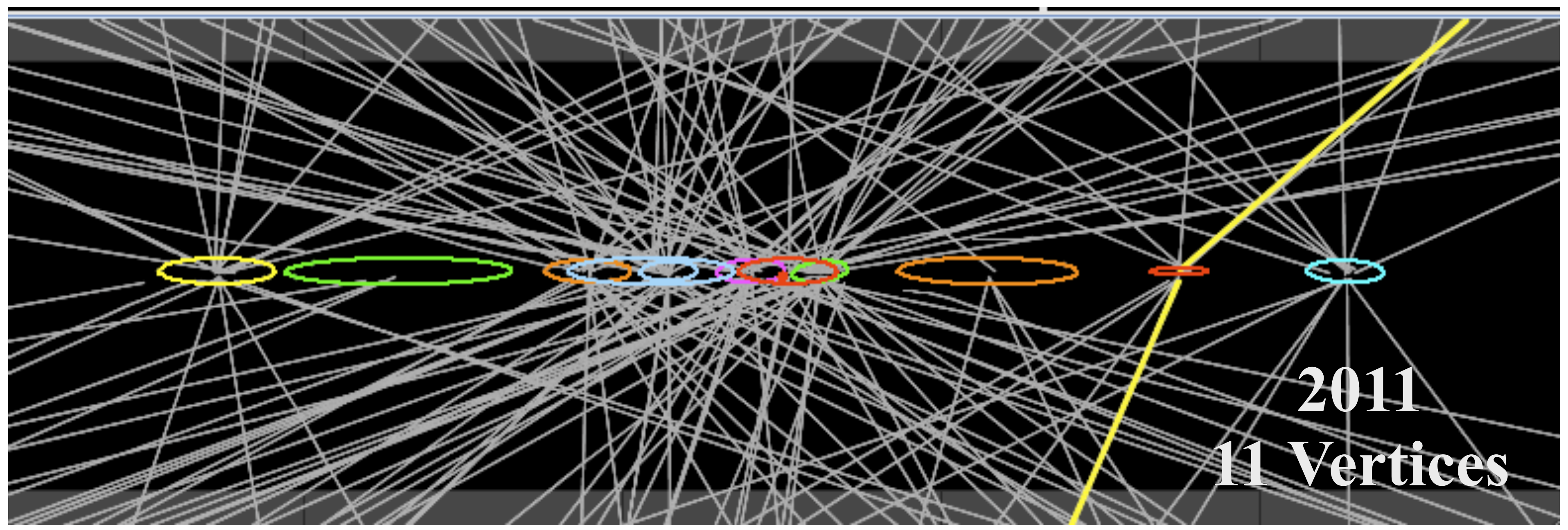


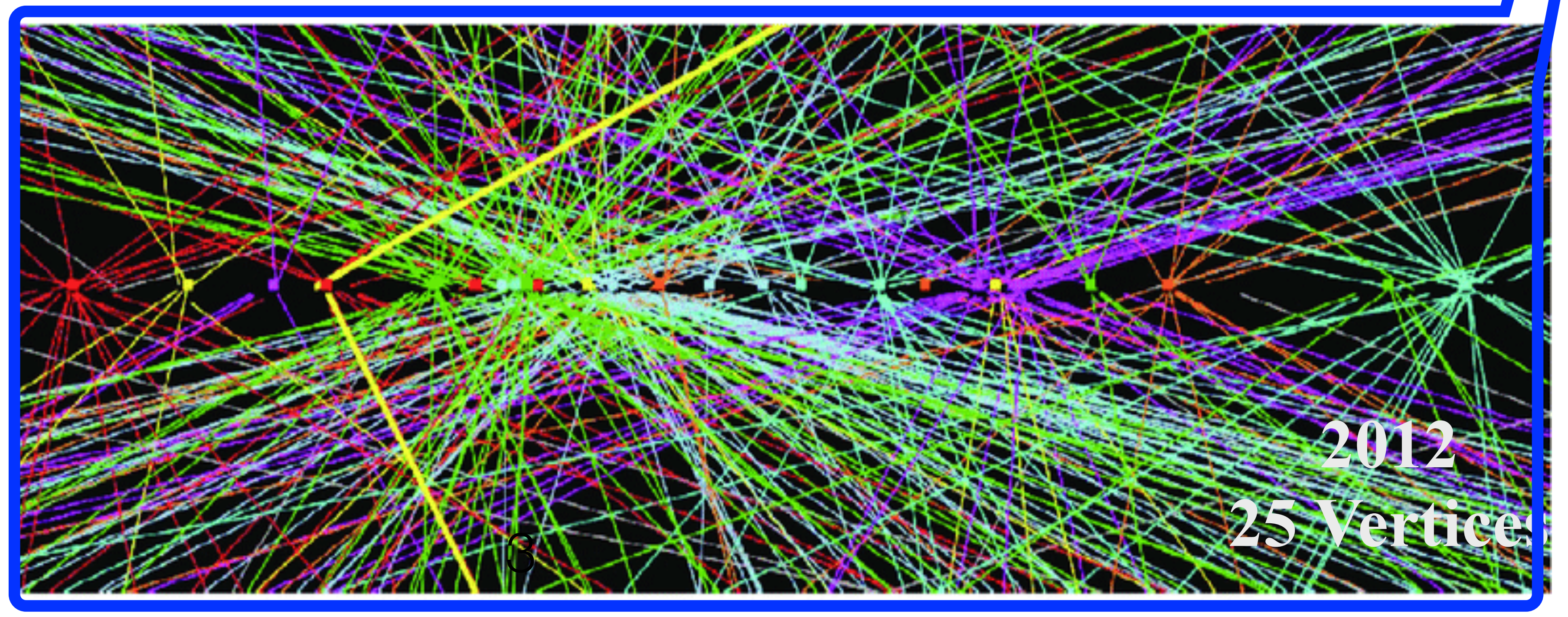
# High Luminosity (HL)-LHC program

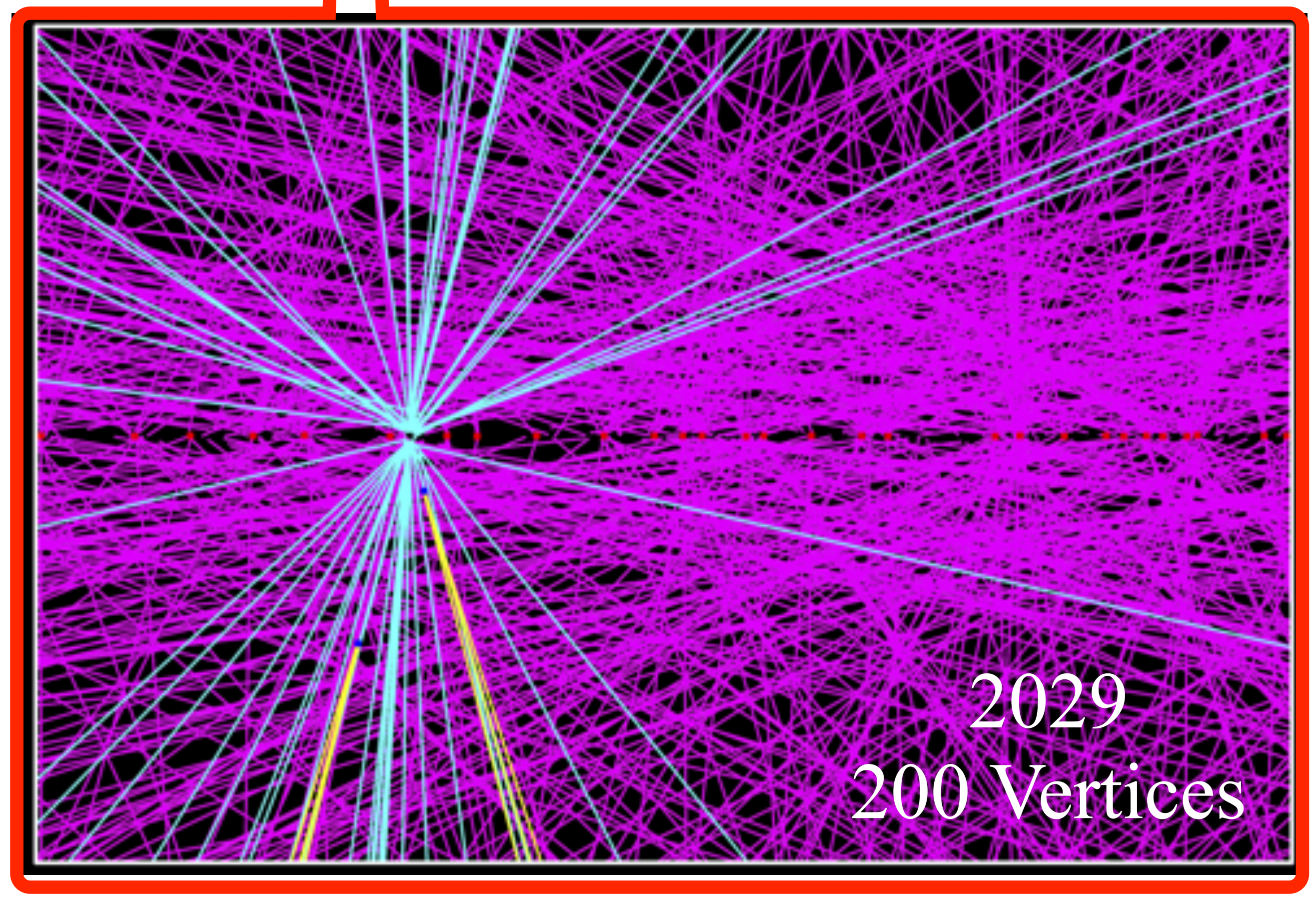



- HL-LHC instantaneous Luminosity will be $7.5 \times 10^{34} cm^{-2} s^{-1}$ (~ 5 times of Run2 )
  - Up to 200 inelastic pp-collisions (pile-up) on average per bunch crossing 1.8 vertices/mm expected
    - Challenging the reconstruction of primary vertices
  - Higher radiation requirement
    - Detector radiation hardness increased by an order of magnitude

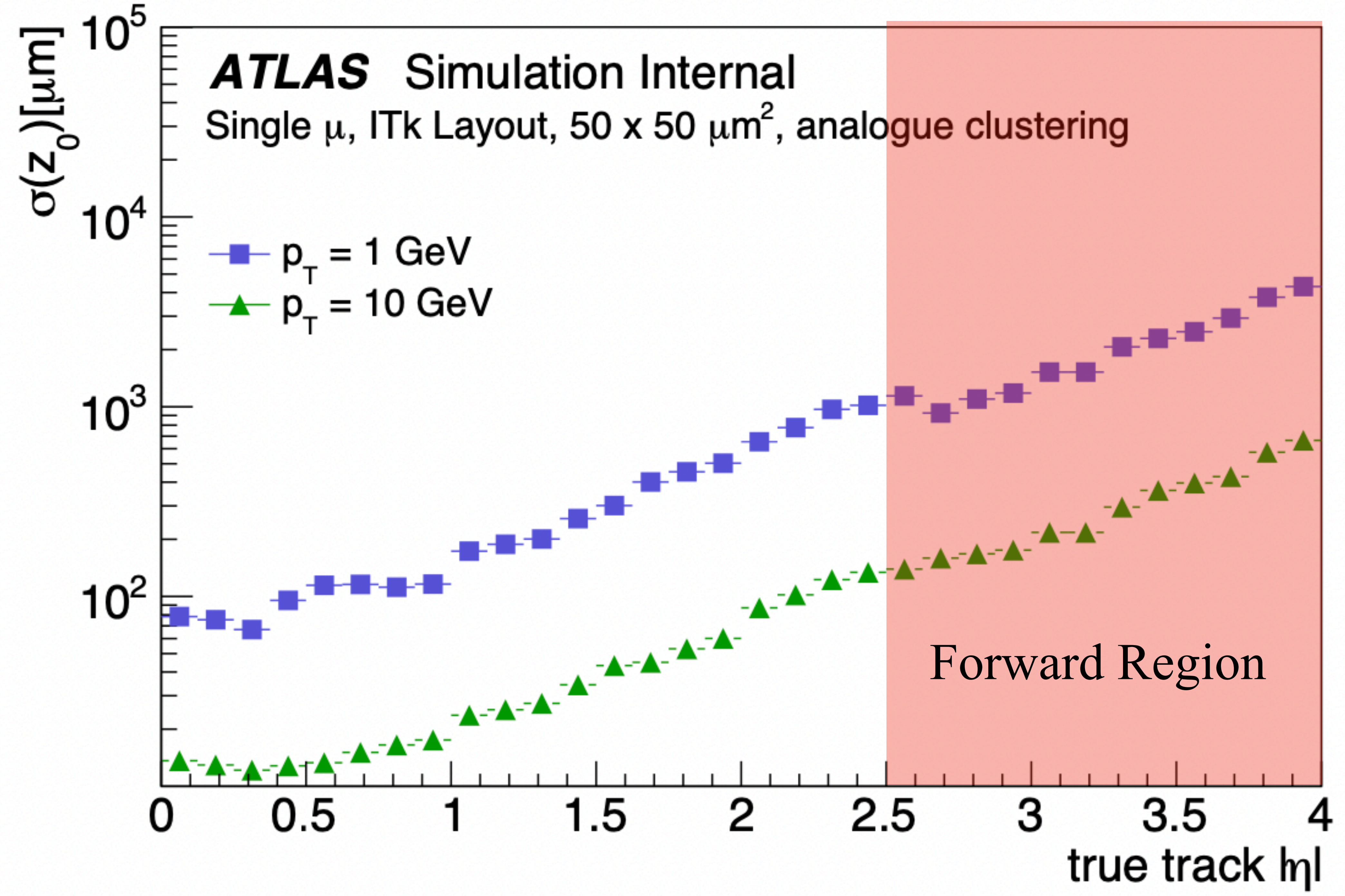


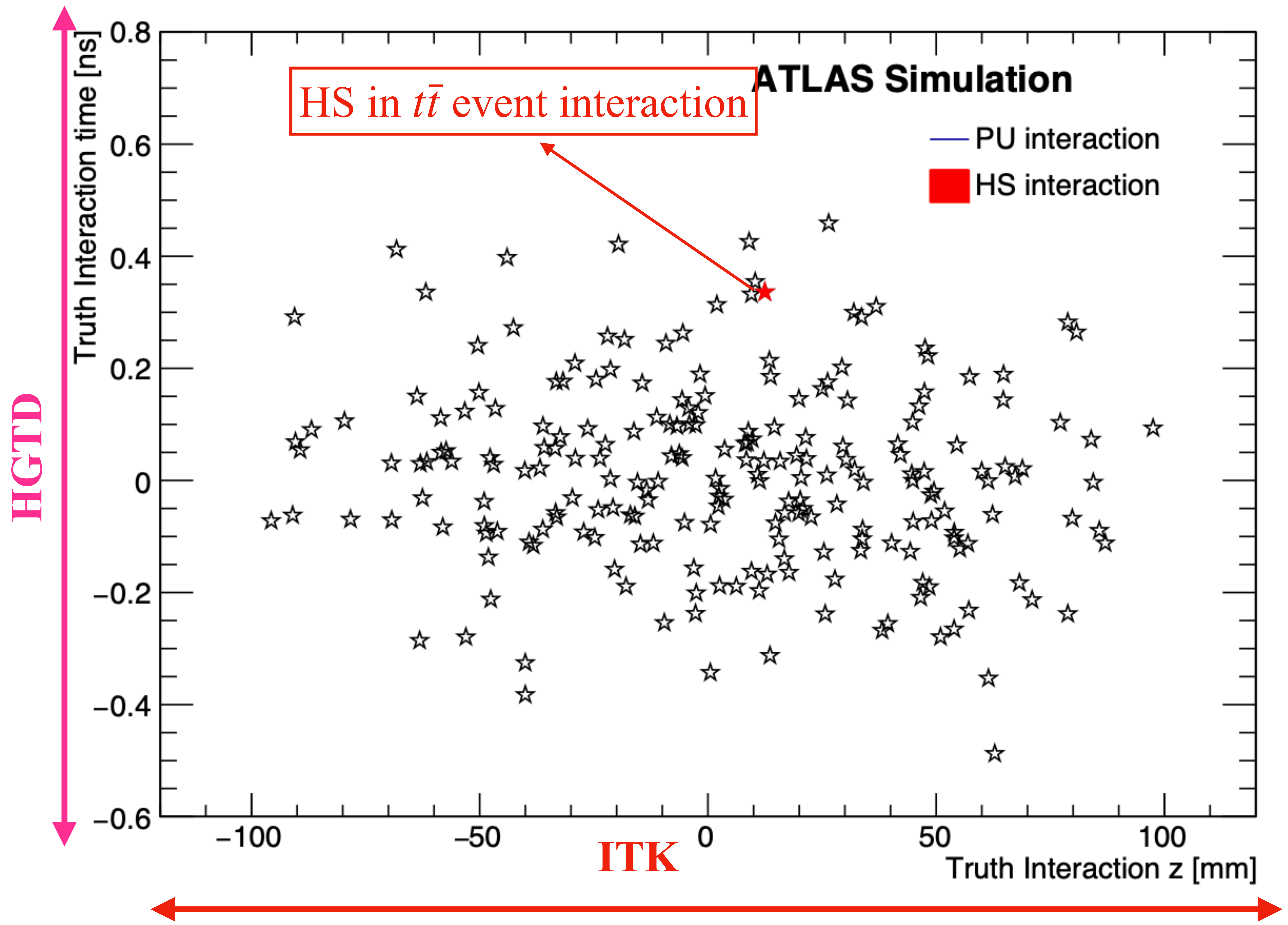



# Physics motivation for HGTD in ATLAS

- In HL-LHC the resolution in longitudinal direction (z) reduced in forward regions
  - Physics and object performance reduced as a result
  - Ambiguities in track-to-vertex information
  - Pile-up density > $z_0$ resolution
- Add timing information to improve pile-up rejection and object reconstruction

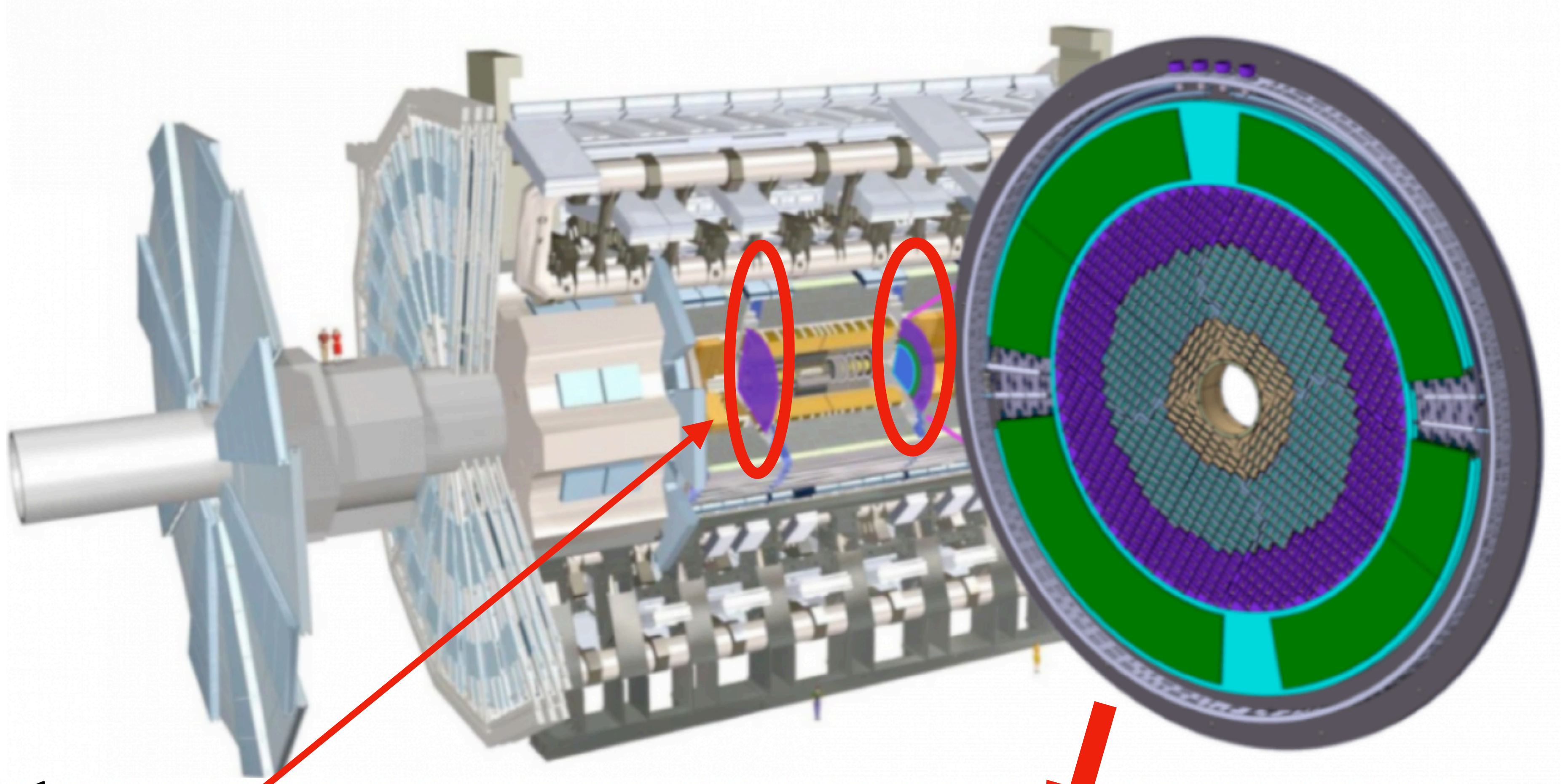


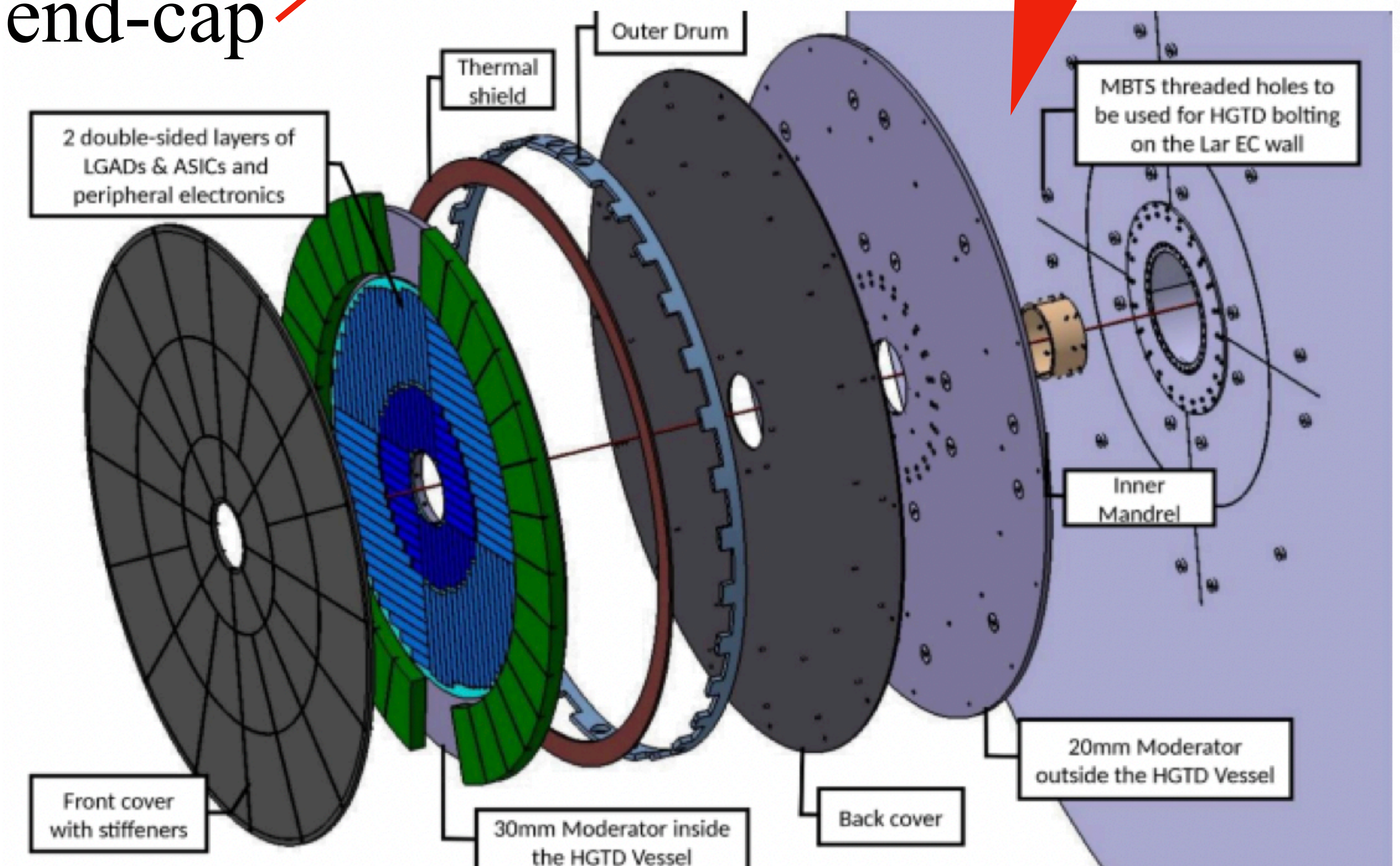

Truth interaction visualisation in single bunch crossing in the z-t plan

# High-Granularity Timing Detector (HGTD)

- The HGTD is being designed for operation with $\langle\mu\rangle = 200$ and a total integrated luminosity of 4000 $fb^{-1}$
  - Time resolution per track (hit):
    - 30-50 ps (35-70 ps)
  - Luminosity measurements, as luminometer
    - Goal for HL-LHC: 1% luminosity uncertainty
  - Approved by CERN LHCC in Sep-2019

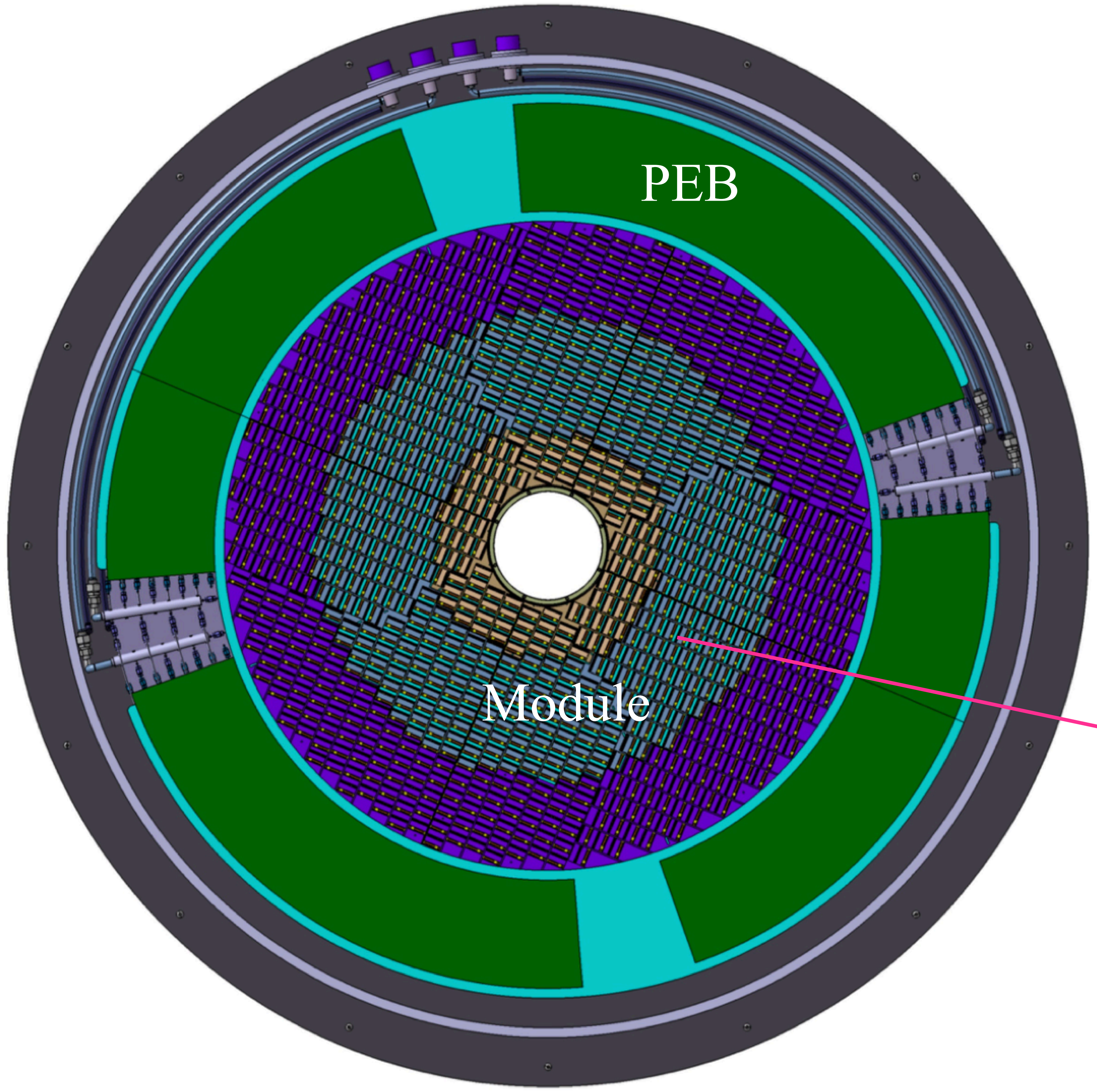


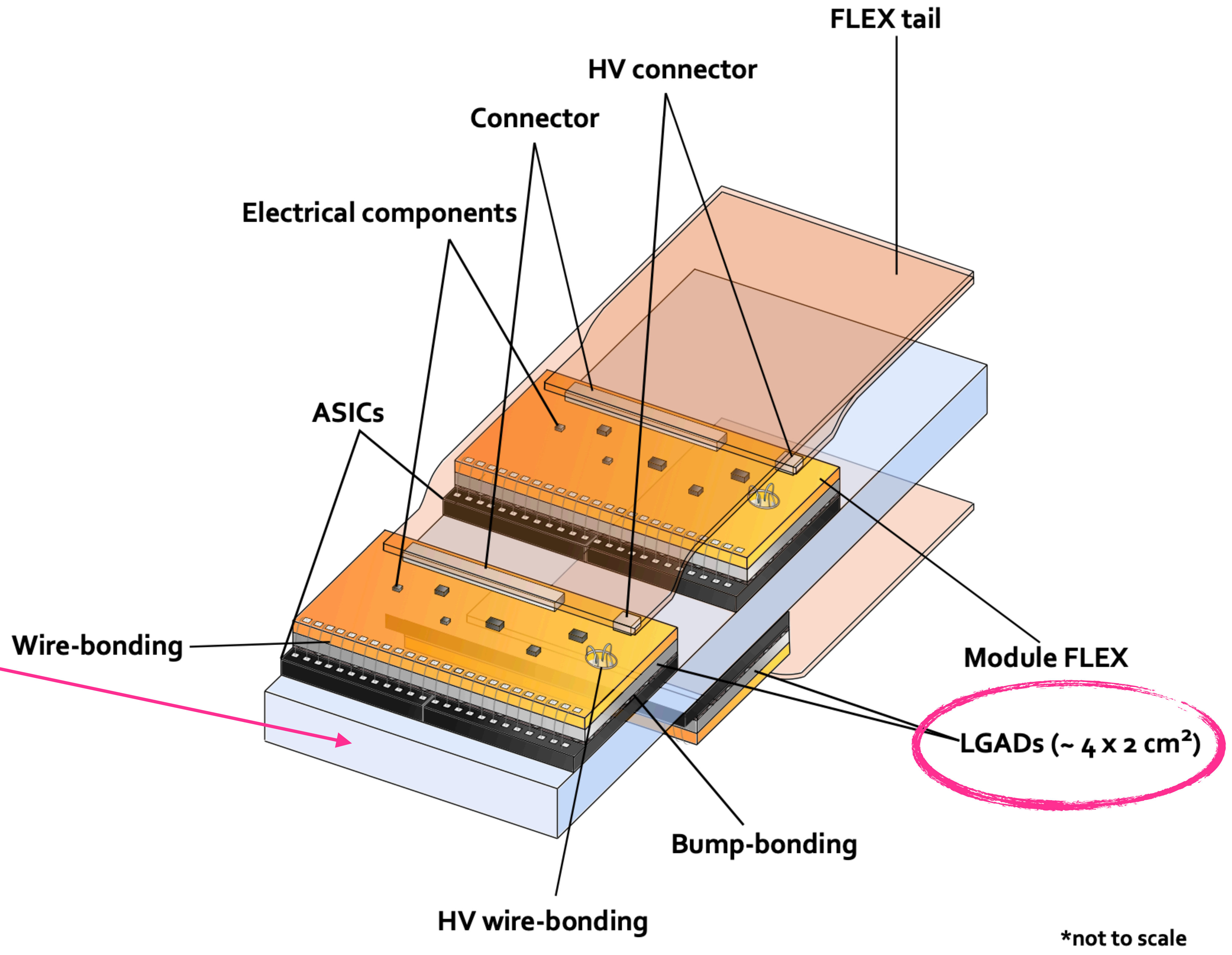
- Two HGTD end-up disks installed in the gap between barrel and end-cap
- z ~ ±3.5 m from the nominal interaction point
- Total radius: 11 cm < R < 100 cm
- Active region covering:
  - $2.4 < \eta < 4.0$, 12 cm < R < 64 cm
- Radiation hardness requirements:
  - $2.5 \times 10^{15}\ n_{eq}/cm^2$ (w/ Safety Factor =1.5) for sensor
  - 2 MGy (w/ SF = 2.25 for electronics)



# HGTD Module

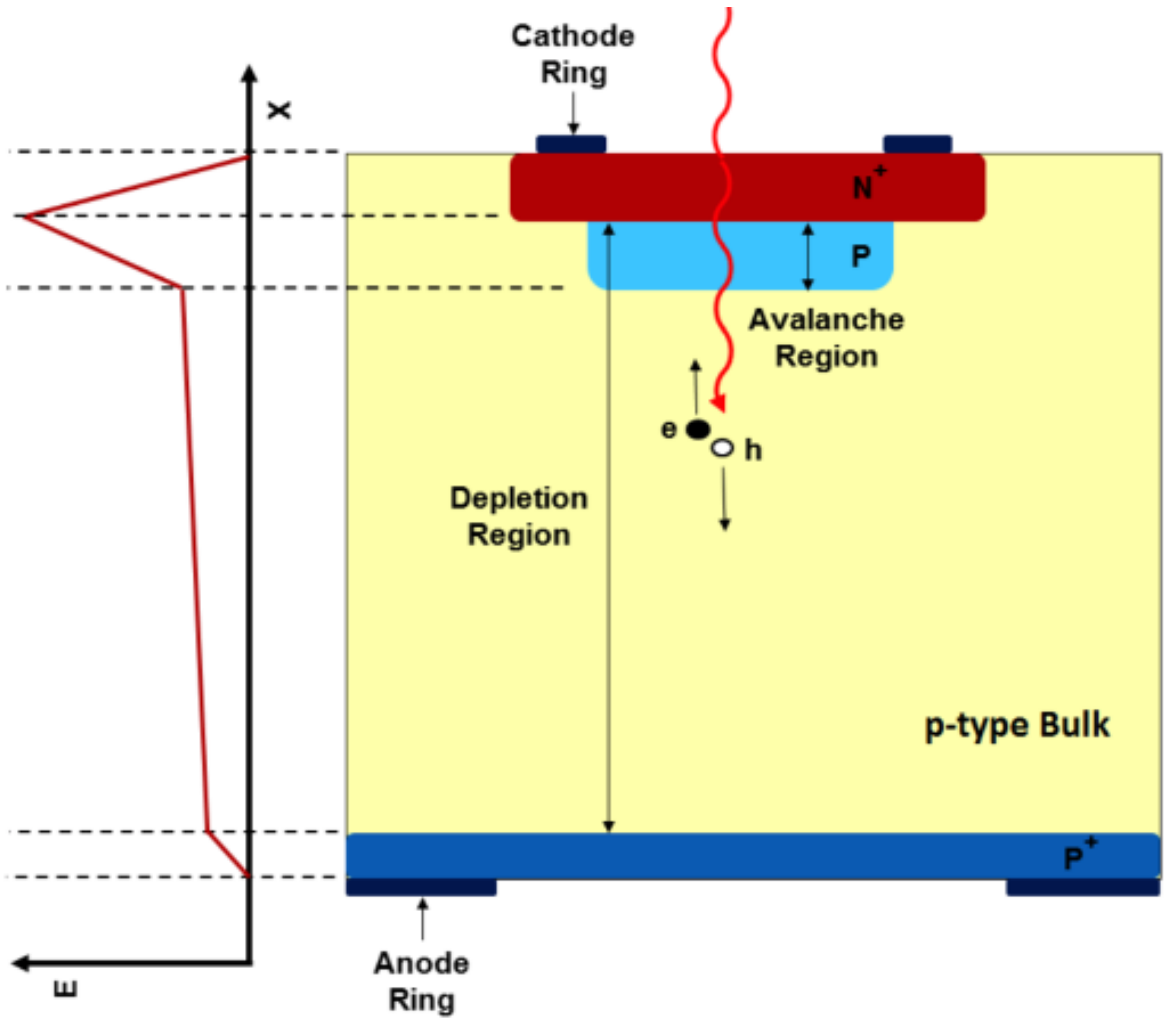
- HGTD will have double-sided disks equipped **with 8034 modules,** surrounded by Peripheral Electronic Boards (PEB), a Printed Circuit Board (PCB) dedicated for power and readout
- Consists of a LGAD sensor (15 × 15 pads) interconnected to the **ALTIROC** readout chip through bump- bonding
- Each module consists of two bump-bonded **sensor+ASIC** combinations, glued and wire-bonded to a **module flex**



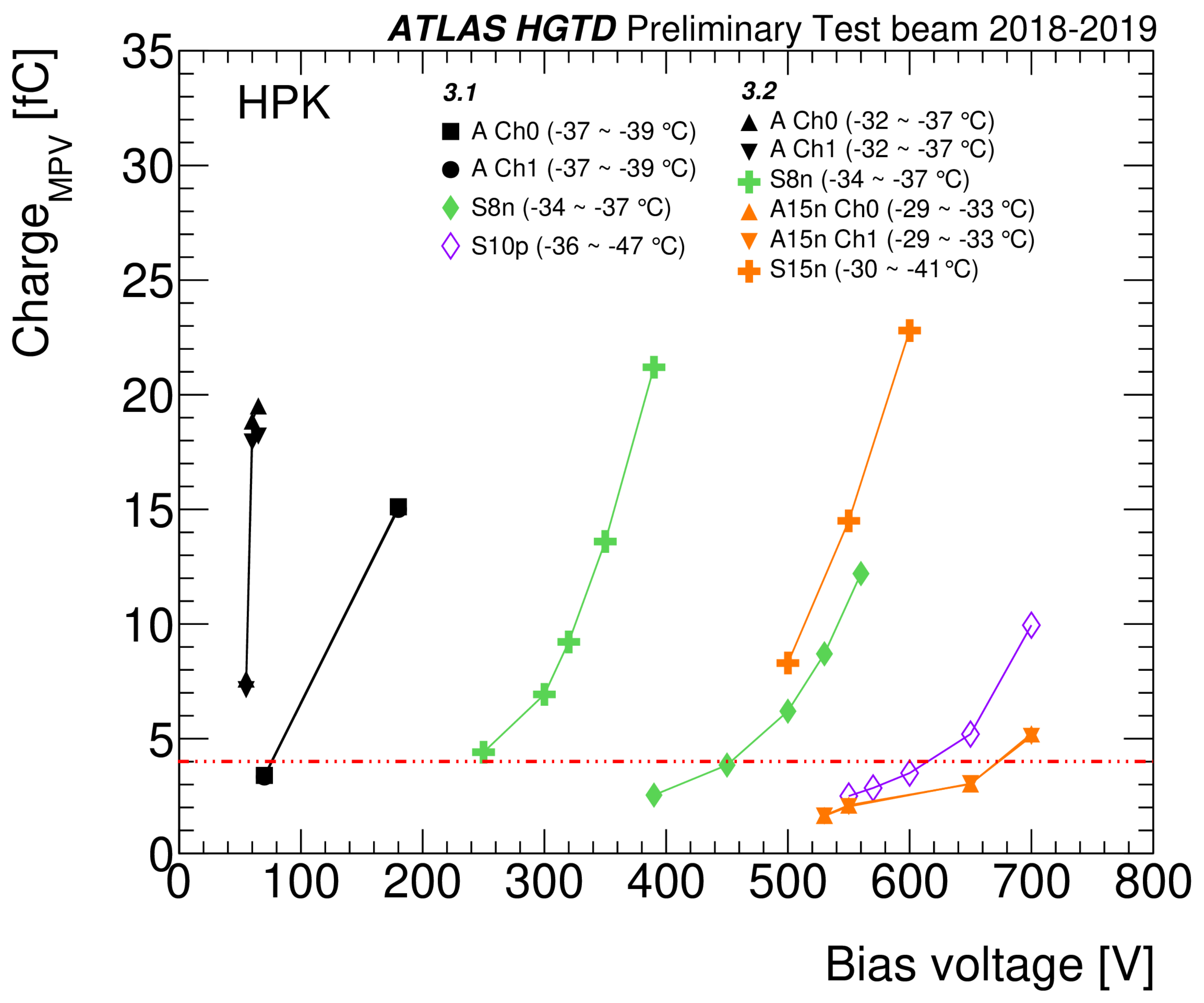
# Low Gain Avalanche Diode: Sensors

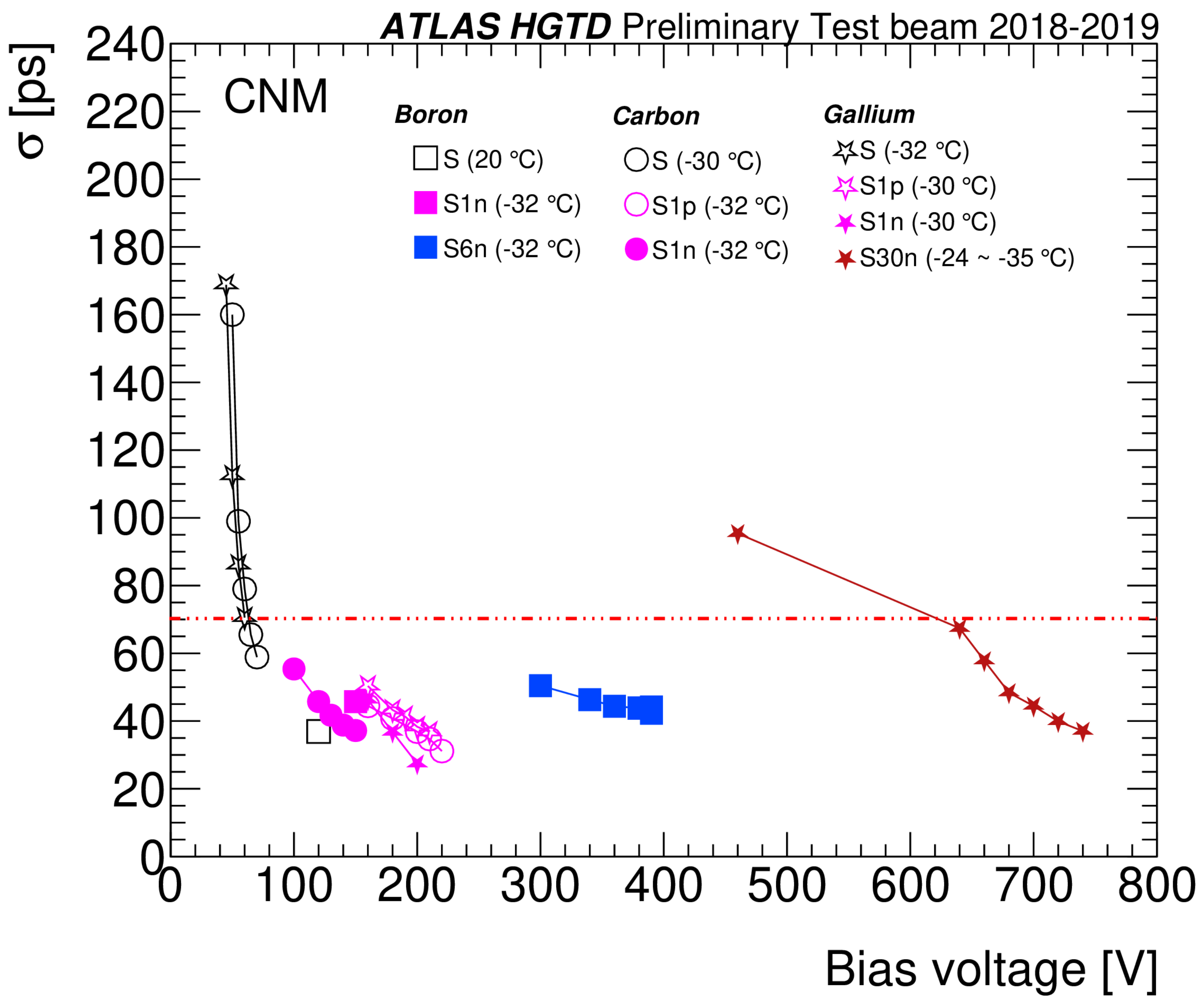
- LGAD sensors are an advanced type of silicon photodetector that harness the avalanche multiplication effect to amplify signals
- LGAD sensors operate in a low gain mode, ensuring linearity and reducing excess noise
- LGAD specifics for HGTD
  - 50 μm thick
    - Compromise between Landau fluctuations contributing to the time resolution etc
  - Pad size1.3 ×1.3 mm²
    - Compromise between rise time, capacitance, occupancy
  - Signal level: 10 fC (w/20 gain) before and 4 fC (w/8 gain) after irradiation

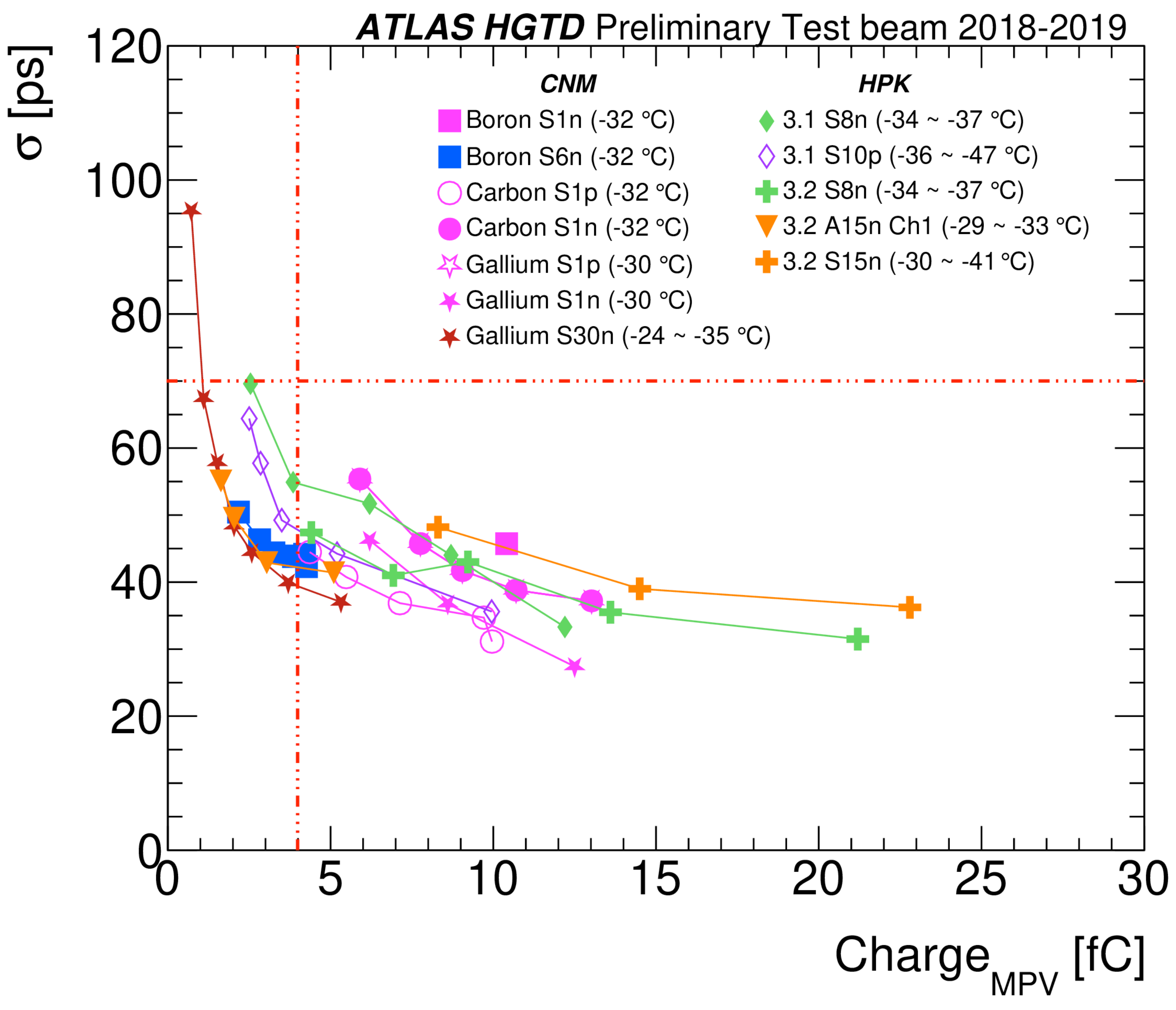


# Sensor performance measurements: Testbeam

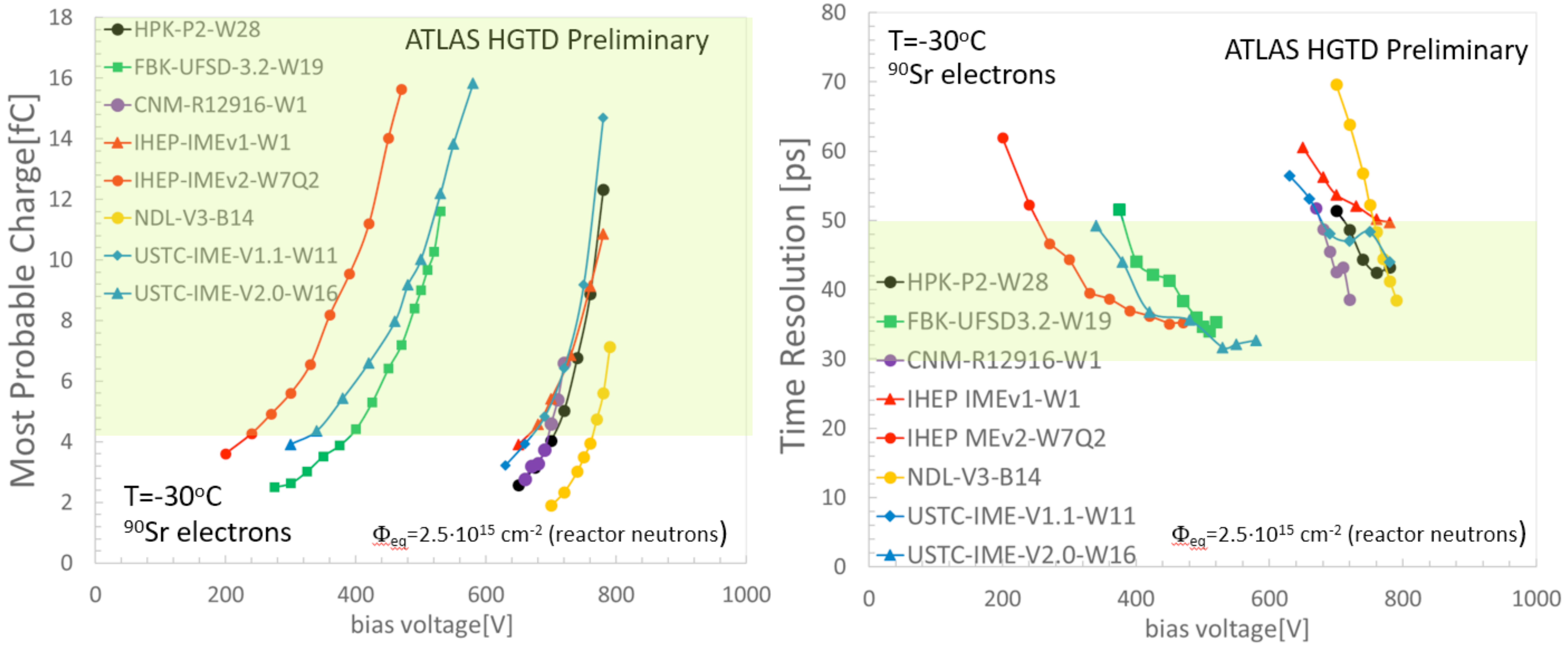
- Published paper on summarising the testbeam results
  - C. Agapopoulou et al 2022 JINST 17 P09026
- For more details about the latest test beam results please see Mei Zhao’s talk on September 7 (Link)



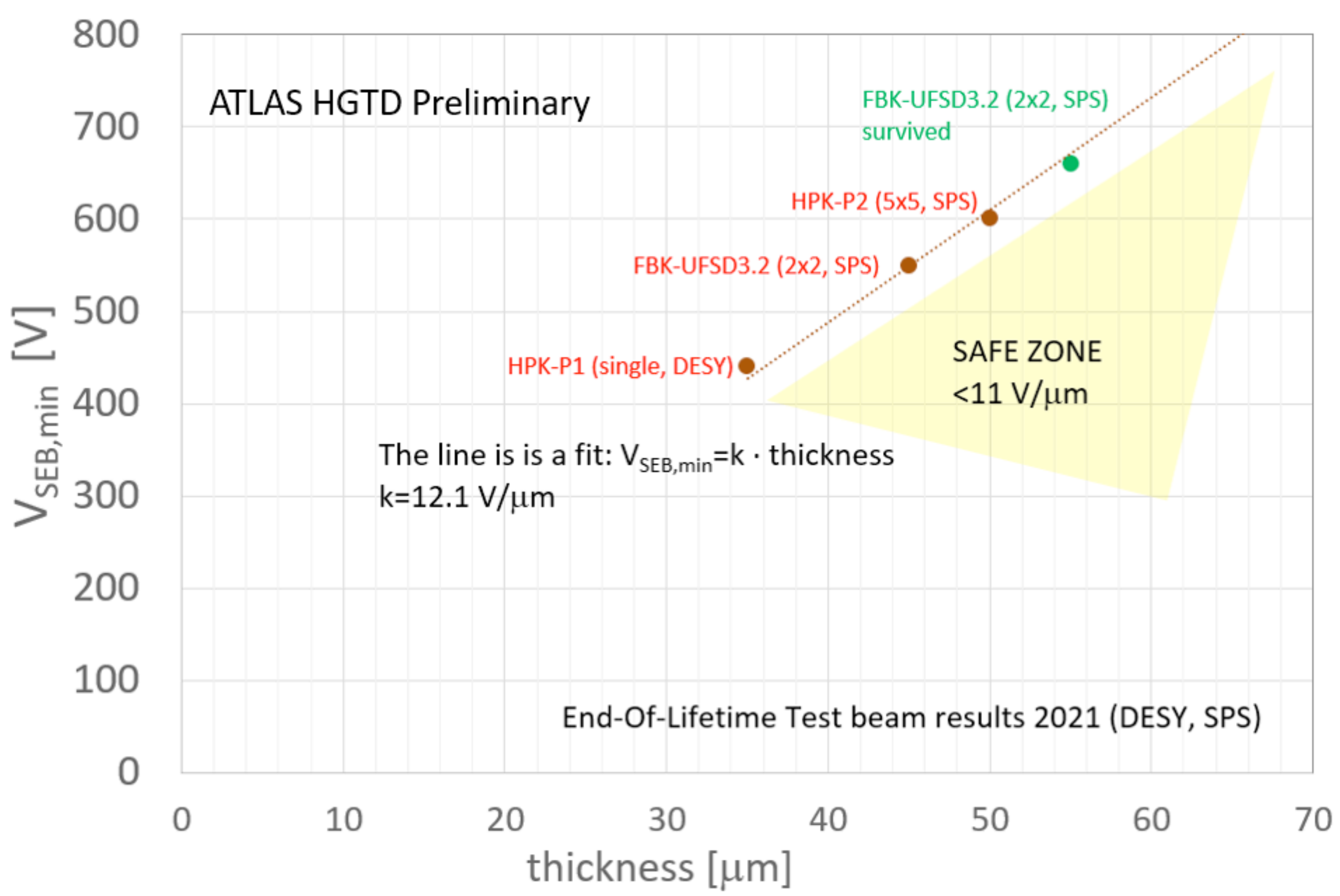
# Study of LGAD performance: Lab

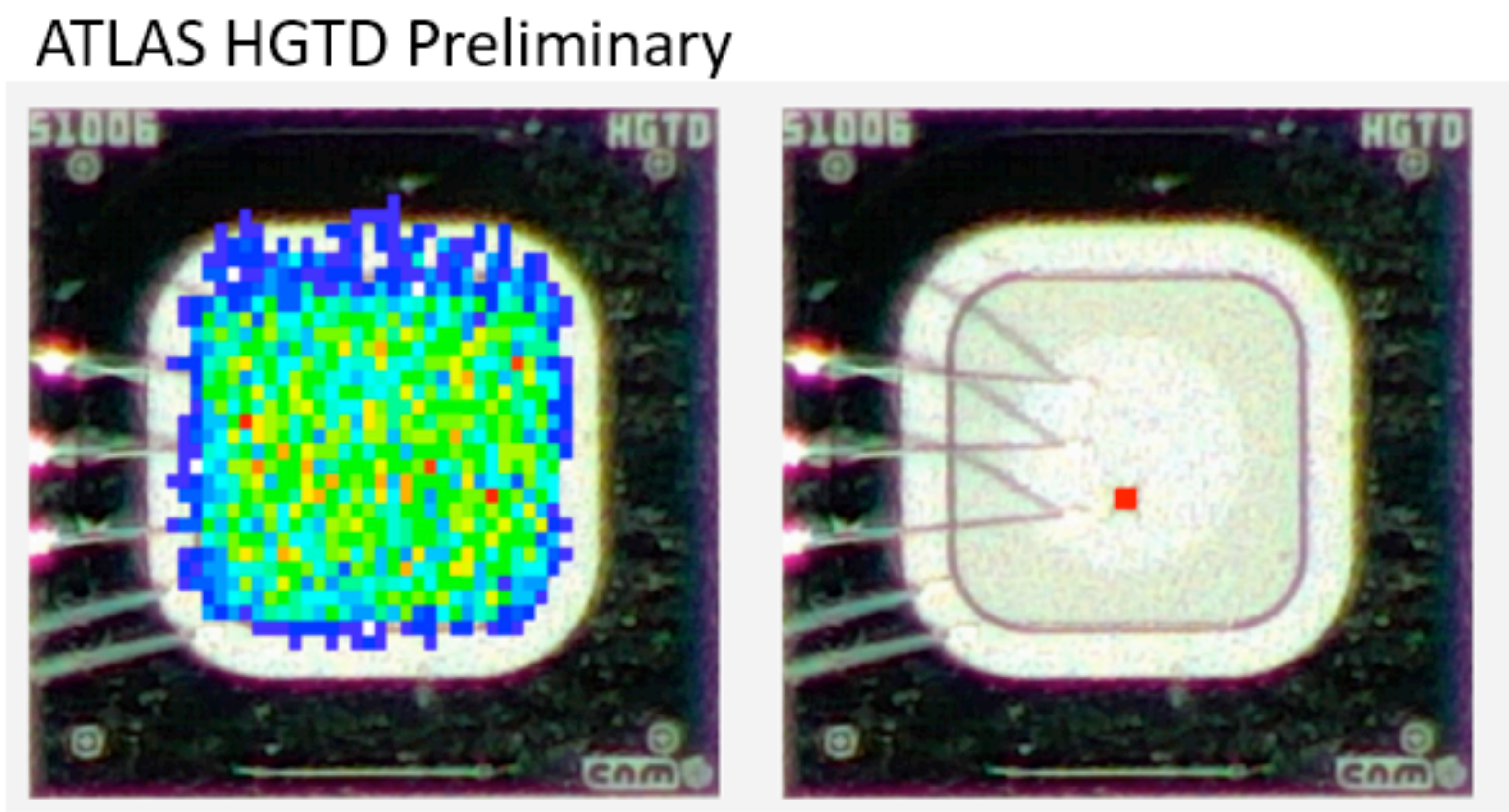


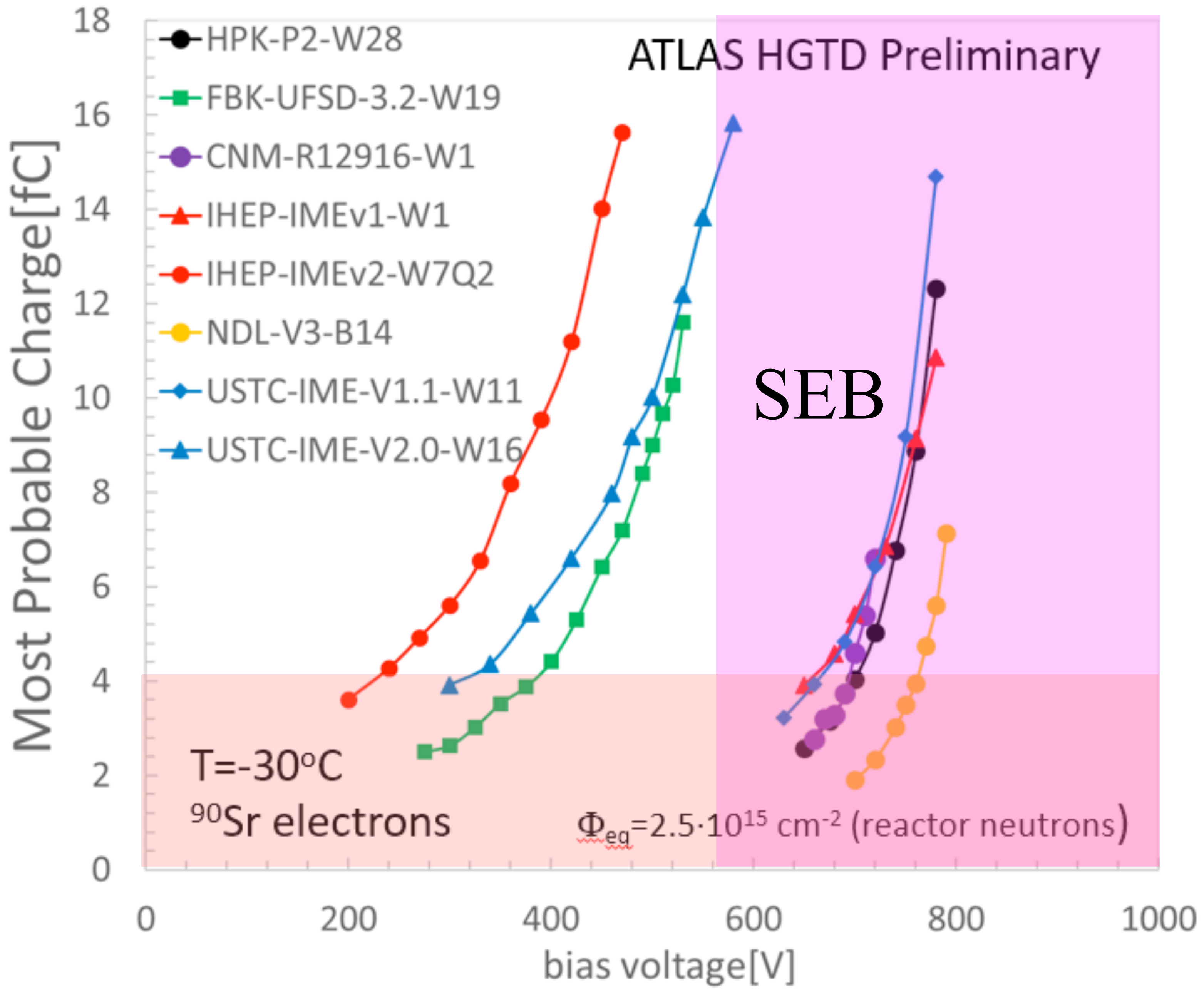

- The target collected charge is 4 fC and time resolution of 50 ps for the HGTD
- Carbon enriched sensors (IHEP-IMEv2-W7Q2, FBK-UFSC-2.3-W19, USTC-IME-V2.0-W16) show stable performance at much lower bias voltages than non-carbon enriched sensors

# LGAD Single Event Burnout

- Single Event Burnout (SEB)- when heavily irradiated sensors (~ end-of-life 2.5 x $10^{15}$ $n_{eq}/cm^2$) operated with high bias voltage
  - No issue if operated with lower voltage!
  - A single particle which deposits enough energy (~tens MeV) causes: conductive path leading to destructive breakdown
- Confirmed & cross checked with R&D at CMS and RD50
- Bias voltage safe from SEB: < 11 V/µm (i.e. ~< 550 V for 50 µm)



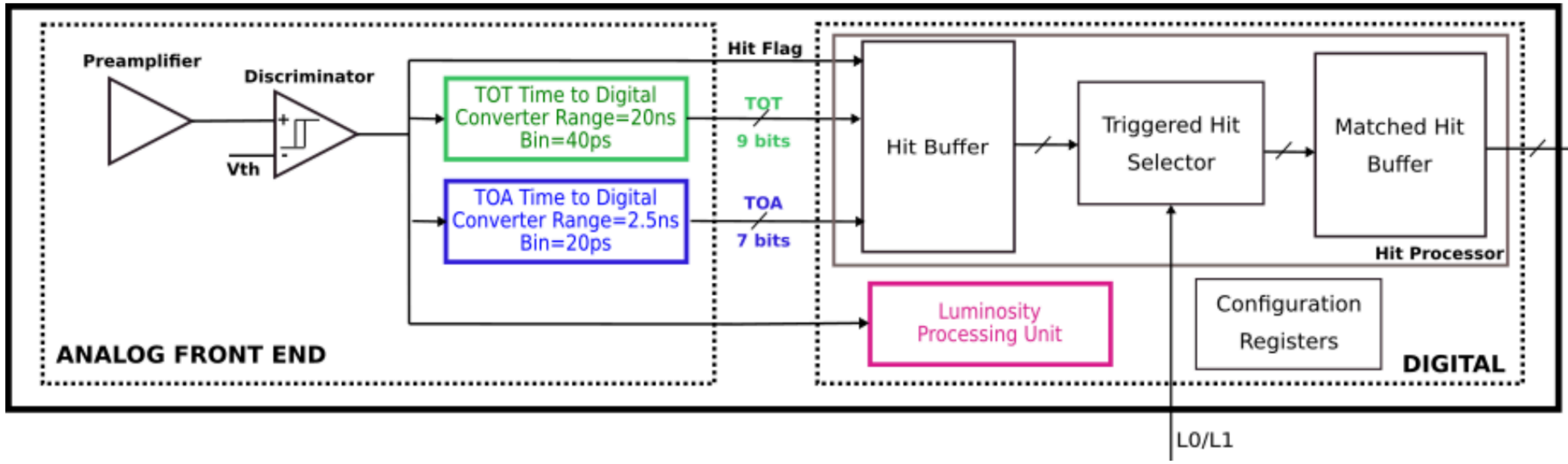



# ALTIROC: LGAD's ASIC

More Detail HGTD-TDR-Chap6

**Requirements:**
- Match timing performance of LGAD
- Small jitter: 25 ps at10 fC, < 70 ps at 4 fC
- Radiation hard




**Status**:
- ALTIROC 0 and ALTIROC 1: analog front end test (C. Agapopoulou et al 2023 JINST 18 P08019)
- ALTIROC 2: first full version with full chain electronics
  - Full size ASIC prototype (15x15 readout channels) ~2x2 cm
  - Irradiation tests done on ALTIROC 2
- ALTIROC 3: is under test and preproduction version under design
  - Tests of performance done with LGADs bump-bonded

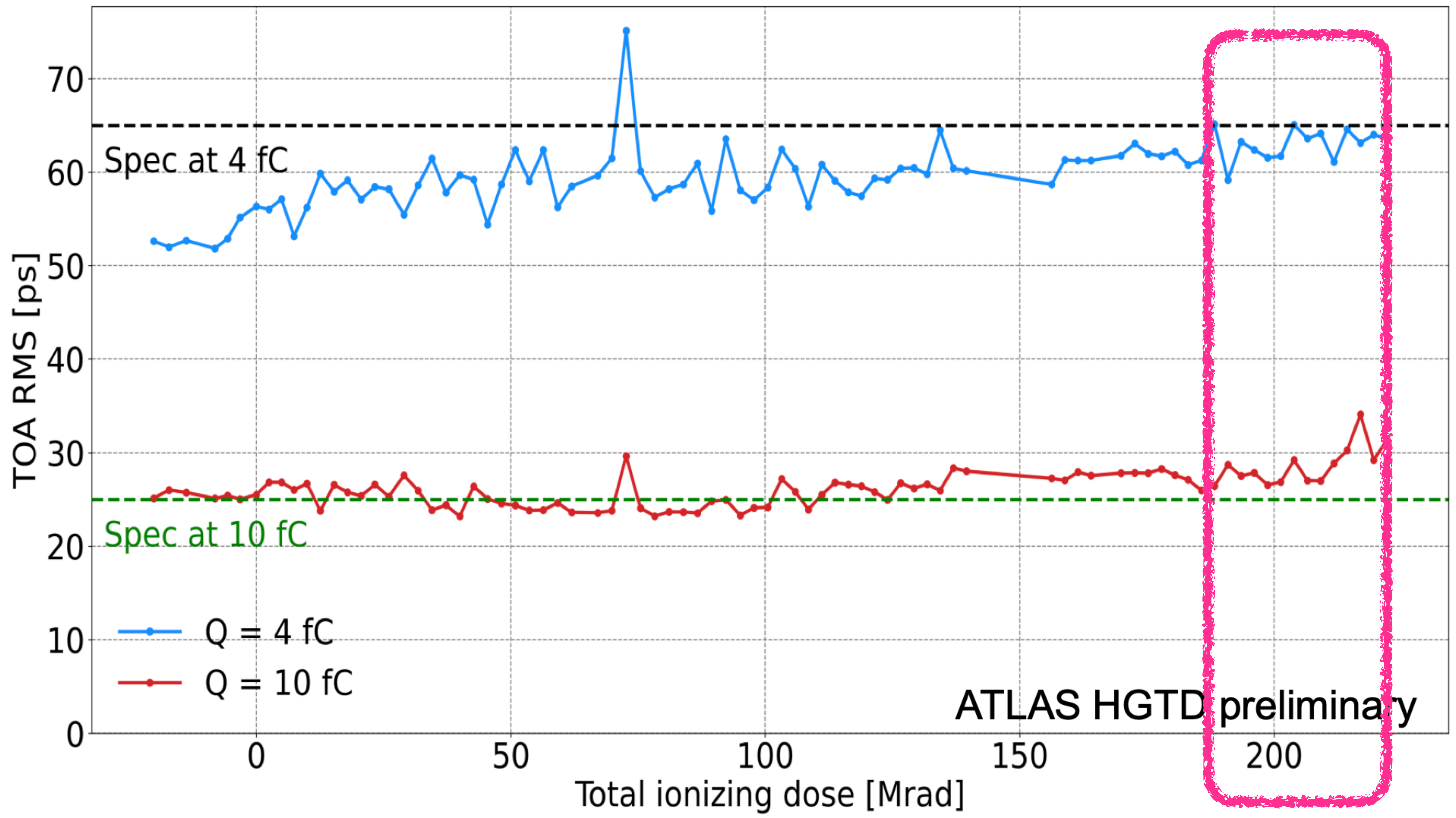
**Analog**:
- Preamplifier + Discriminator + 2TDC

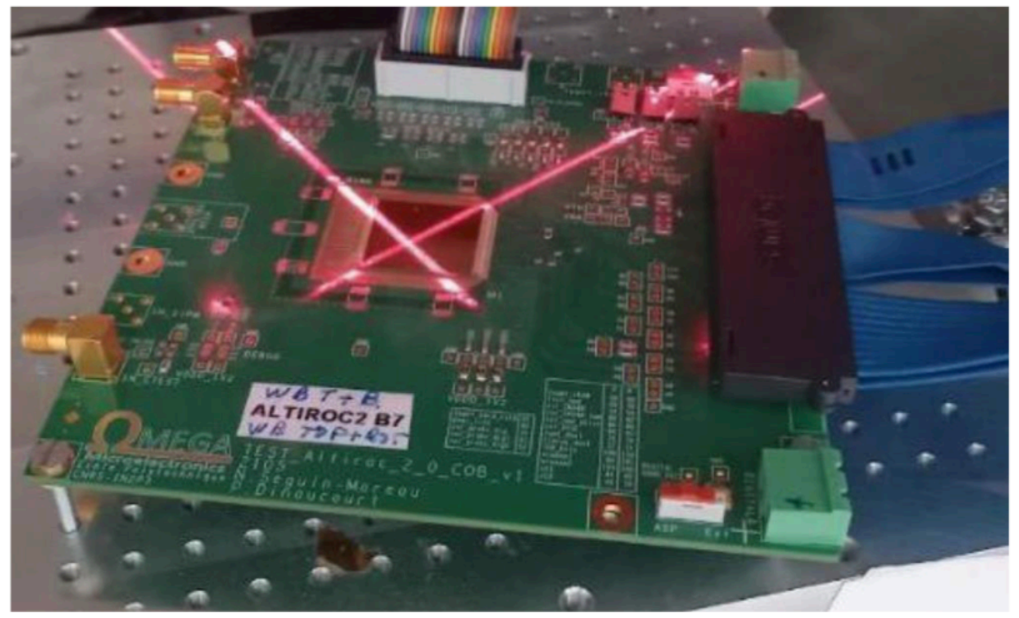
**Digital**:
- Hit buffer, store timing data and hit flag
- Data processed by L0/L1 trigger, allow 35$\mu$s latency
- Luminosity data: sum of hits per bunch crossing

# ASIC: ALTIROC2 performance

More Detail Link

- Tested with and without full size sensor prototype
- Intensive tests prove it to be fully functional
  → thus used for module assembly tests and demonstrator tests
  - **Close to specification as ASIC alone**: meets the specs with one activated column ON at a time
  - **Additional** noise found in ASIC+LGAD assembly
  → Understood:
    - Due to parasitic inductances separating sensor/preamp grounds.
    - Noise get amplified 10 times more than ASIC alone
    - **Close to spec** 2.6 fC min. threshold **achieved**
- Radiation influence studied
- Jitter stays stable with the increasing Total ionising does (TID)

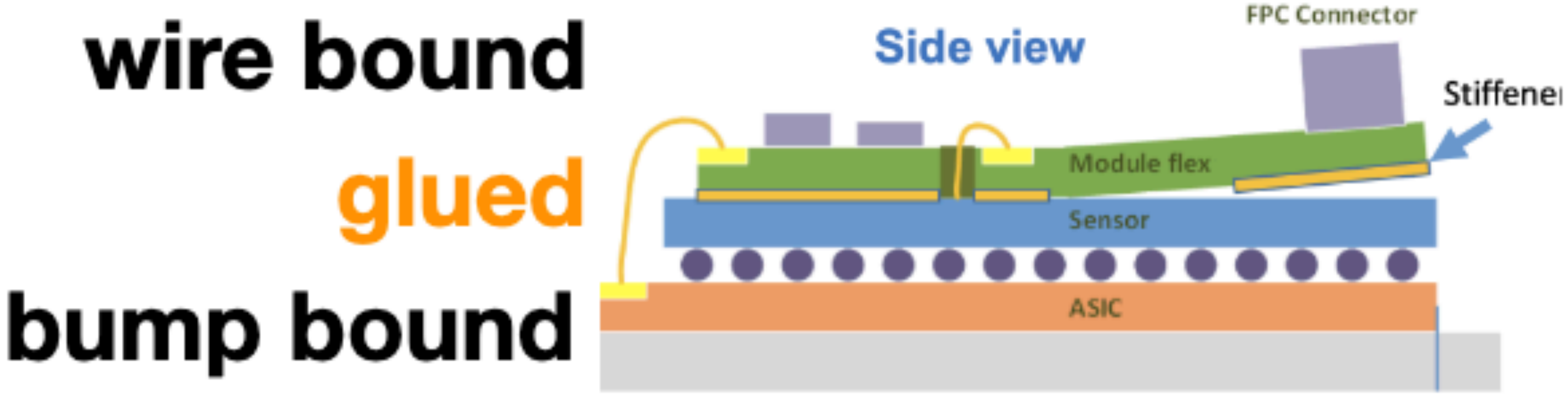


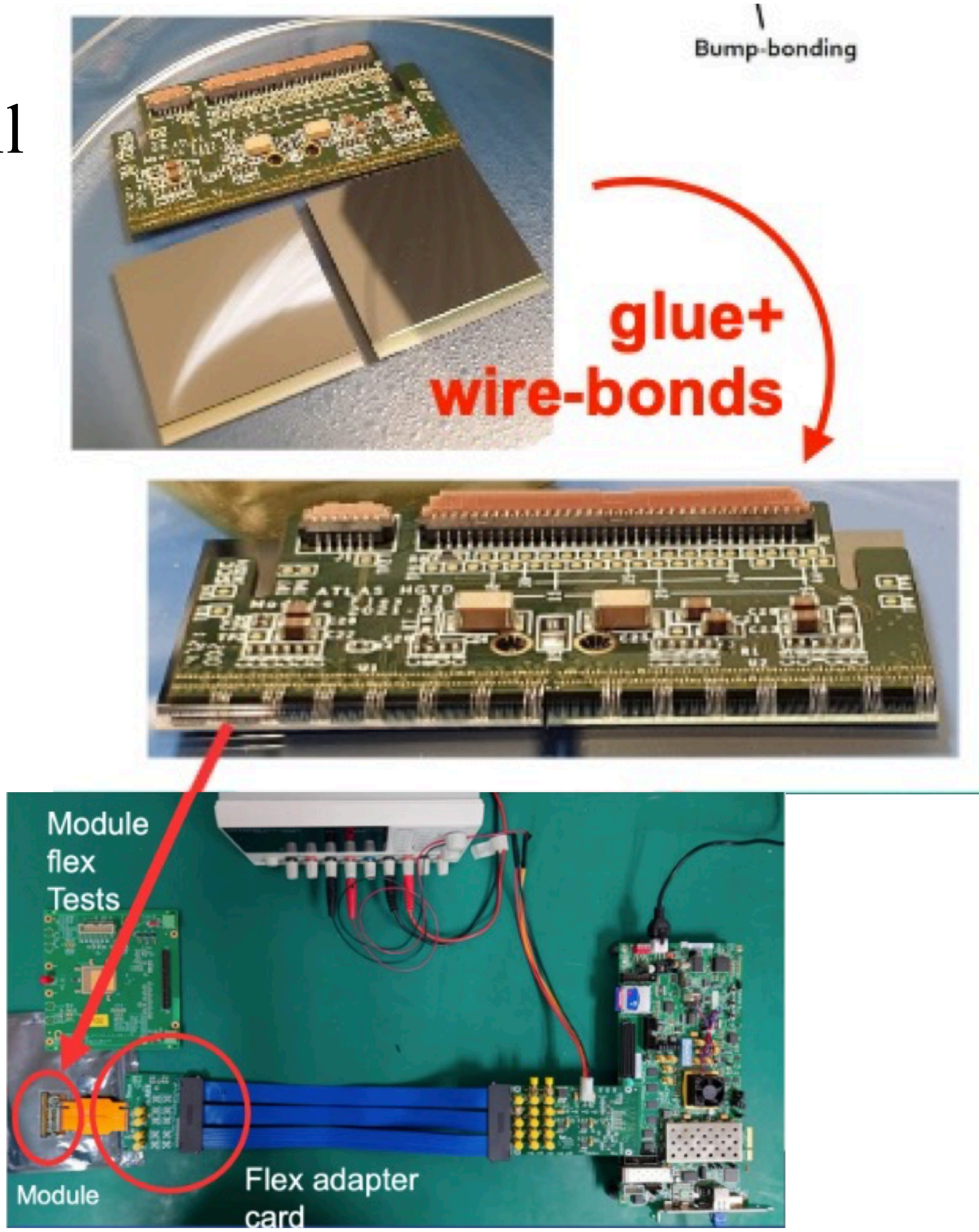



TID : 220 Mrad
Dose rate : 3 Mrad/h
Temperature : 22°C

# Module Assembly

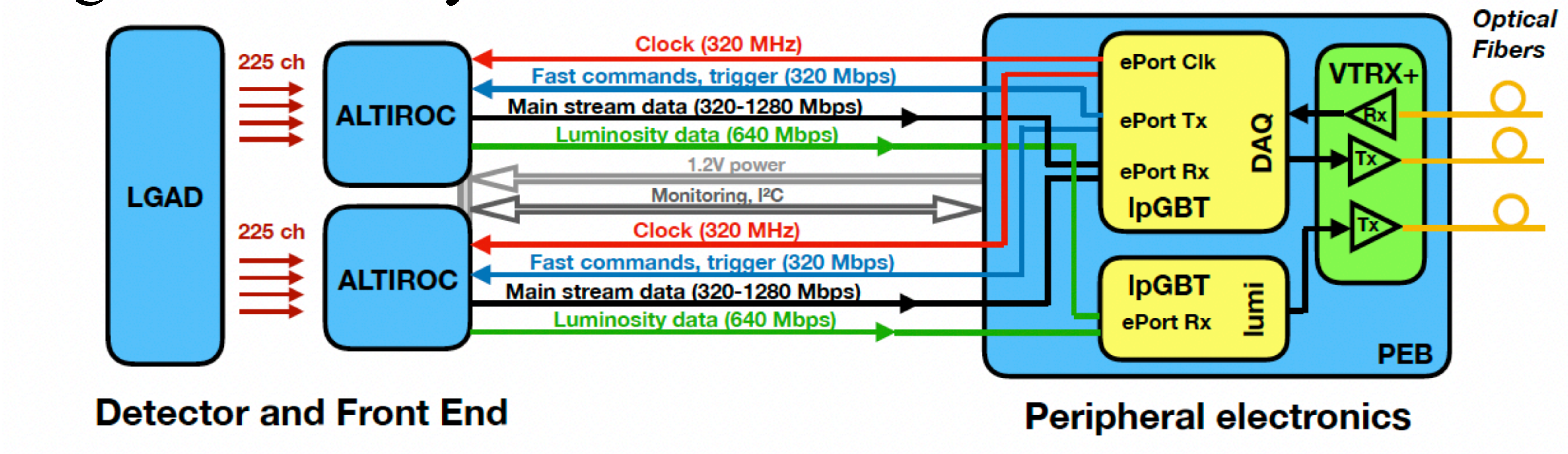
- Module = 2 Hybrid (LGAD + ASIC) + Module FLEX (flexible PCB)
- Flexible PCB connect to peripheral electronics(PEB) through FLEX tail
- HGTD will be composed of 8032 modules (3.6 M channels)



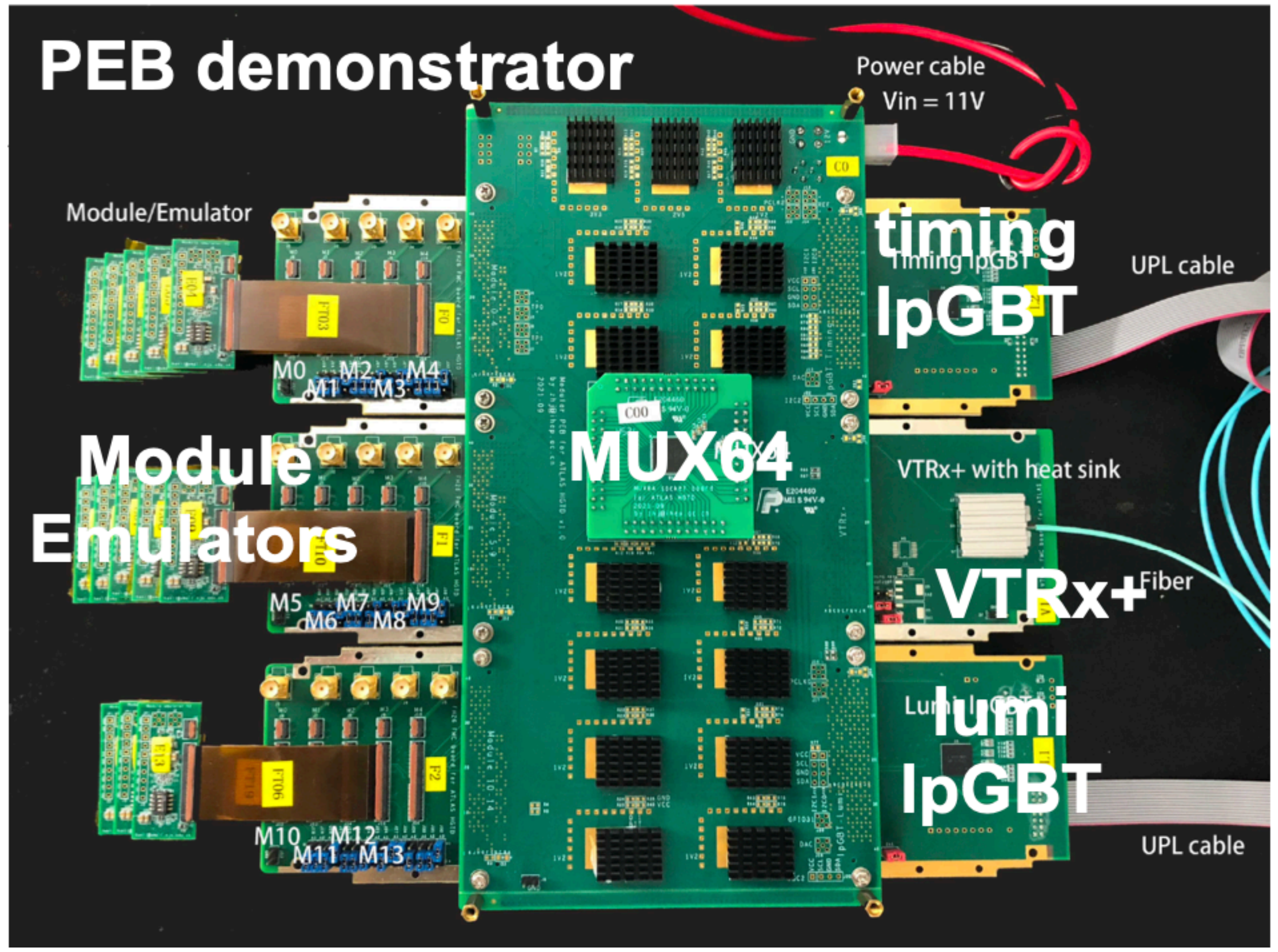



# Peripheral Electronics Board

- Peripheral Electronic Boards (PEB) are integral components of the overall detector system.
- They play a crucial role in managing data transmission, power distribution, control, and monitoring within the system.




More Detail HGTD-TDR-Chap9

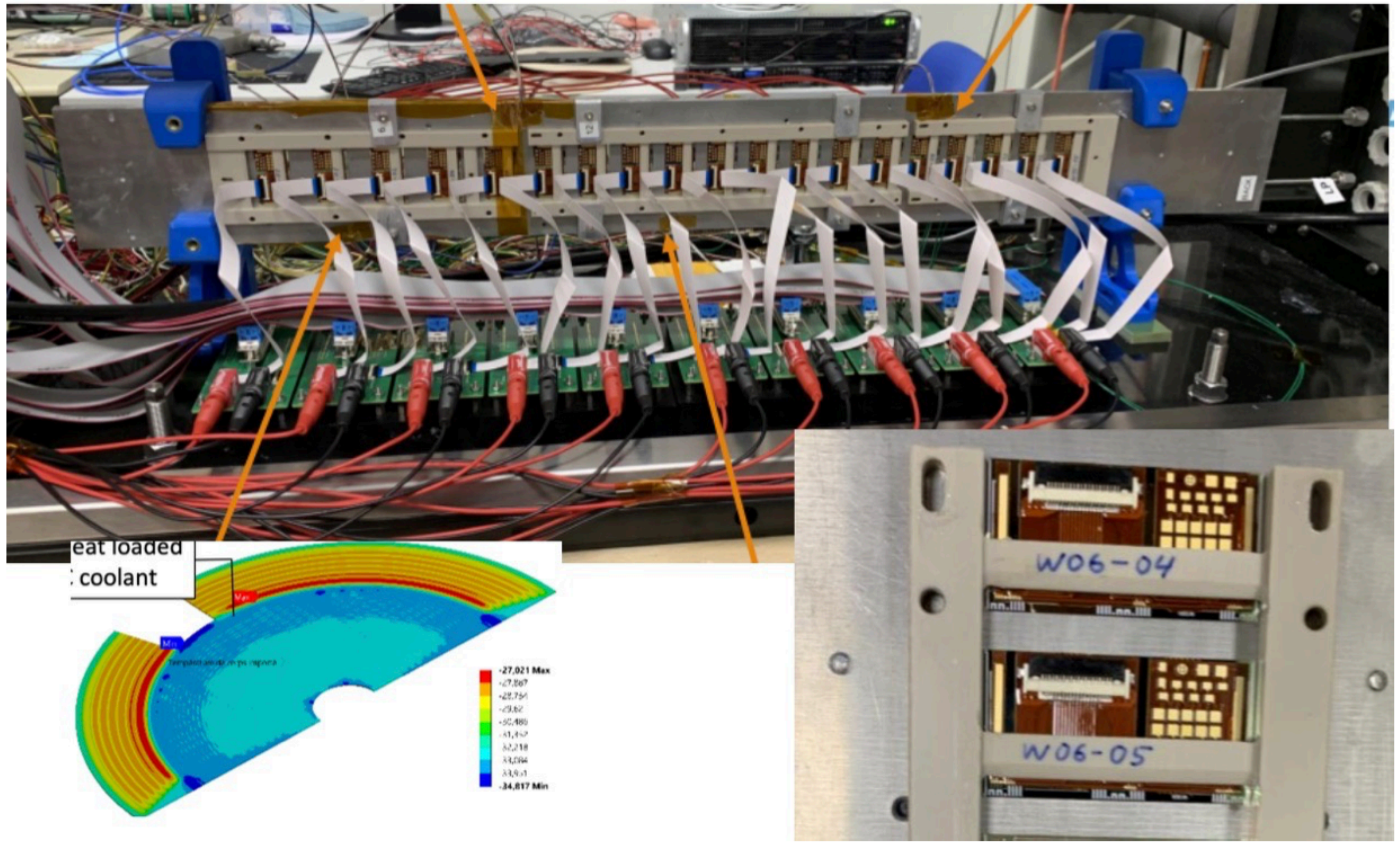


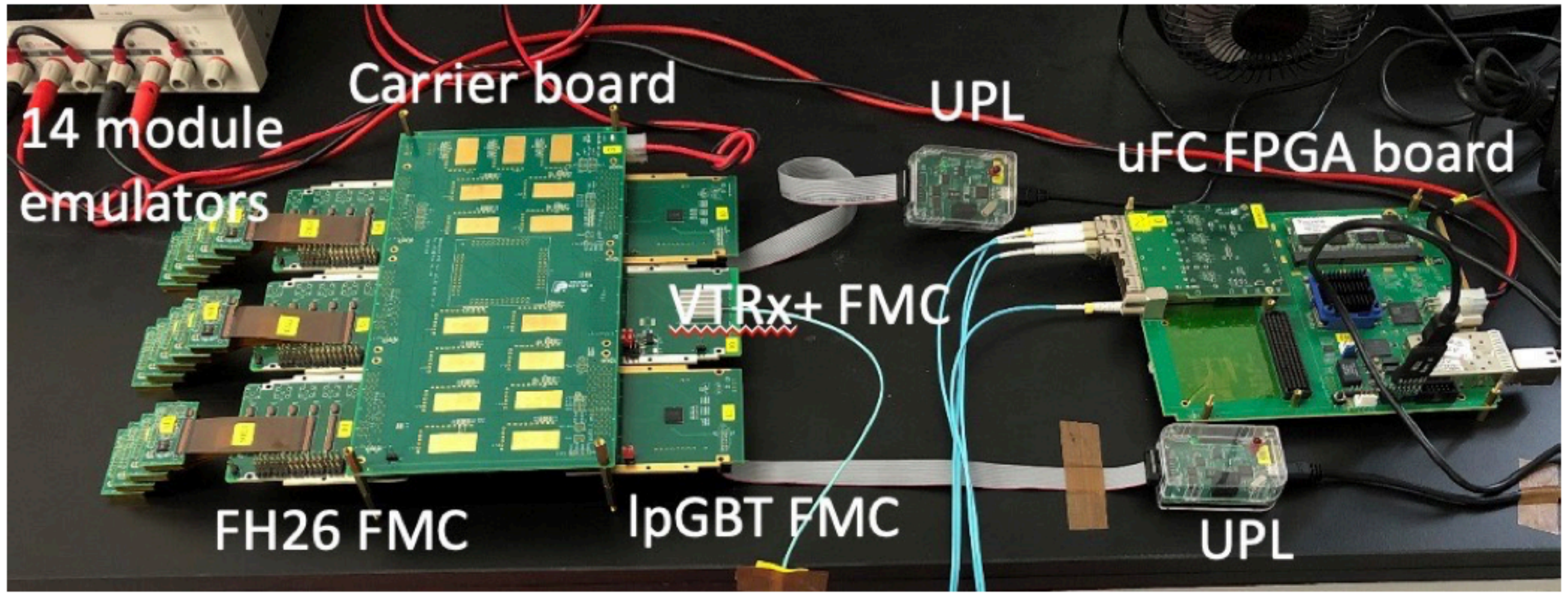

- Intensive work on characterising all individual components on its prototypes
  - DC-DC converter PointOf Load regulators (bPOL) 12V-in depth investigated regarding space constraints, power efficiency
  - Intense tests communications via lpGBT with the FELIX readout card
  - MUX64: analogue multiplexer (for monitoring ASIC power supply and temperature)

# Demonstrator

**Heater demonstrator**

- Validated the modules dissipating heat on CO2 cooling plate
- Found best thermal media = 2 graphite with thermal grease in between




**DAQ demonstrator**

- Verify the HGTD read-out path to off-detector back-end
- Success communication between FELIX and digital module

# Summary

- **Ultra-Precise Track Time Measurements**:
  - HGTD will offer track time measurements with an exceptional resolution of 30-50 ps in the forward region ($2.4 < \eta < 4$)
  - This high precision promises significant gains in suppressing pile-up tracks and forward jets
  - Enhanced potential for precise object identification emerges as a result
- **Noteworthy Progress and Prospects**:
  - **LGAD Sensor and ALTIROC Readout ASIC Advancements:**
    - Strides have been taken in the development of LGAD sensors and ALTIROC readout ASICs
  - **LGAD Design and Radiation Hardness:**
    - Promising headway in LGAD design to meet stringent radiation hardness criteria
    - Carbon-enriched LGADs exhibit remarkable radiation resilience, reaching up to $2.5 \times 10^{15}\ n_{eq}/cm^2$
  - **ALTIROC2 and Upcoming Milestones**:
    - Successful testing of ALTIROC2, the first full-size prototype, showcasing robust functionality
    - Expectation for ALTIROC3 is currently in test with good preliminary results for ASIC alone, waiting for tests with sensor
- **Stay tuned for the next milestones:**
  - 2023: Critical Elements Transition:
    - 2023 marks the transition of key components (Sensor, ASIC, and PEB) to the pre-production phase
  - 2024: Module and Detector Units Preparation:
    - Pre-production initiation for module and detector units is slated for 2024
  - 2025-2026: Integration Steps:
    - Integration of HGTD-A and HGTD-C vessels, a pivotal phase in the project

# Thanks for the listening

# Backups

# HGTD General Parameters

| | |
|---|---|
| Pseudo-rapidity coverage | $2.4 < \lvert\eta\rvert < 4.0$ |
| Thickness in $z$ | 75 mm (+50 mm moderator) |
| Position of active layers in $z$ | $\pm 3.5$ m |
| Weight per end-cap | 350 kg |
| Radial extension: | |
| Total | $110\,\text{mm} < r < 1000\,\text{mm}$ |
| Active area | $120\,\text{mm} < r < 640\,\text{mm}$ |
| Pad size | $1.3\,\text{mm} \times 1.3\,\text{mm}$ |
| Active sensor thickness | 50 µm |
| Number of channels | 3.6 M |
| Active area | $6.4\,\text{m}^2$ |
| Module size | 30 x 15 pads (4 cm × 2 cm) |
| Modules | 8032 |
| Collected charge per hit | $> 4.0$ fC |
| Average number of hits per track | |
| $2.4 < \lvert\eta\rvert < 2.7$ $(640\,\text{mm} > r > 470\,\text{mm})$ | $\approx 2.0$ |
| $2.7 < \lvert\eta\rvert < 3.5$ $(470\,\text{mm} > r > 230\,\text{mm})$ | $\approx 2.4$ |
| $3.5 < \lvert\eta\rvert < 4.0$ $(230\,\text{mm} > r > 120\,\text{mm})$ | $\approx 2.6$ |
| Average time resolution per hit (start and end of operational lifetime) | |
| $2.4 < \lvert\eta\rvert < 4.0$ | $\approx$ 35 ps (start), $\approx$ 70 ps (end) |
| Average time resolution per track (start and end of operational lifetime) | $\approx$ 30 ps (start), $\approx$ 50 ps (end) |

Main parameters of the HGTD.

# HGTD Bandwidth

- With the baseline ATLAS architecture, the ATLAS detector is read-out with a single Level-0 (L0) trigger at an maximum rate of 1MHz, with a maximum latency of 10 μs
- The time information of the HGTD hit cells will be read out on reception of this L0 trigger signal
- Evolved scheme considered by ATLAS, called L0–L1, the HGTD will be read-out on the reception of a L1 trigger signal with a maximum frequency of 800 kHz and a maximum latency of 35 μs
- Therefore the maximal bandwidth is limited to 1.28 Gbit $s^{-1}$

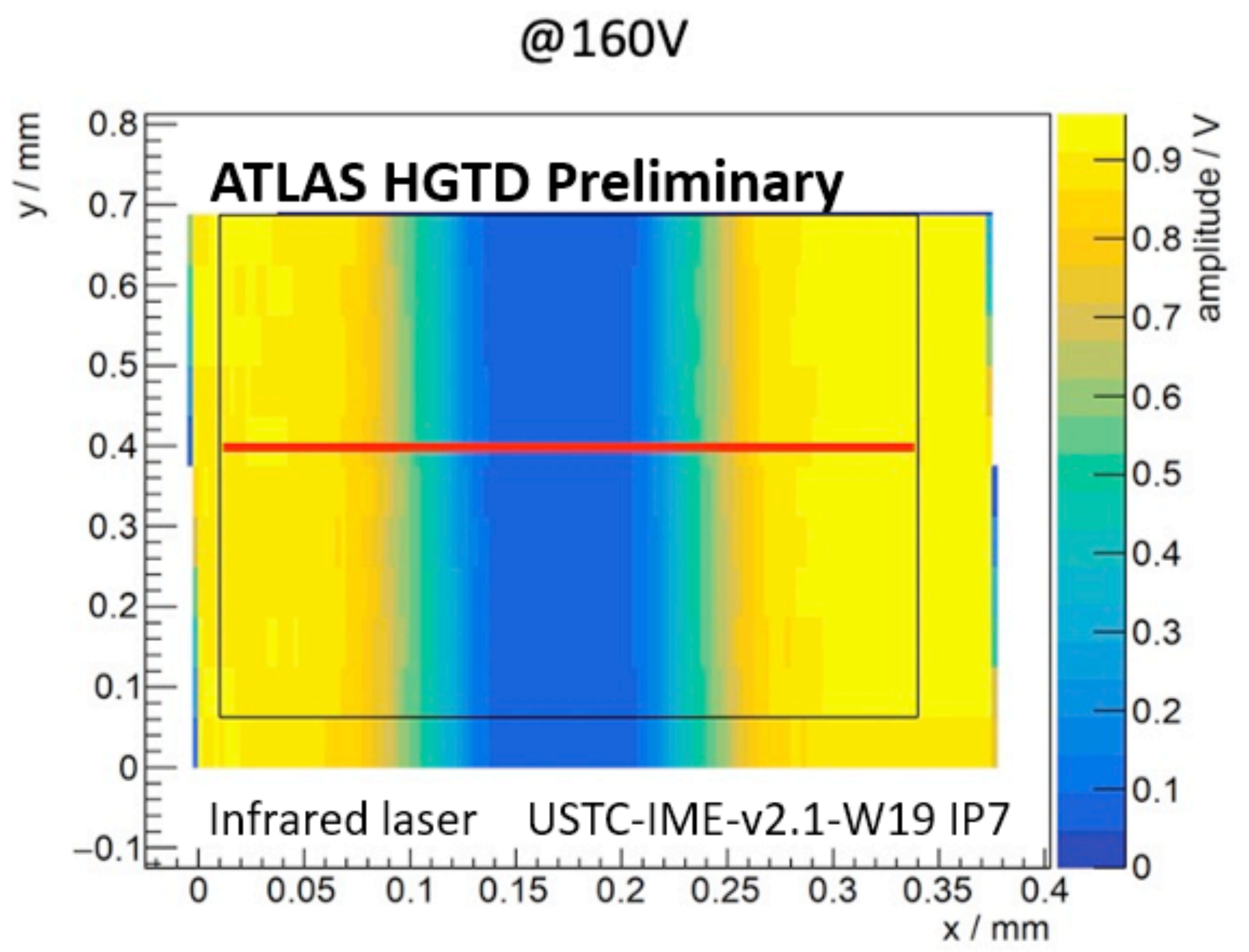
# ALTIROC R&D Roadmap

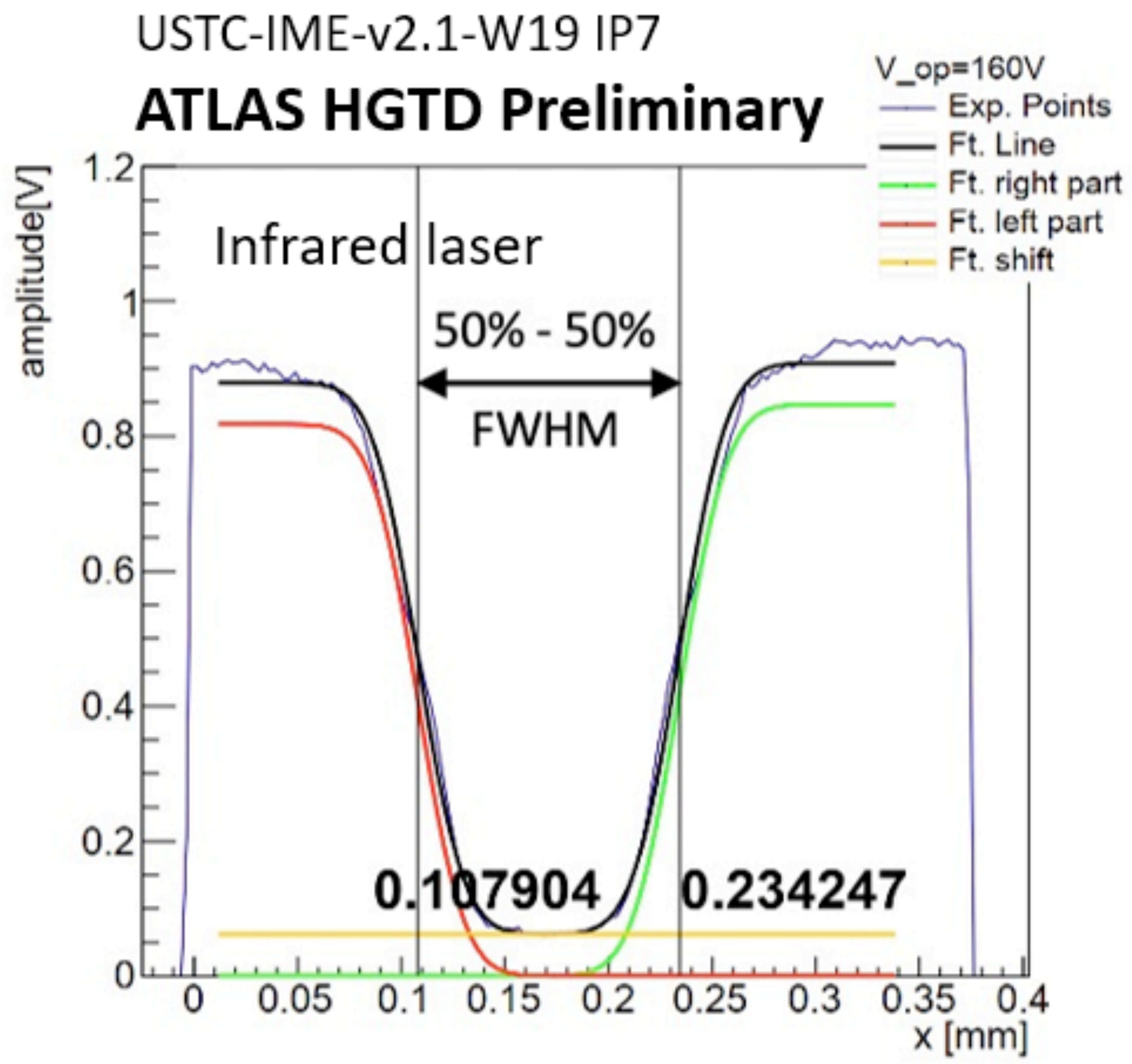
ASICs
Application
Specific
Integrated
Circuits

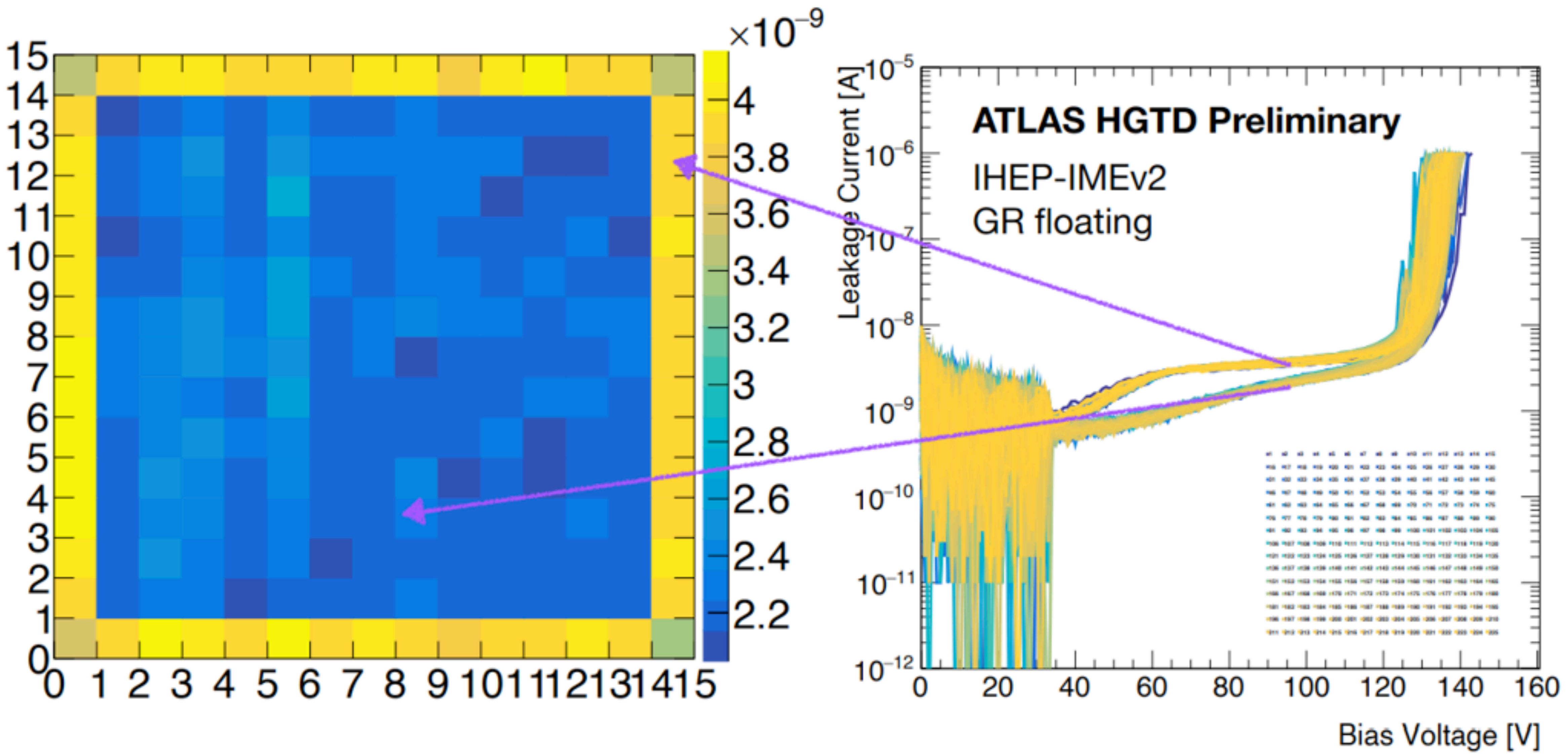
- **ALTIROC0**: version0 ASIC, **preamplifier+discriminator** wave form sampling on the oscilloscope
- **ALTIROC1**:5x5 array with **complete analogue** front end (discriminator, **TOA, TOT**)
- **ALTIROC2**: **first** 15x15 full scale prototype, **first** digital module, with almost complete functionalities
- **New territory in HEP:** first full scale bump-bond able 1GHz front-end store adout 4pFLGAD pixels
- **Maingoal: demonstrate the functionality performance** of the ASI (time resolution + luminosity)

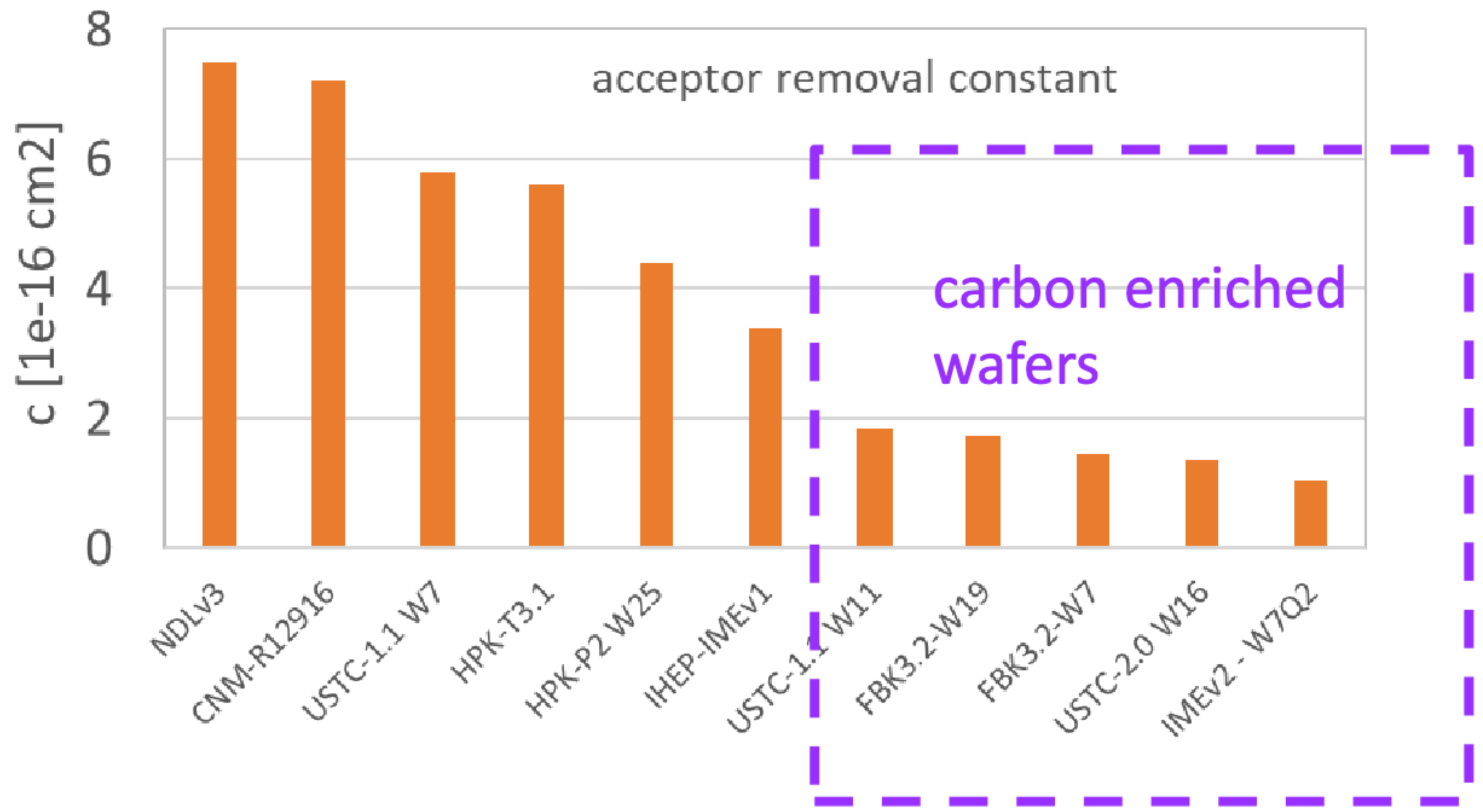
# Study of LGAD performance: Lab

- Studies have been performed to check that prototypes meets the specifications before and after irradiation



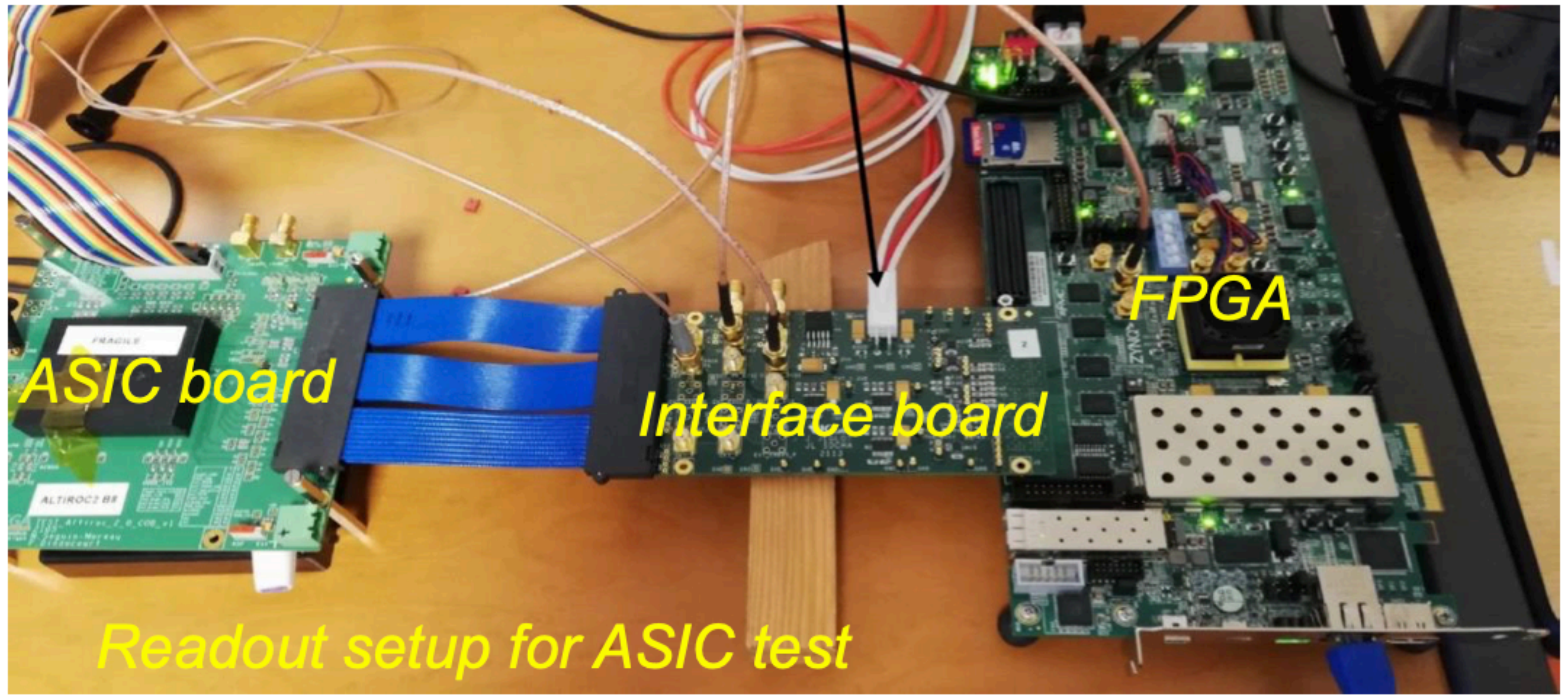



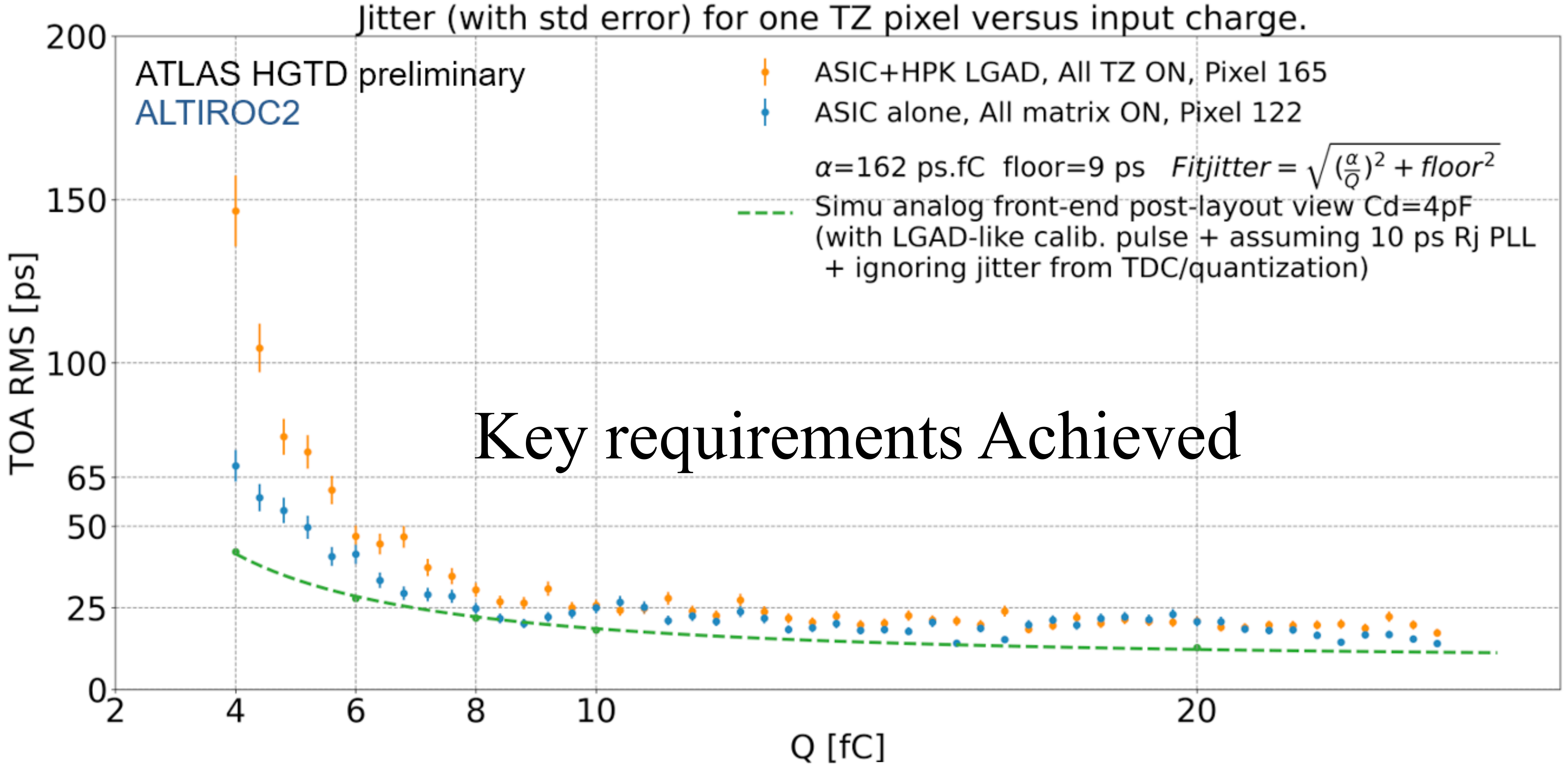

After the irradiation

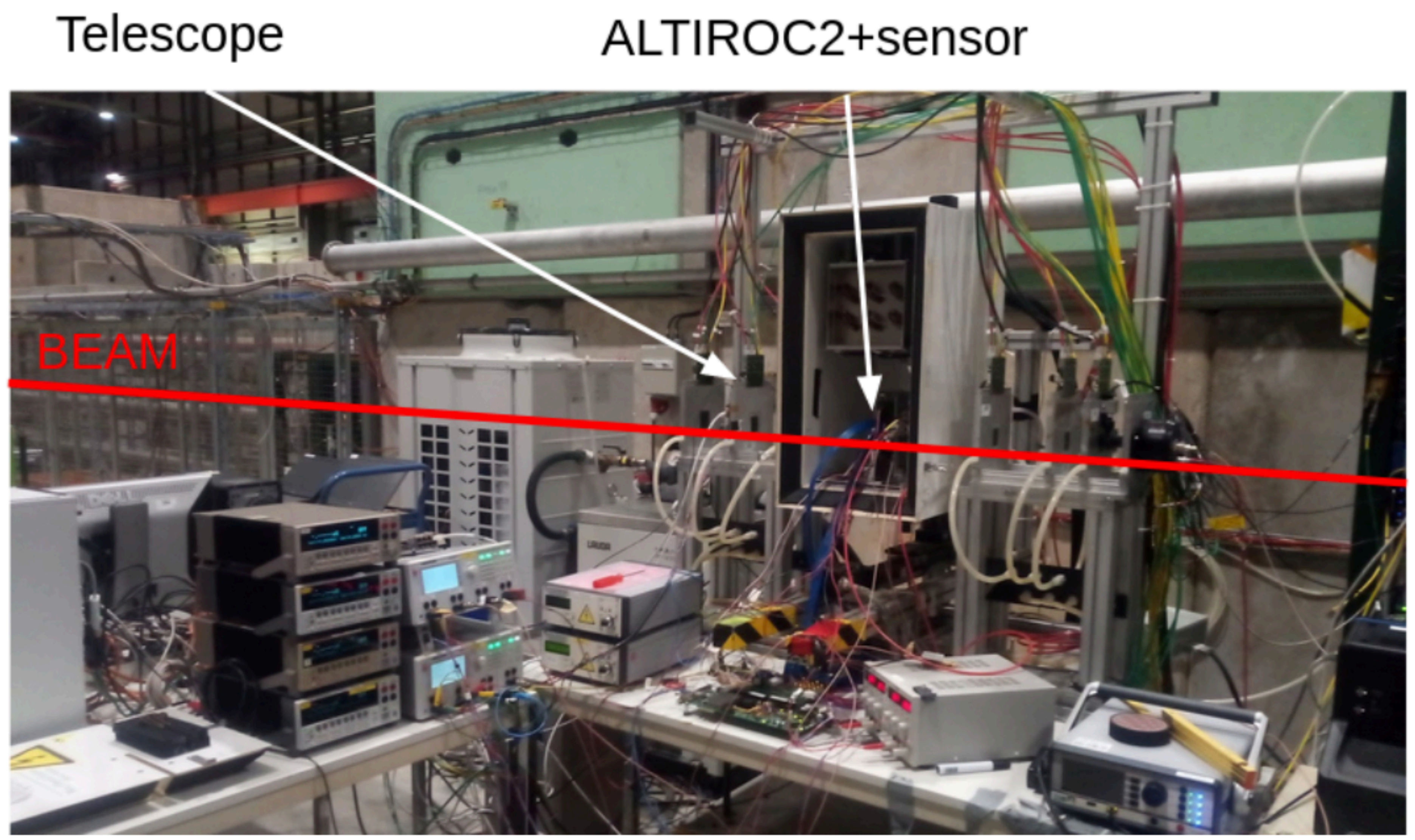
- Boron doping in gain layer became less active (acceptor removal) increase operation voltage to compensate
- Carbon-enriched LGAD shows best radiation hardness

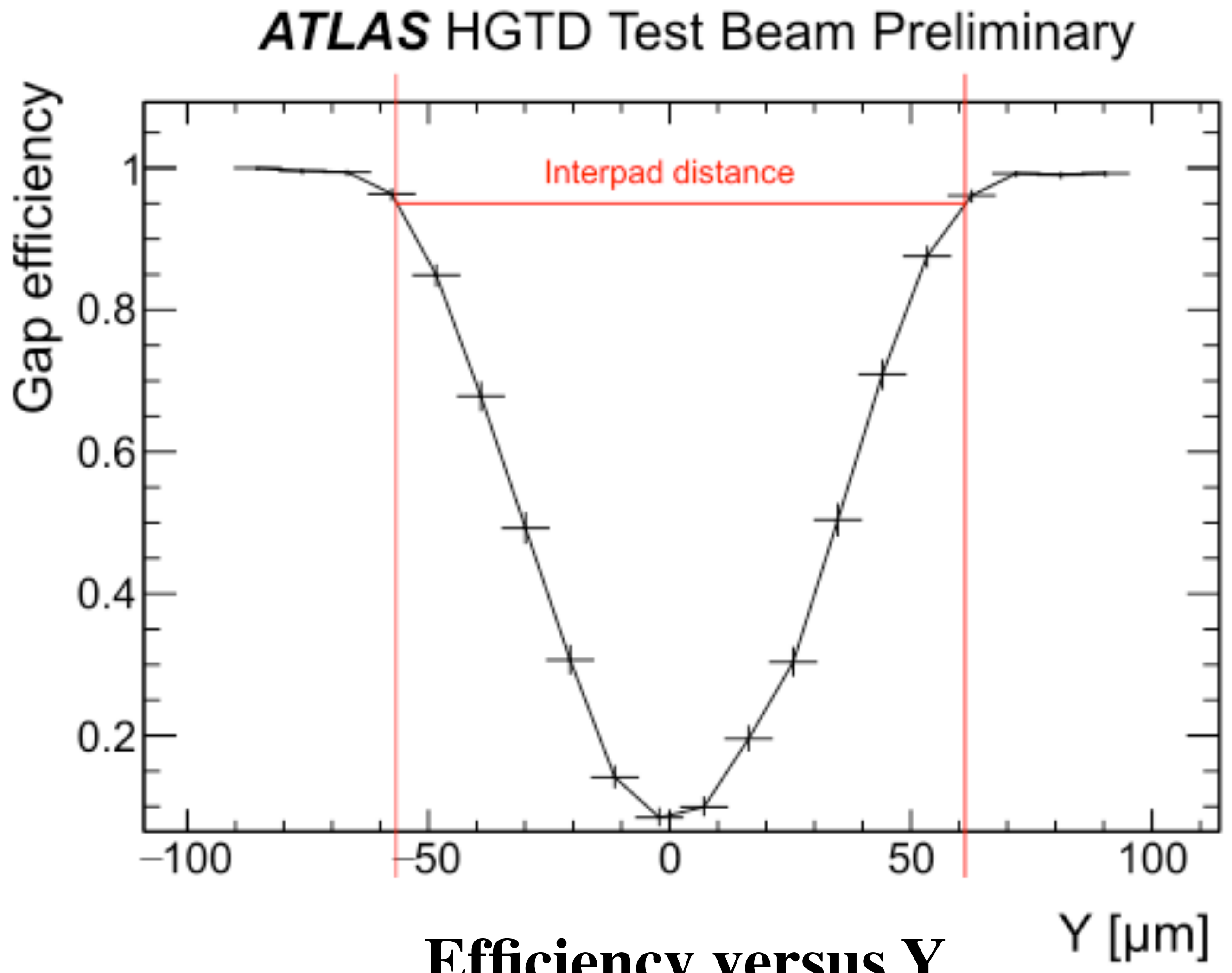
# ASIC: ALTIROC2 performance

**ALTIROC2 test bench: ASIC + interface board +FPGA**

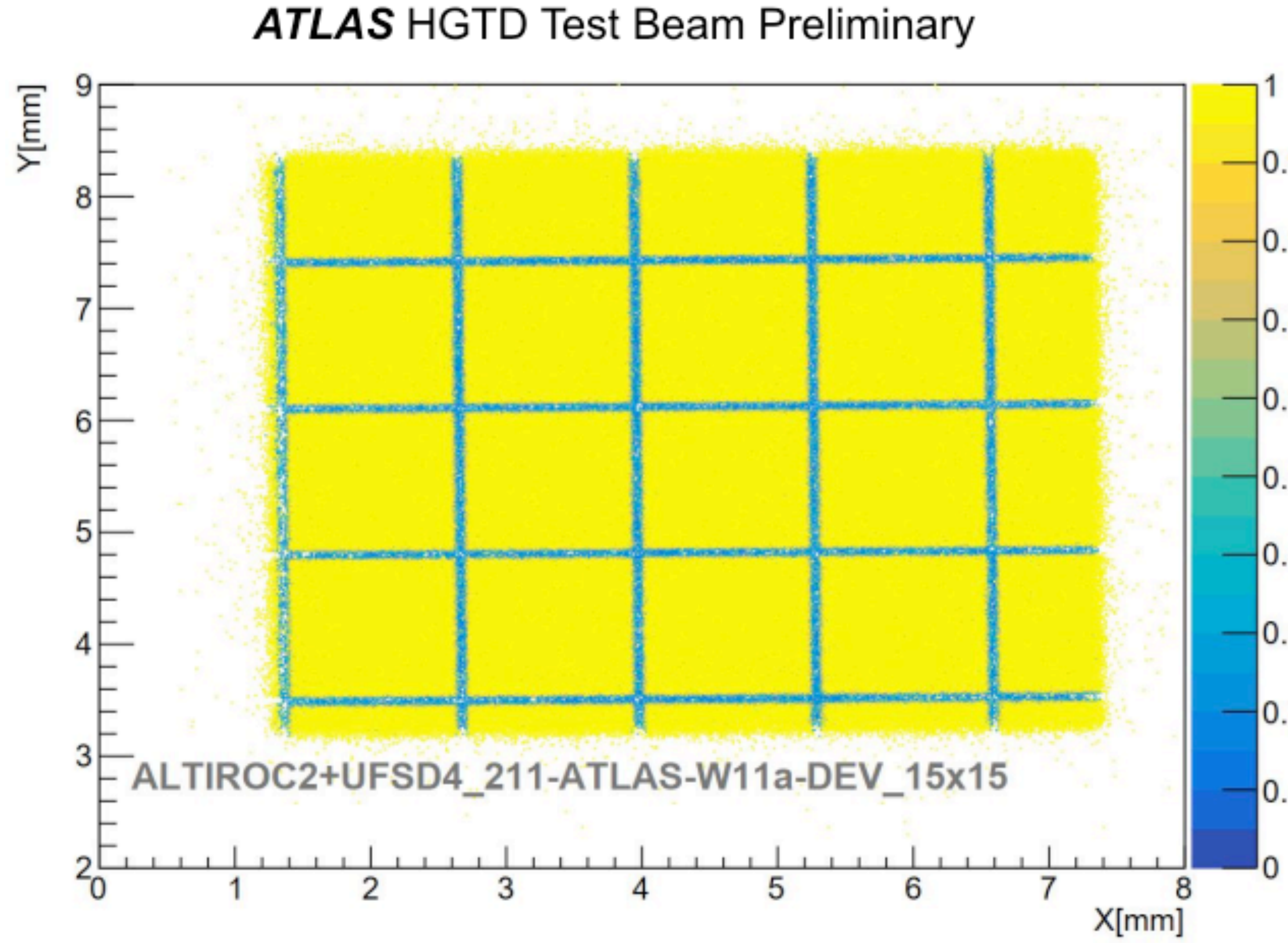



**Efficiency versus Y**

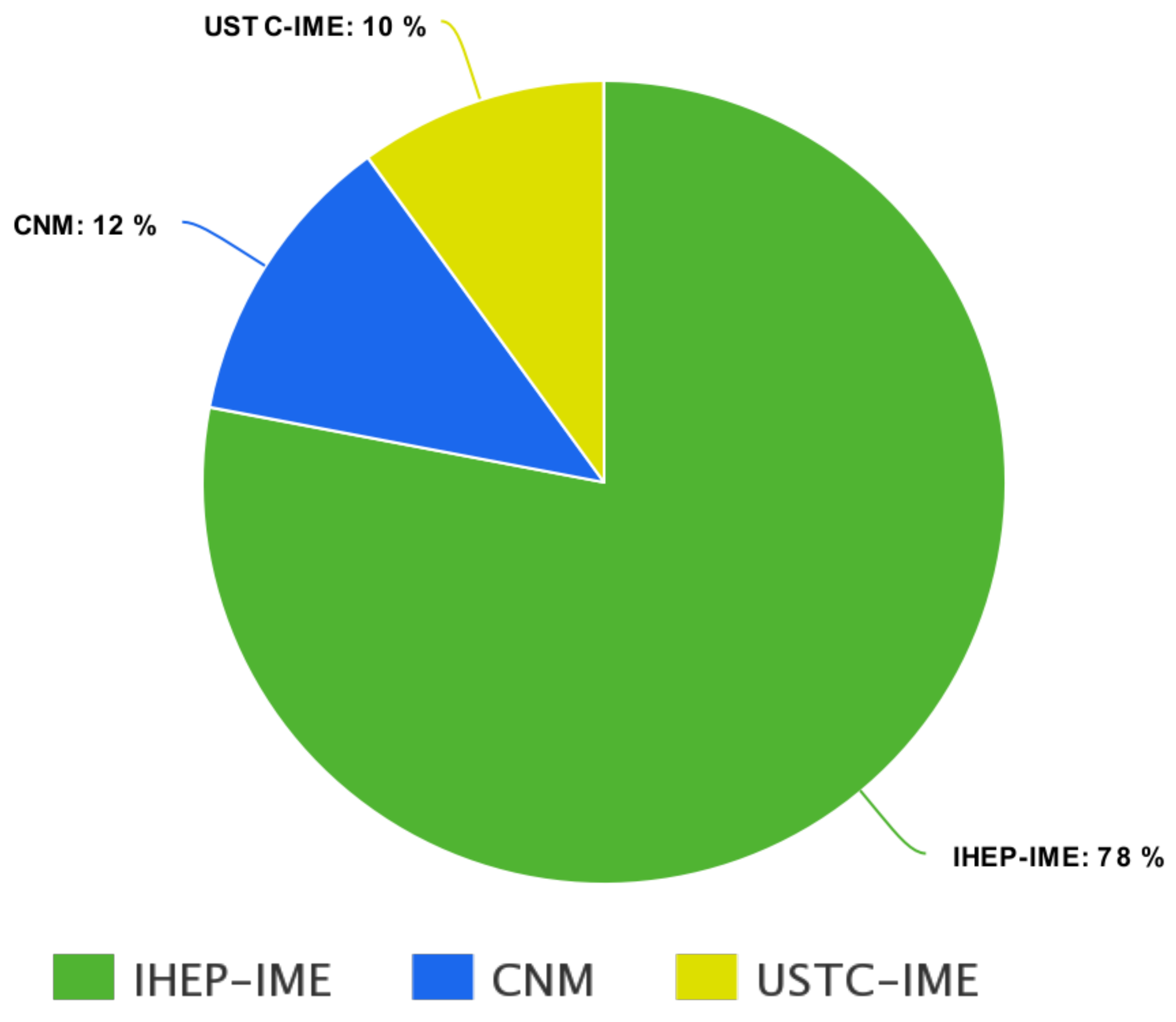



**Efficiency map**

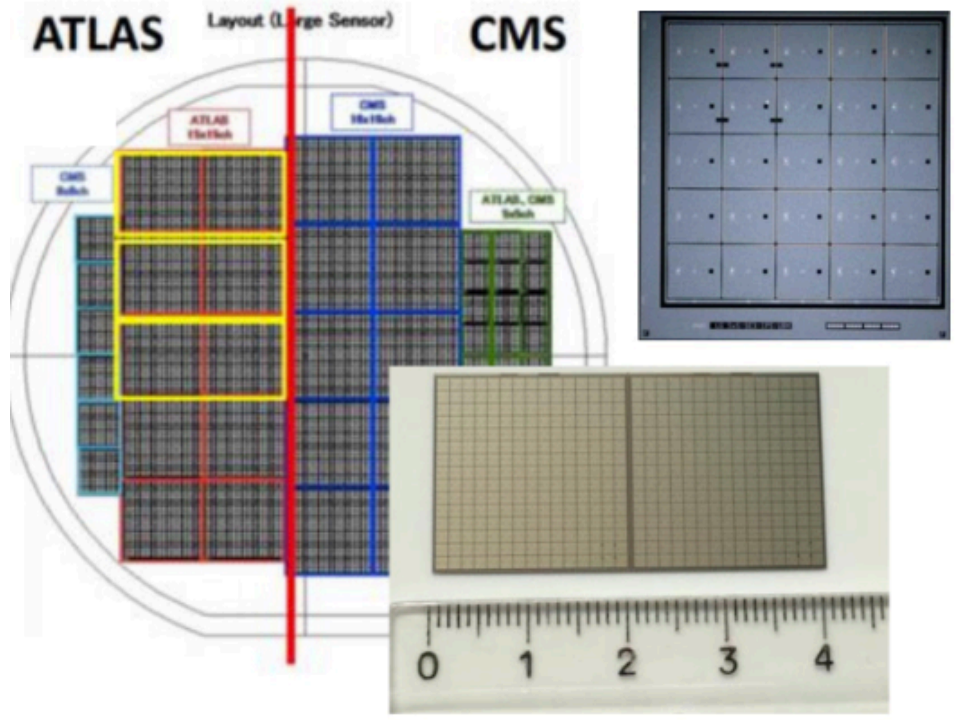
**ALTIROC2+UFSD4_211-ATLAS- W11a-DEV_15x15**

# HGTD LGAD prototypes

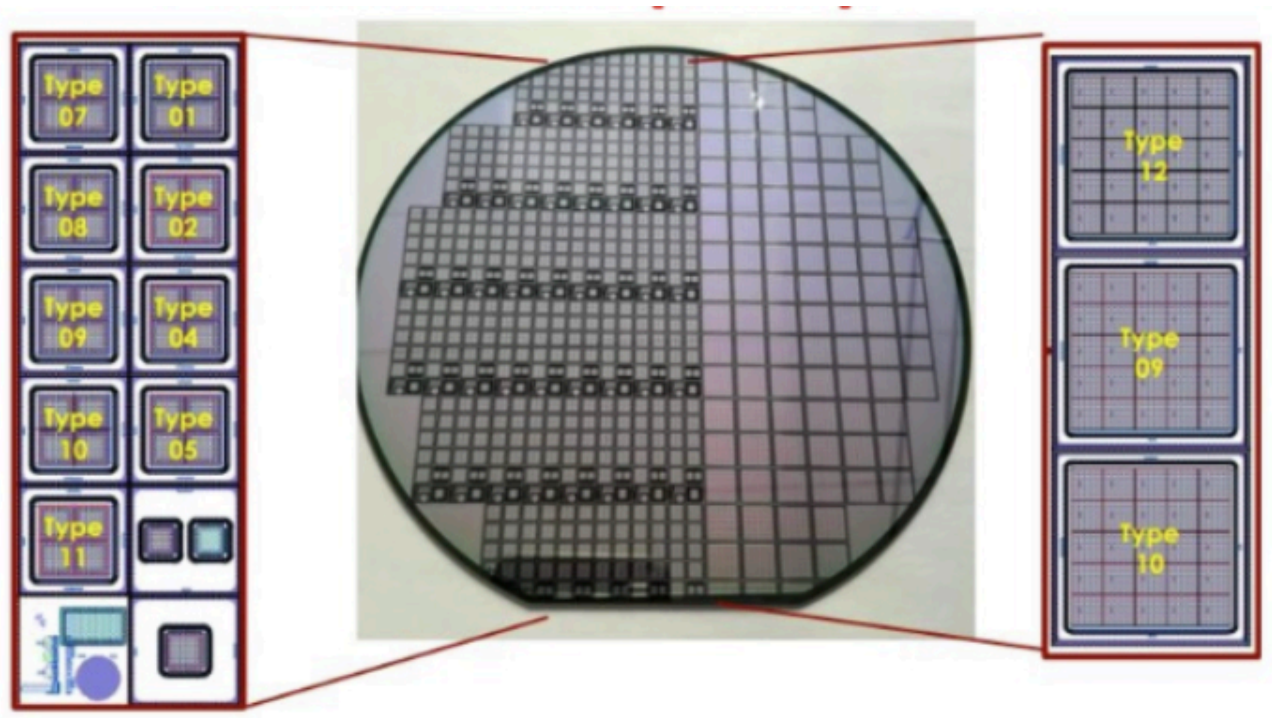
- HGTD LGADs vendors are:
  - IHEP-IME (China), USTC-IME (China), IHEP-NDL (China), FBK (Italy), CNM (Spain), HPK (Japan)



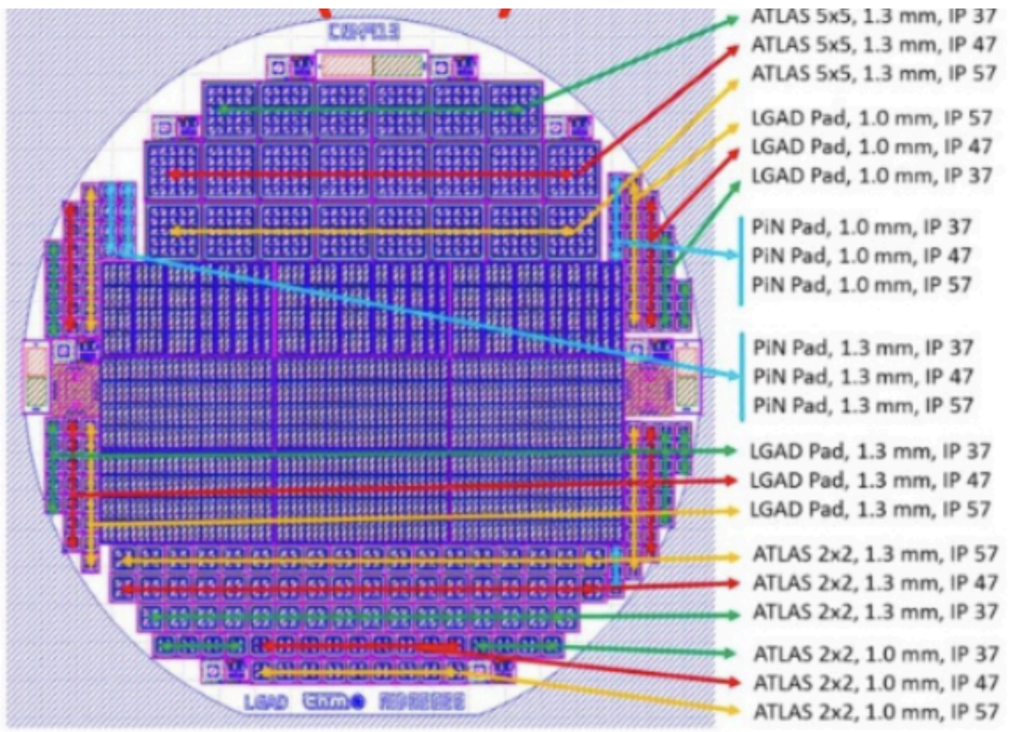

HPK




FBK

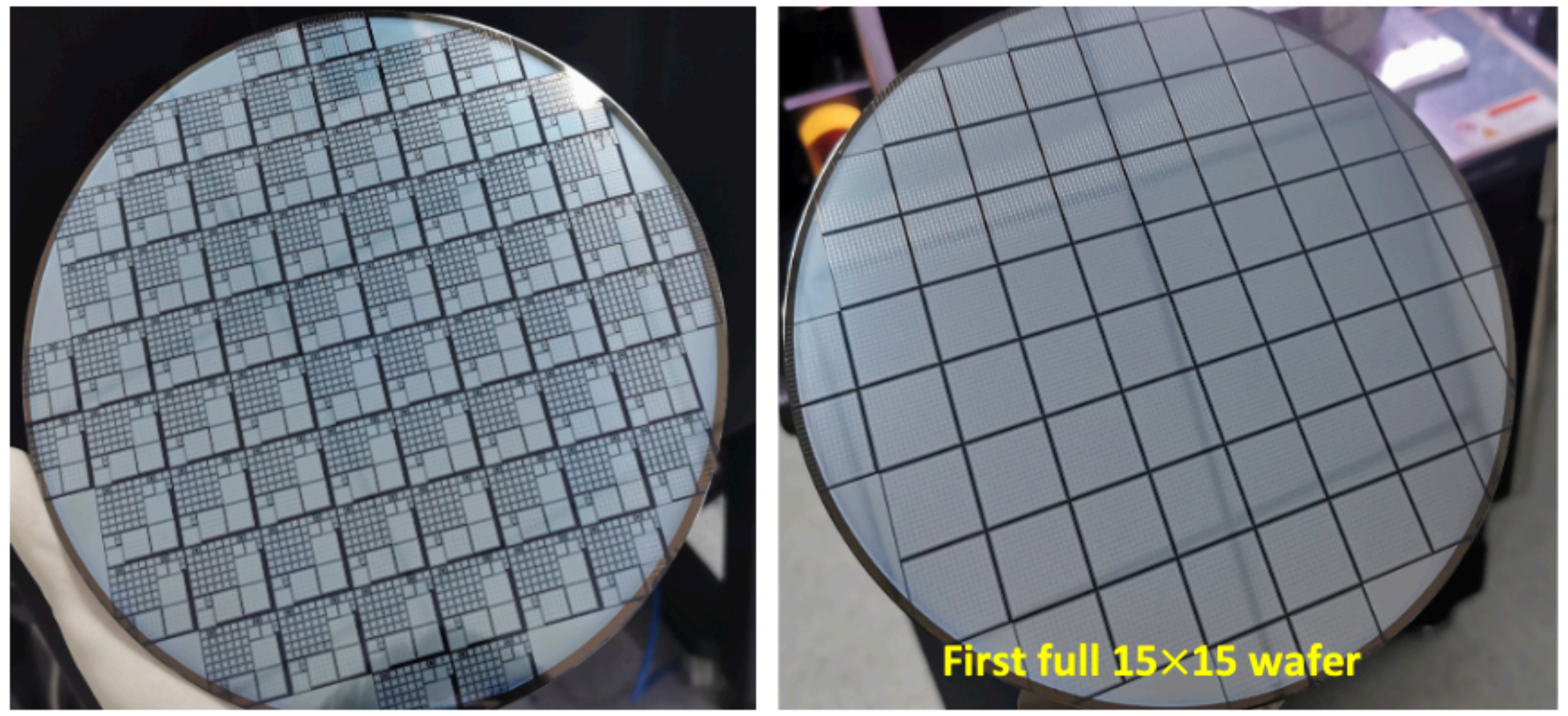


CNM



IHEP-IME


USTC-IME




NDL