环形正负电子对撞机
Circular Electron Positron Collider

Development of CMOS Pixel Sensor prototypes for the CEPC vertex detector

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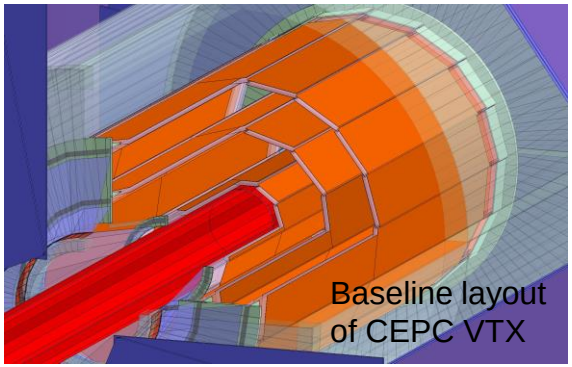
CEPC Vertex detector requirements

The Circular Electron Positron Collider (CEPC) is a large international scientific facility proposed by the Chinese particle physics community in 2012.

- **Efficient tagging of heavy quarks (b/c) and τ leptons**

  ➔ Excellent impact parameter resolution,

$$\sigma_{r\phi} = 5 \oplus \frac{10}{(p \cdot sin^{3/2}\theta)} \ (\mu m)$$



Baseline design parameters for CEPC VTX

	R (mm)	$\lvert z\rvert$ (mm)	$\lvert\cos\theta\rvert$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

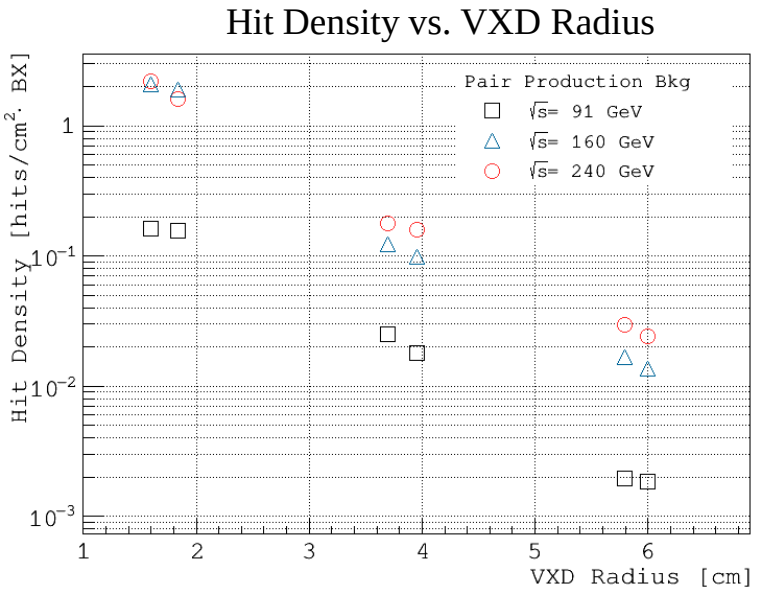
Physics driven requirements → **Running constraints** → **Sensor specifications**

- $\sigma_{s.p.}$ 2.8 μm → Small pixel ***~16 μm***
- Material budget 0.15% X_0/layer → Thinning to ***50 μm***
- Air cooling → low power ***50 mW/cm²***
- r of Inner most layer 16 mm → beam-related background → fast readout ***~1 μs***
- radiation damage → radiation tolerance
  ≤ 3.4 Mrad/ year
  ≤ 6.2×10¹² n_{eq}/ (cm² year)

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector

Main specifications of the full-scale chip

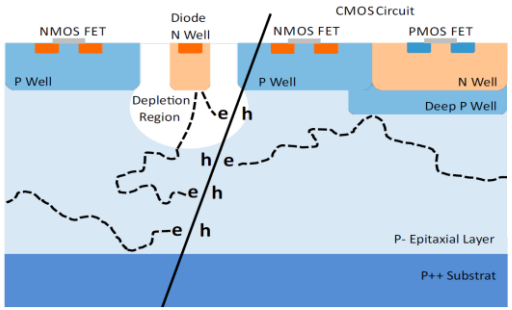
- **Bunch spacing**
  - Higgs: 680 ns; W: 210 ns; Z: **25 ns**
  - Max. bunch rate: 40 M/s
- **Hit density**
  - 2.5 hits/bunch/cm^2 for Higgs/W; 0.2 hits/bunch/cm^2 for Z
- **Cluster size: ~3 pixels/hit**
  - Epi-layer thickness：~18 μm
  - Pixel size：25 μm × 25 μm



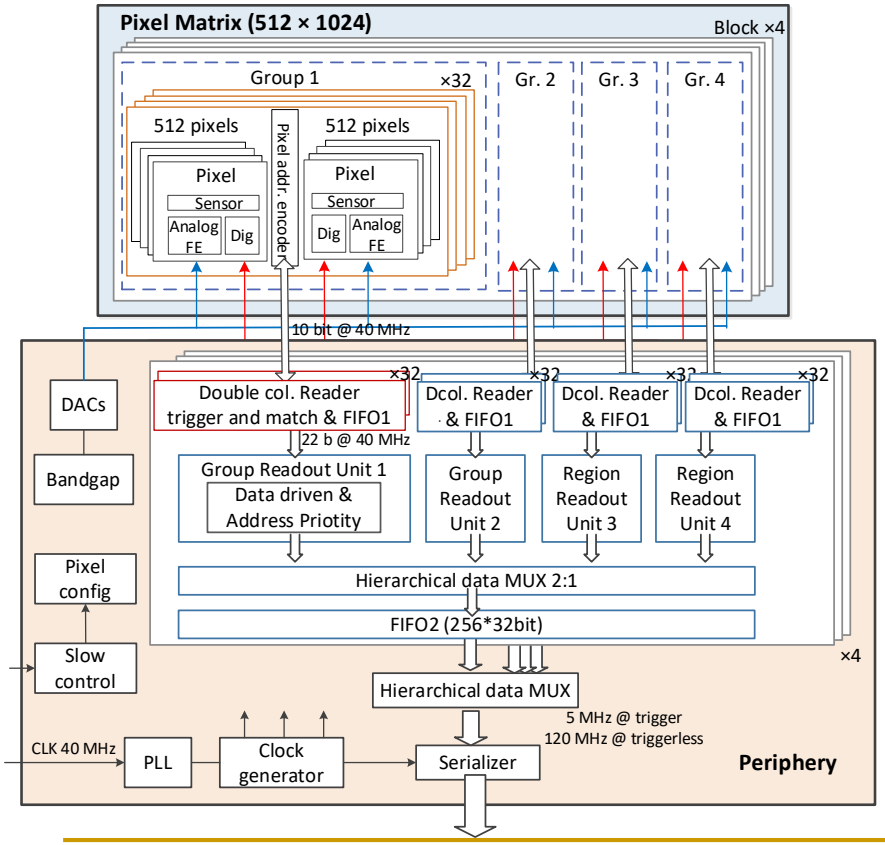
Ref: CEPC Conceptual Design Report, Volume II

For Vertex	Specs	For High rate Vertex	Specs.	For Ladder Prototype	Specs.
Pixel pitch	≤ 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Data rate	**3.84 Gbps** --triggerless **~110 Mbps** --trigger	Power Density	< 200 mW/cm^2 (air cooling)
		Dead time	< 500 ns --for 98% efficiency	Chip size	~1.4 × 2.56 cm^2

TaichuPix sensor architecture



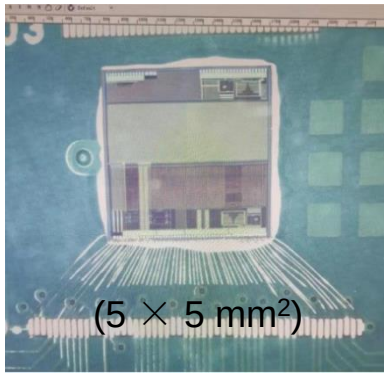
CMOS monolithic pixel sensor



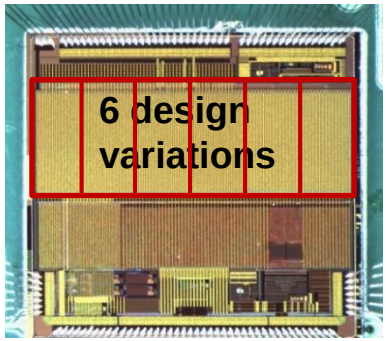
- **Pixel 25 μm × 25 μm**
  - Continuously active front-end, in-pixel discrimination
  - Fast-readout digital, with masking & testing config. logic
- **Column-drain readout for pixel matrix**
  - Priority based data-driven readout
  - Time stamp added at end of column (EOC)
  - Readout time: 50 ns for each pixel
- **2-level FIFO scheme**
  - L1 FIFO: de-randomize the injecting charge
  - L2 FIFO: match the in/out data rate between core and interface
- **Trigger-less & Trigger mode compatible**
  - Trigger-less: 3.84 Gbps data interface
  - Trigger: data coincidence by time stamp, only matched event will be readout
- **Features standalone operation**
  - On-chip bias generation, LDO, slow control, etc.

TaichuPix prototypes overview

- **Motivation: a large-scale & full functionality pixel sensor for the first 6-layer vertex detector prototype**
- **Major challenges for design**
  - Small pixel size → high resolution (3-5 μm)
  - High readout speed (dead time < 500 ns @ 40 MHz) → for CEPC Z pole
  - Radiation tolerance (per year): 1 Mrad TID
- **Completed 3 round of sensor prototyping in a 180 nm CMOS process**
  - Two MPW chips (5 mm × 5 mm)
    - TaichuPix-1: 2019; TaichuPix-2: 2020 → feasibility and functionality verification
  - 1st engineering run
    - Full-scale chip: TaichuPix-3, received in July 2022 & March 2023

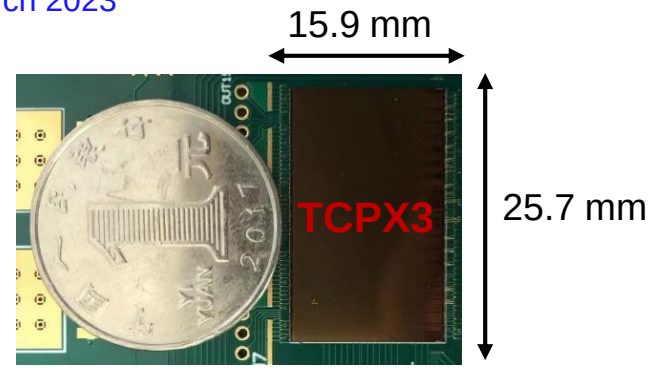


TaichuPix-1



(5 × 5 mm²)

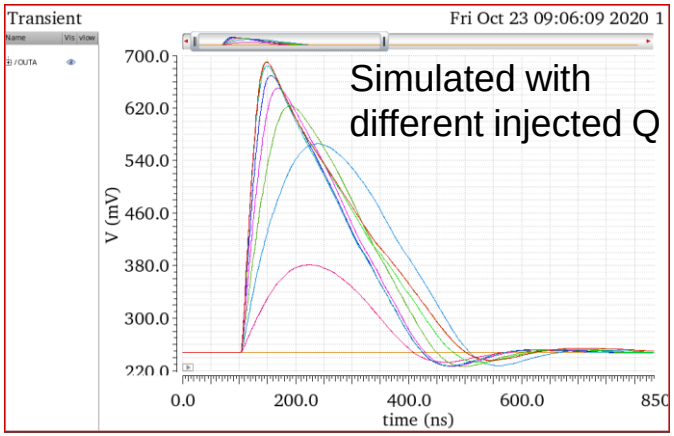
TaichuPix-2

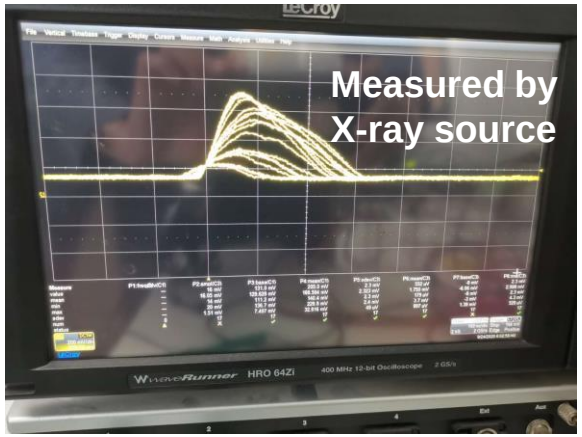


TaichuPix-3
Pixel size：25 μm × 25 μm

Functionality of complete signal chain

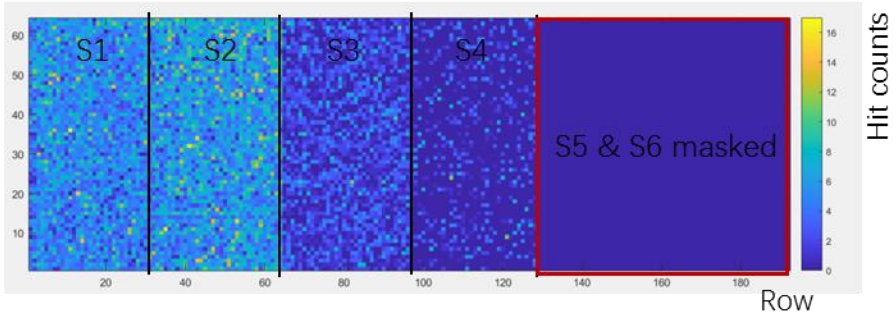
- **Functionality of the complete signal chain (including sensor, analog front-end, in-pixel logic readout, matrix periphery readout and data transmission unit) was firstly proved with X-ray, electron and laser sources.**



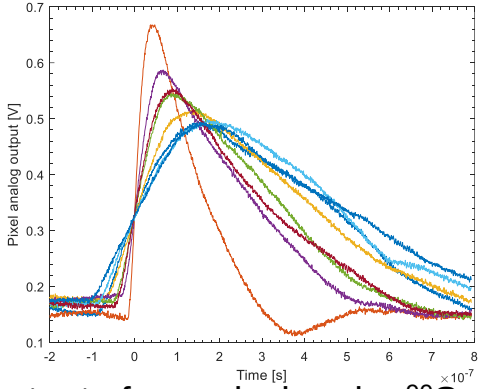


Measured results consistent with simulations in term of shape, amplitude

Pixel analog signals from simulation (left) and measurement (right)



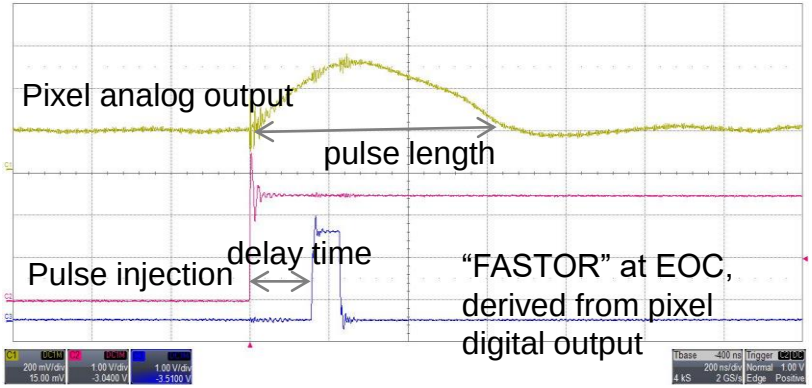
Hit map of the TaichuPix-2 under X-ray from the X-tube for 5 min.

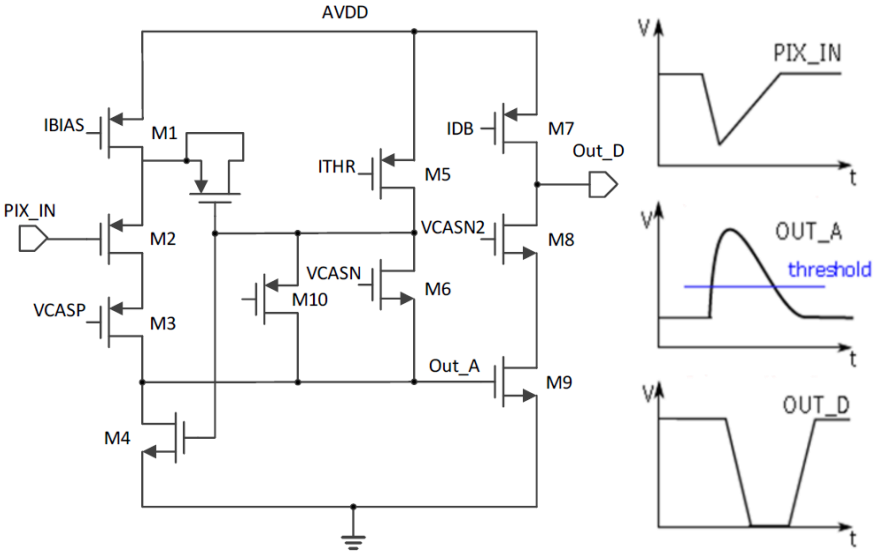


Analog output of one pixel under ^{90}Sr exposure

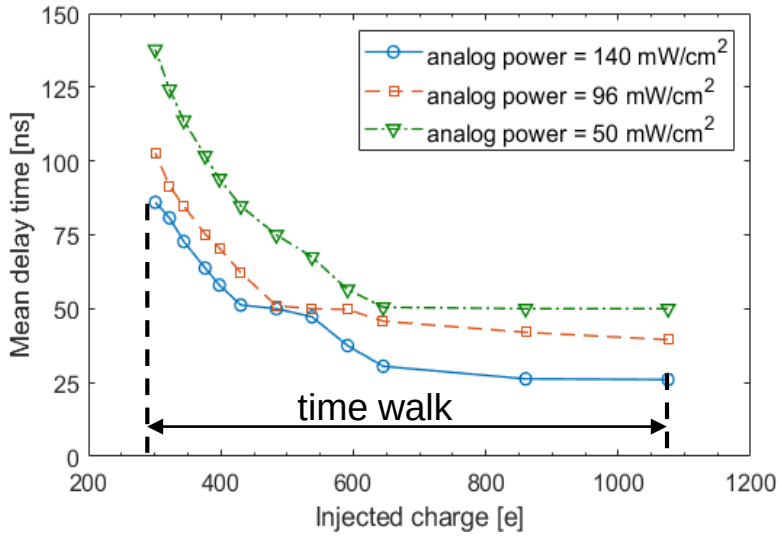
Pixel analog front-end

- **Based on ALPIDE* front-end scheme**
  - modified for faster response
  - ‘FASTOR’ signal delivered to the EOC (end of column) when a pixel fired, timestamps of hit recorded at pos. edge of ‘FASTOR’





Schematic of pixel front-end



Delay time of FASTOR with respect to the pulse injection vs. injected charge. The delay time was measured by the timestamp of a step of 25 ns.

*Ref: D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042

TaichuPix-2 test with ^{90}Sr

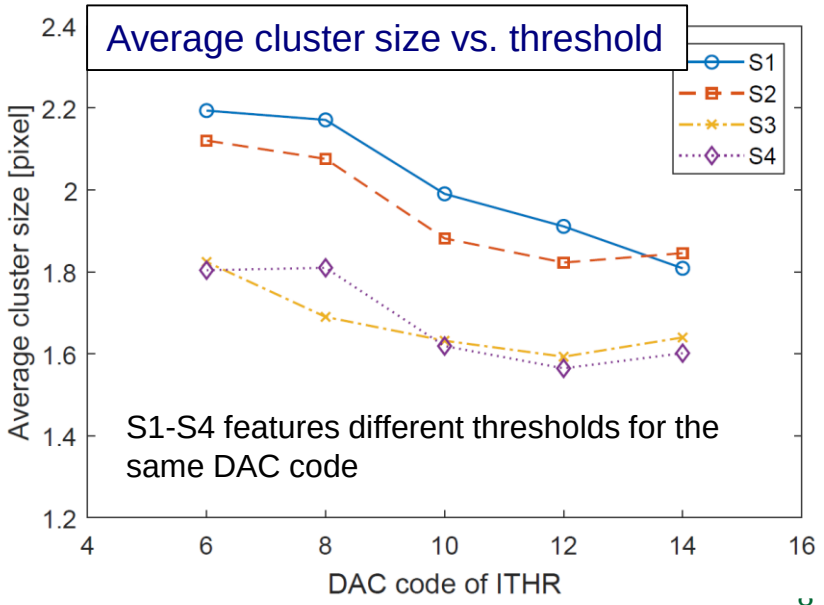
- **Four pixel sectors with different analog front-end variations for design optimization, S1 used in the full-scale chip due to the lowest ENC**

Sectors	Front-end design features
S1	Reference design, inherited from TaichuPix-1
S2	PMOS in independent N-wells
S3	One transistor in an enclosed layout
S4	Increased transistor size to reduce the threshold dispersion

Threshold and noise of different pixel sectors

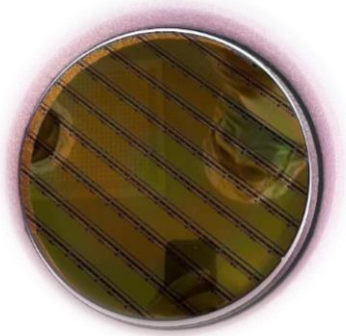
Sectors	Threshold Mean (e^-)	Threshold rms (e^-)	Temporal noise (e^-)	Total equiv. noise (e^-)
S1	**267.0**	**49.8**	**29.3**	**57.8**
S2	293.4	54.5	26.9	60.8
S3	384.9	58.4	24.4	63.3
S4	411.9	56.6	26.5	62.5

- **TC2 exposure to ^{90}Sr source**
  - Average cluster size decreases with threshold as expected
  - Average cluster size for S1-S4 larger than 1, → benefits the spatial resolution (better than the binary resolution, $25/\sqrt{12} \approx 7.2\ \mu m$)

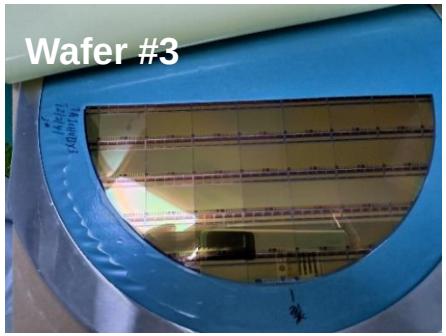


Large-scale sensor TaichuPix-3

- **12 TaichuPix-3 wafers produced from two rounds**
  - **Wafers thinned down to 150 μm and diced**



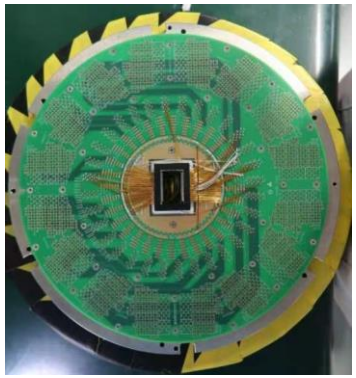
8-inch wafer



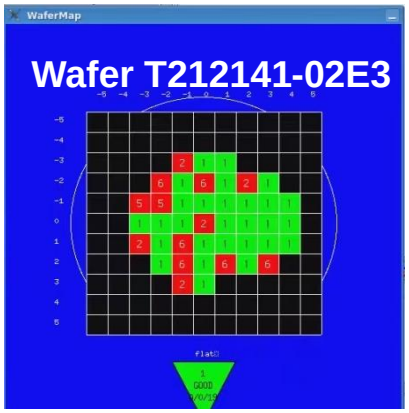
Wafer after thinning and dicing

Thickness after thinning

  - **Wafers tested on probe-station** → chip selecting & yield evaluation



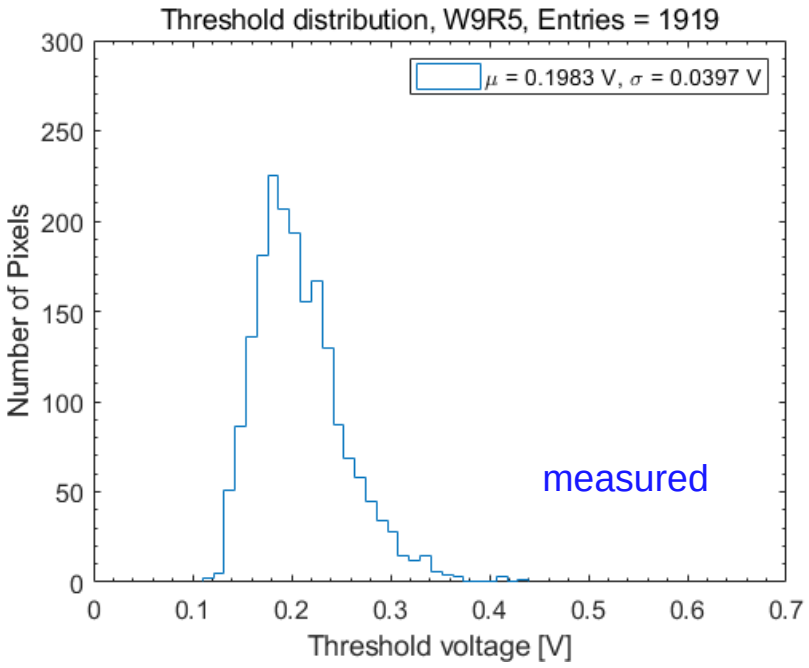
Probe card for wafer test

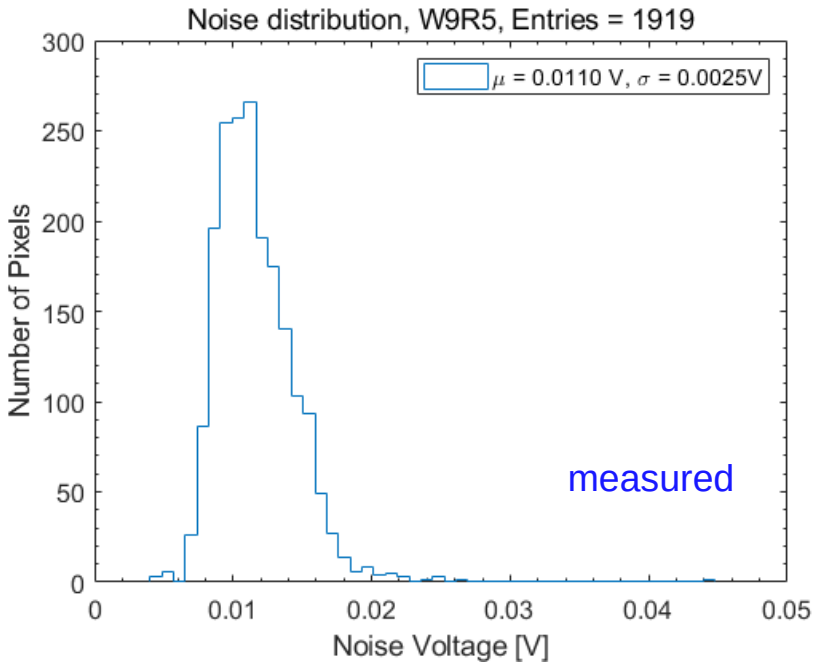


An example of wafer test result

Threshold and noise of TaichuPix-3

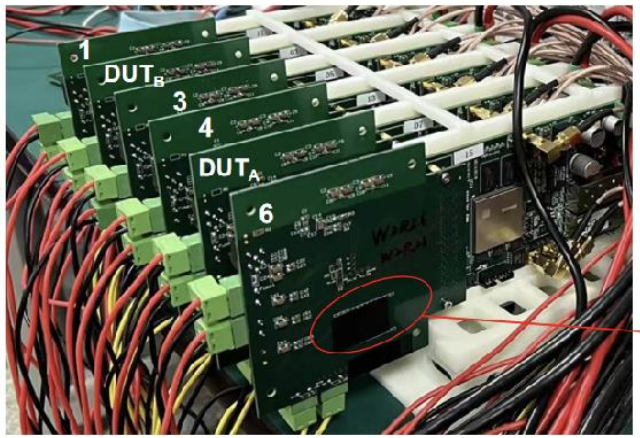
- **Pixel threshold and noise were measured with selected pixels**
  - Average threshold ~215 e^-, threshold dispersion ~43 e^-, temporal noise ~12 e^- @ nominal bias setting

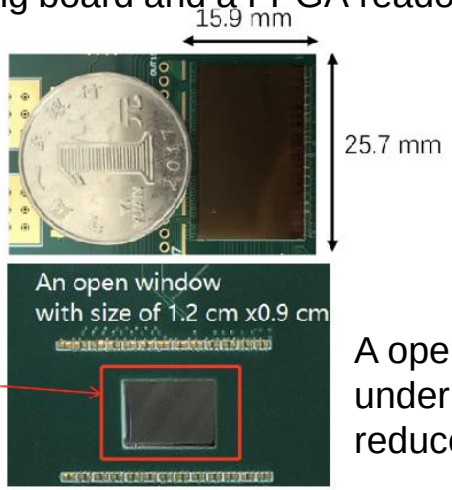




TaichuPix-3 telescope

- **The 6-layer of TaichuPix-3 telescope built**
  - Each layer consists of a TaichuPix-3 bonding board and a FPGA readout board

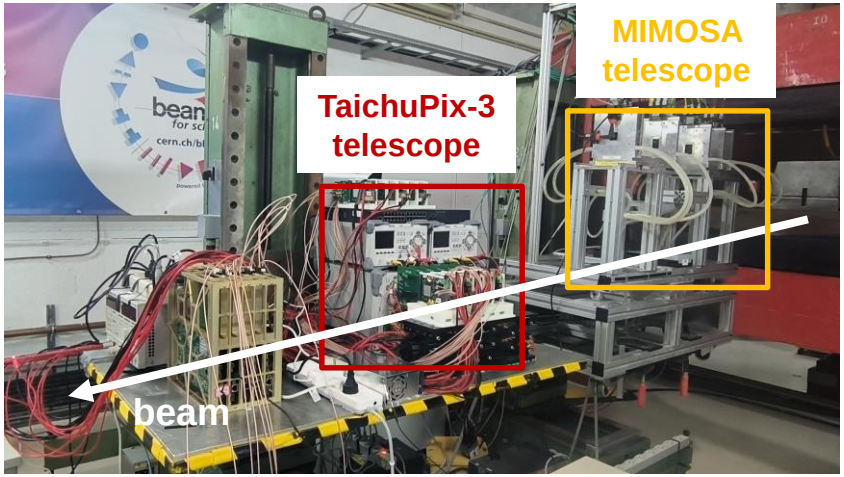




A open window on PCB under TC3 chip to reduce multi-scattering

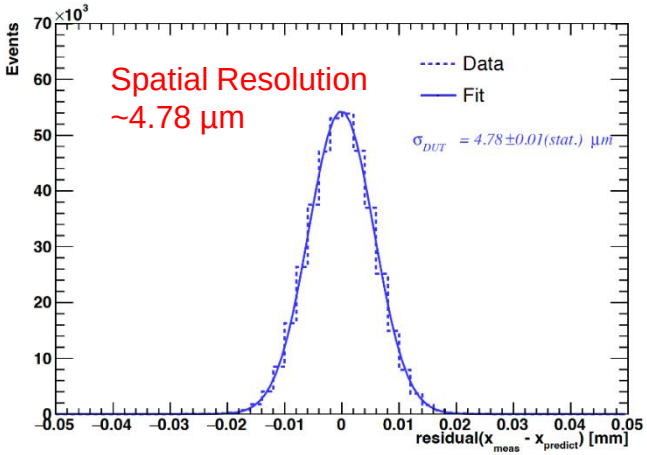
6-layer TaichuPix-3 telescope

- **Setup in the DESY testbeam**
  - TaichuPix-3 telescope in the middle
  - Beam energy: 4 GeV mainly used
  - Tests performed for different DUT (Detector Under Test)

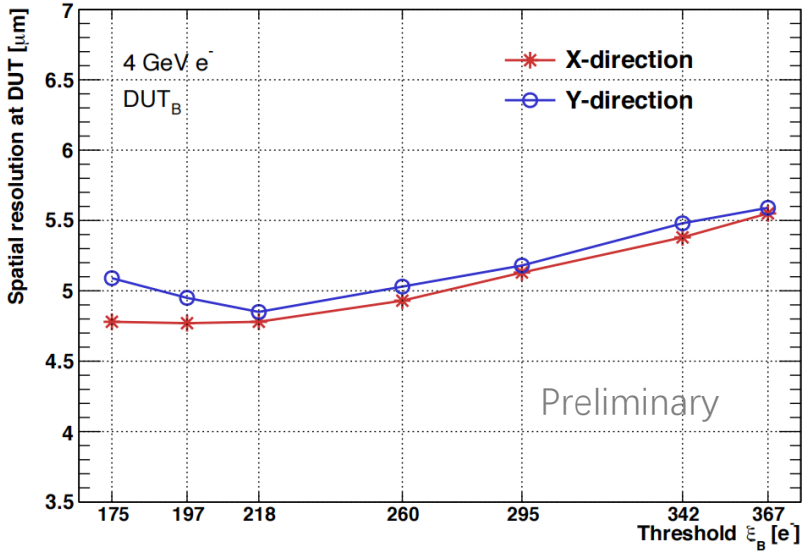


TaichuPix-3 beam test result

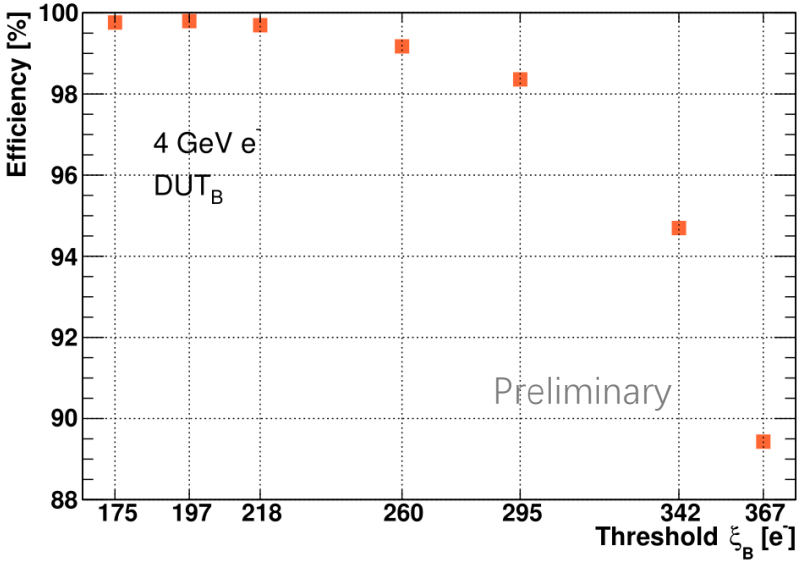
- **Spatial resolution**
  - Gets better when decrease the pixel threshold, due to the increased cluster size
  - A resolution < 5 μm achieved, best resolution is 4.78 μm
- **Detector efficiency**
  - Decreases with increasing the threshold, detection efficiency >99.5% at threshold with best resolution



Distribution of residual X



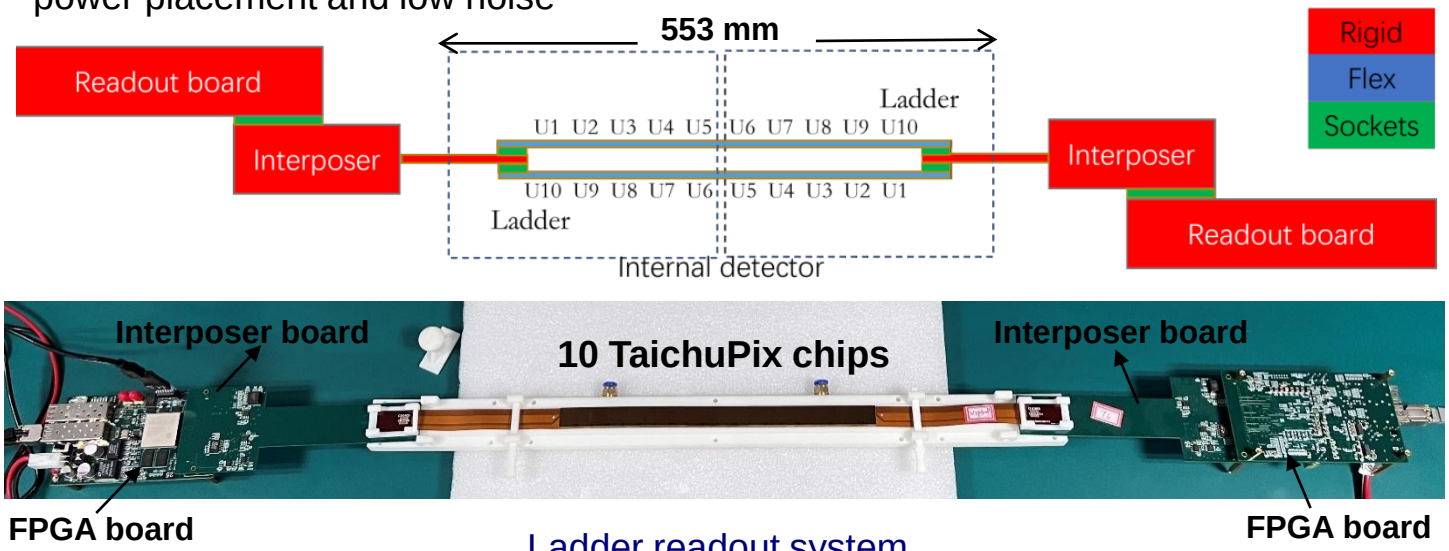
Spatial resolution vs. pixel threshold



Detection efficiency vs. pixel threshold

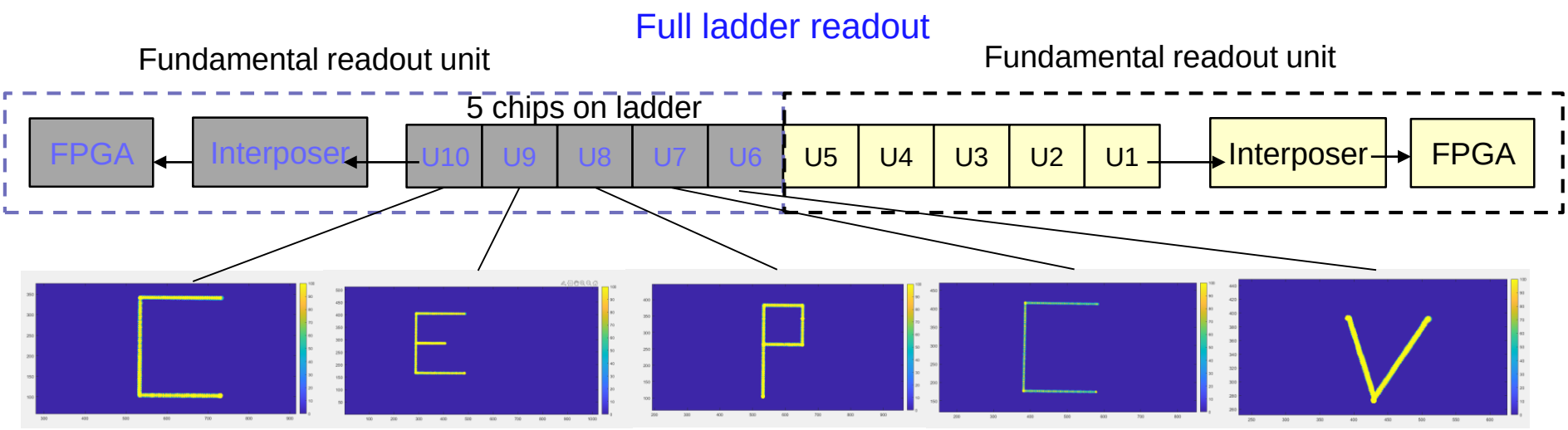
Ladder readout design

- **Detector module (ladder) = 10 sensors + readout board + support structure + control board**
  - Sensors are glued and wire bonded to the flexible PCB, supported by carbon fiber support
  - Signal, clock, control, power, ground will be handled by control board through flexible PCB
- **Challenges**
  - Long flex cable → hard to assemble & some issue with power distribution and delay
  - Limited space for power and ground placement → bad isolation between signals
- **Solutions**
  - Read out from both ends, readout system composes of three parts, careful design on power placement and low noise



Ladder readout system

Laser test result of ladder



Laser tests on 5 Taichupix chip on a full ladder
("CEPCV" pattern by scanning laser on different chips on ladder)

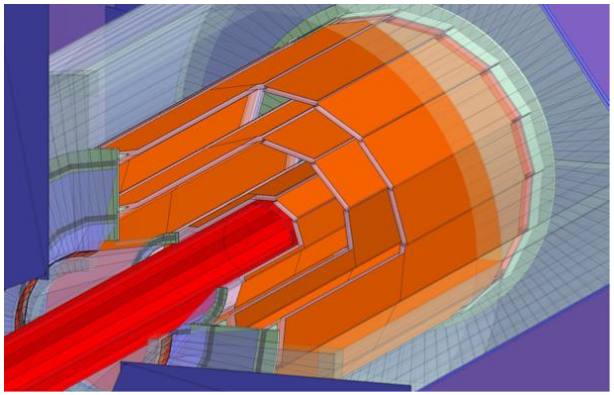
- **A full ladder includes two identical fundamental readout units**
  - Each contains 5 TaichuPix chips, a interposer board, a FPGA readout board

- **Functionality of a full ladder fundamental readout unit was verified**
  - Configuring 5 chips in the same unit
  - Scanning a laser spot on the different chips with a step of 50 μm, clear and correct letter imaging observed
  - **Demonstrating 5 chips working together → one ladder readout unit working**

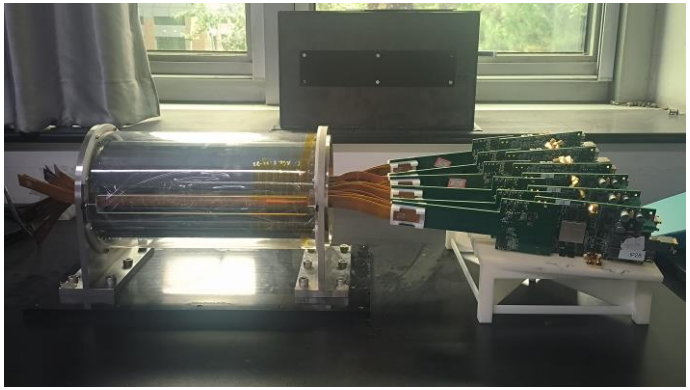
Summary

- **The full-scale and high granularity pixel prototype, TaichuPix-3, has been designed and tested for CEPC VTX R&D**
  - Spatial resolution of 4.78/4.85 μm measured with 4 GeV electron beam in DESY
  - Total ionization dose (TID) > 3 Mrad

- **Readout electronics for the sensor test and the ladder readout were developed**
  - Performed the sensor characterization in the lab successfully
  - Completed beam tests for the pixel sensor prototype and the vertex detector mechanical prototype



Concept (2016)



Vertex detector prototype (2023)

Thank you very much for your attention !