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Development of CMOS Pixel Sensor prototypes for the CEPC vertex detector

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The proposed Circular Electron Positron Collider (CEPC) imposes new challenges for the vertex detector in terms of material budget, spatial resolution, readout speed, and power consumption. The TaichuPix chip is a dedicated CMOS Pixel Sensor that is being developed for the first 6-layer silicon vertex detector prototype of the CEPC vertex detector R&D. The TaichuPix chip need to provide a spatial resolution better than $5\ \mu\text{m}$, and a radiation tolerance higher than 1 MRad. The TaichuPix development is based on a fast in-pixel readout combined with a hit-driven architecture, which would be beneficial for the high hit rate. Over the last years of R&D, several prototypes have been designed to optimize in-pixel circuit and readout architecture, and to verify radiation hardness. Two small-scale demonstrator chips ($25\ \text{mm}^2$) capable of achieving a hit rate up to $36\ \text{MHz}/\text{cm}^2$, were developed in a 180 nm CMOS process. Two different in-pixel digital readout designs, benefiting from the FE-I3 and ALPIDE approaches, have been implemented to achieve a fast readout. The readout of the pixel array is based on a proposed “column-drain” architecture. The positive results of the small-scale prototypes led to a submission of the first full-scale ($2.6\ \text{cm} \times 1.6\ \text{cm}$) TaichuPix prototype in 2022. These prototypes were firstly characterized with electrical and radioactive sources in laboratory. The full-scale sensor chip was further characterized at the DESY test beam facility. The design details of TaichuPix prototypes and a summary of the results obtained are given.

Primary author: ZHANG, Ying

Co-authors: WEI, Wei (IHEP, CAS); HU, Jun (IHEP,CAS); YAN, Ziyue (IHEP); ZHANG, Xiaoxu; WEI, Xiaomin; LI, Xiaoting; LIANG, Zhijun; ZHANG, Liang; DONG, Jianing; WU, Tianya; WANG, Wei; LI, Shuqi; ZHOU, Jia; HUANG, Xinhui; ZHANG, Hongyu; DONG, Mingyi; WANG, Jia; ZHENG, Ran; CASANOVA, Raimon; LU, Weiguo; ZHANG, Lei; QI, Ming; GRINSTEIN, Sebastian; GUIMARAES DA COSTA, Joao

Presenter: ZHANG, Ying

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