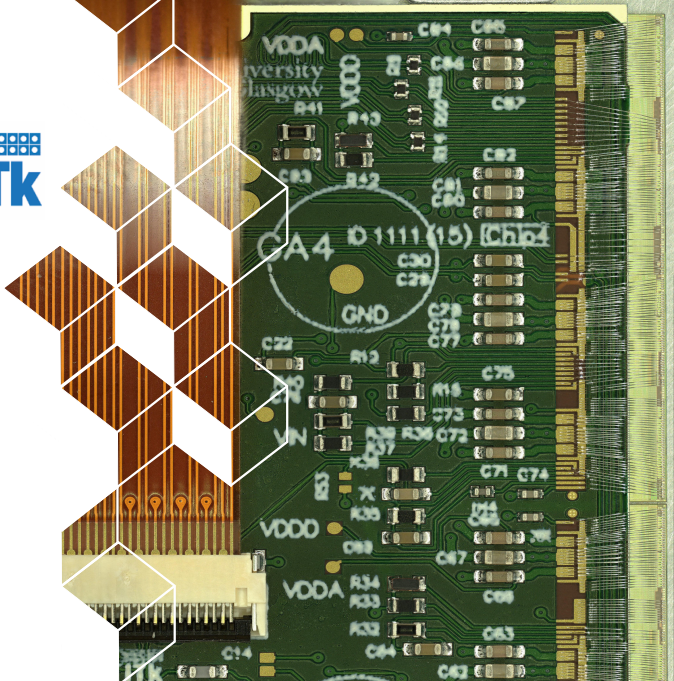
Module development for the ATLAS ITk Pixel Detector

Matthias Saimpert (CEA Saclay, IRFU/DPhP)
on behalf of the ATLAS ITk project

TIPP2023, Cape Town, South Africa

September 6, 2023



The ATLAS ITk pixel detector

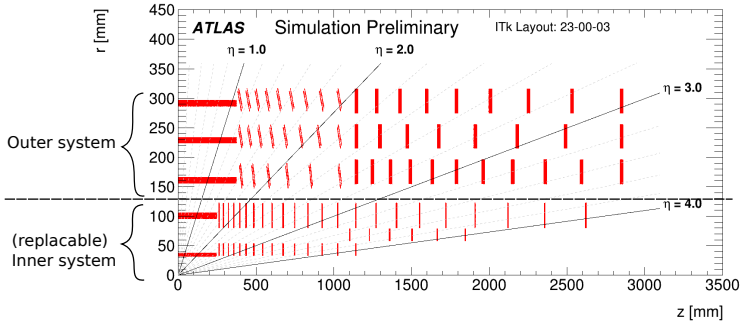
High Luminosity LHC (2026+)

- $\sim 7x10^{34}$ cm^{-2} s^{-1} lumi.
- $\sim$ 200 pileup interactions

ITk pixel system vs current

- $\sim$ 5G pixels ($\times$500)
- $\sim$ 8,400 modules ($\times$5)
- $\sim$ 13.5 m^2 active area ($\times$7)

ATL-PHYS-PUB-2021-024



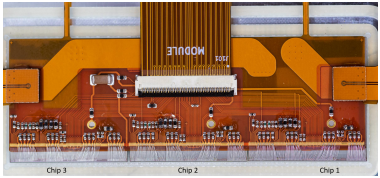
- **ATLAS requires a new inner tracker** for the LHC "high luminosity" phase (2026 onward)
- **Targeting same or better performance than current inner detector,** extending $|\eta| = 2.5 \rightarrow 4.0$
- Higher granularity, less material and improved radiation hardness (up to 20 MGy @ 4000 fb^{-1} exp.) required

$\rightarrow$ More details in Koji's talk

ITk pixel modules

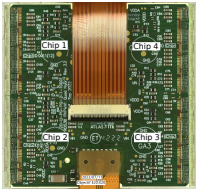
L0: $\sim$ 600 modules 'triplet'

- 3$\times$(1 sensor + 1 FE chip) glued to 1 flex PCB
- 250 µm 3D silicon sensor
- 50x50 µm^2 pixels (25x100 µm^2 in barrel)



L1 to L4: $\sim$ 8,000 modules 'quadruplet'

- 1 sensor + 4 FE chips glued to 1 flex PCB
- 150 µm n-in-p planar silicon sensor (100 µm in L1)
- 50x50 µm^2 pixels



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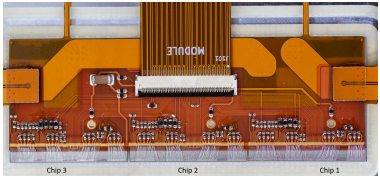

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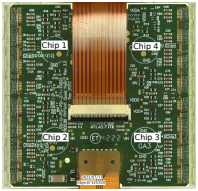

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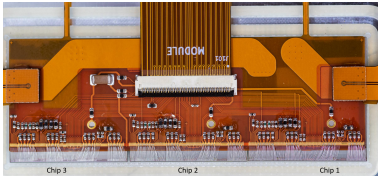

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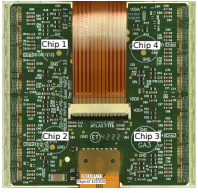

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- Modules use the RD53B front-end chip – joint ATLAS+CMS R&D on TSMC 65nm technology
  - ATLAS final chip: ITkPix - 400x384 pixels, differential analog FE – JINST 16 (2021) 12, (see Stefano's talk)
  - chip size 2x2 cm^2, thickness 150 µm, low threshold (1000*e*), high hit rate (3 GHz/cm^2), 4 data links at 1.28 Gbit/s

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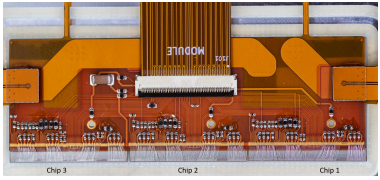

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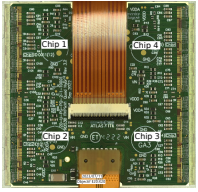

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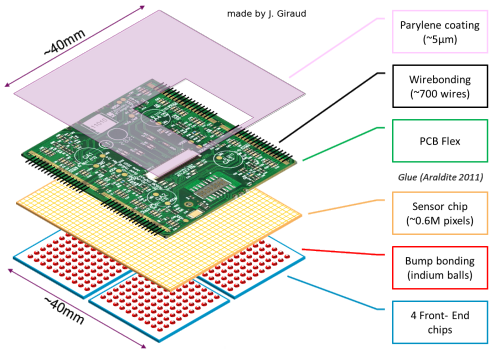
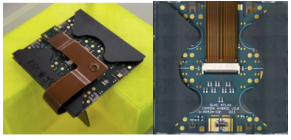
After yield factor ∼ **12k modules to be produced in total, incl. 95% quadruplet (focus of this talk)**

ITk pixel quad module layout





wirebond mechanical protection

- **4 ITkPix flip-chip bump-bonded to 1 sensor tile**
  - indium or solder bumps
  - ITkPix and sensor tiles produced in industry
  - hybridization performed in industry
- **Custom-designed flex PCB glued on sensor backside**
  - flex PCB produced in industry
  - incl. connectors for power and data service cables
  - wirebonded to 4 ITkPix chips
  - gluing + wirebonding performed in labs
- **Wirebond protections**
  - electrical: parylene coating (in labs or industry)
  - mechanical: 'canopee' (in labs)
    [outer barrel modules only, not shown on sketch]

Total thickness: 565 µm (515 for L1)

Module production: organization & timeline

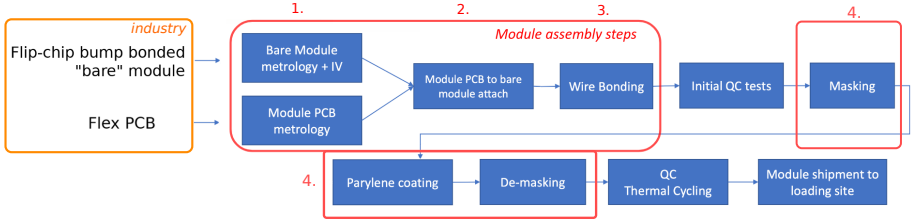
- **Dispatched over $\sim$ 20 institutes** (CERN, France, Germany, Italy, Japan, UK, USA)
  - often subset of operations per site, e.g. 50% do testing only
  - grouped in 'regional clusters' incl. $\geq$ 1 complete production line w/ backups

Challenge: harmonize process across sites $\rightarrow$ $\sim$ 80 qualification 'blocks' defined must be passed to unlock module component deliveries

- **General timeline**
  - 2021-2022: 'R&D' production of $\sim$ 160 modules based on previous chip version (RD53A)
  - May 2022: Module Final Design Review (FDR) is passed
  - 2023: Site qualification & pre-production of $\sim$ 500 modules (rate $\times$ 4 w.r.t R&D prod.)
  - 2024+: Module production, $\sim$ 12,000 modules (rate $\times$ 2 w.r.t pre-prod.)
  - 2026 Module production complete

1. Module assembly steps

Overview & Main challenges



- **First step of module construction in lab – components received from industry**
  1. component reception → sensor IV
  2. bare module to flex PCB attach → common dedicated tooling
  3. wirebonding of flex PCB to FE chips → wirebond pull tests
  4. wirebonding protection → electrical/mechanical, + visual inspection/metrology between each step

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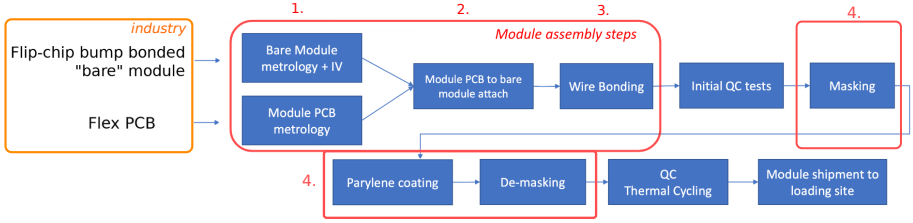

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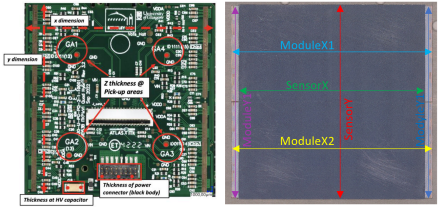
Main challenges (personal selection)

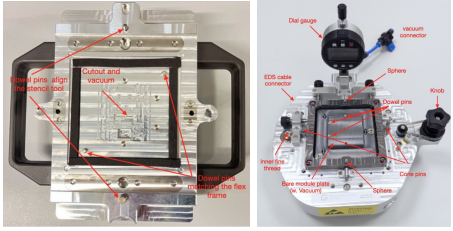
- tight module envelope specifications
- no delamination/failure over $\Delta T = 80°C$
- 'fast' assembly ($<$ few hrs w/o curing time)

Metrology & Flex PCB attach

Flex PCB & Bare module metrology



Common flex-attach tooling: flex PCB & bare module jig



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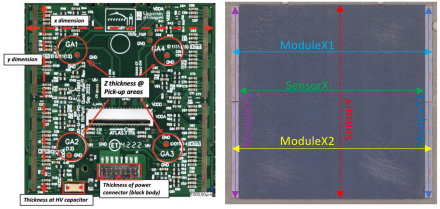

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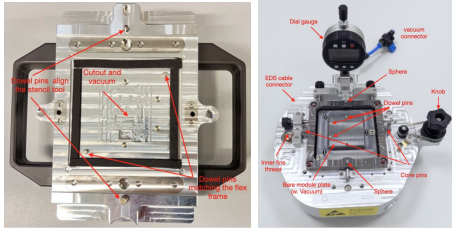

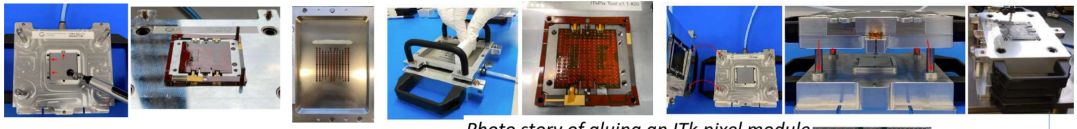

Photo story of gluing an ITk-pixel module

- ≥1 tooling planned per site

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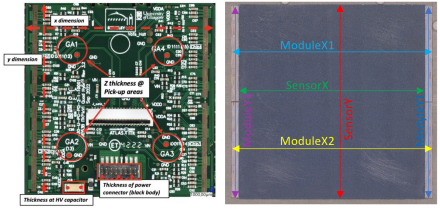

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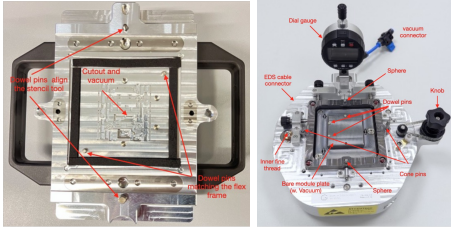


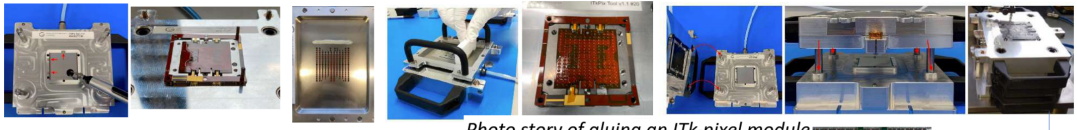
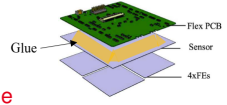
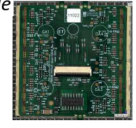


Photo story of gluing an ITk-pixel module

- ≥1 tooling planned per site
- **Critical aspects:**
  - visual inspection of flex PCB
  - good glue coverage & thickness, no seapage
  - good flex PCB / bare module alignment (±100 µm)



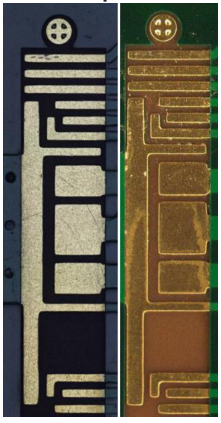


8h later

Glued module

Visual Inspection & Wirebonding

Visual inspection of flex PCB pads



[taken w/ Keyence VHX-7000]

- contamination revealed only w/ specific lighting
- PCB pad surface quality crucial for strong bondings

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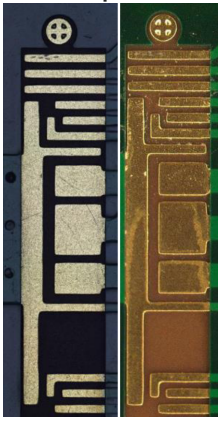

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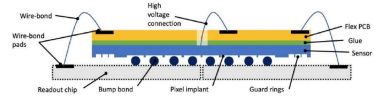
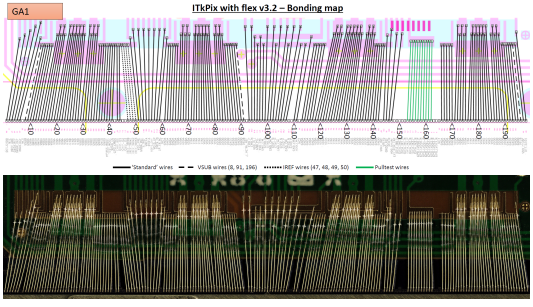
Wirebonding map (here for chip 1)

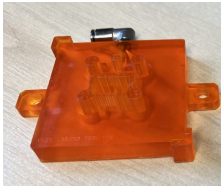


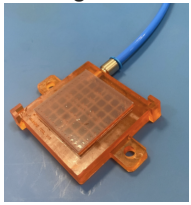


- $\sim$ 170 aluminium wires per chip (25 µm diameter)
  $\rightarrow$ high density, various lengths & angles
- alignment & glue coverage crucial for wirebonding

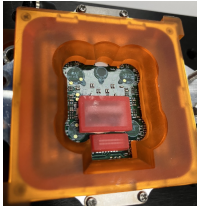
Electrical & mechanical protections

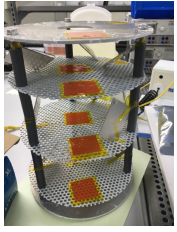
Masking bef. parylene coating





masking tools for dicing tape





(left) connector masking caps
(right) common module holder for coating

- **high density of wirebonds → electrical protection**
  - parylene coating ($\sim 5\,\mu m$)
  - masking of module backside, pickup areas and connectors

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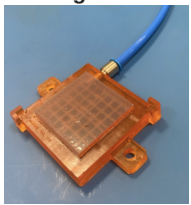

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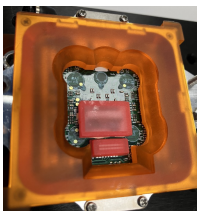
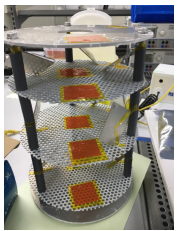
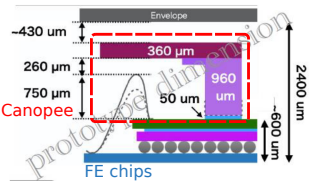




(left) connector masking caps
(right) common module holder for coating

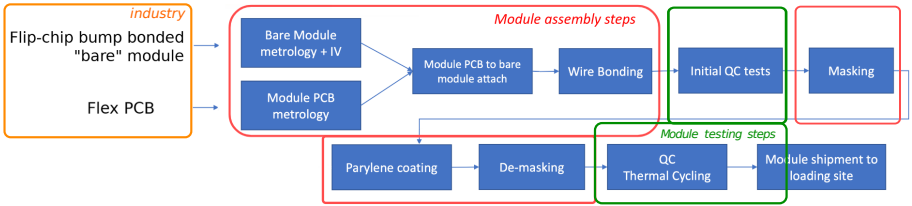
- **high density of wirebonds → electrical protection**
  - parylene coating ($\sim 5\,\mu m$)
  - masking of module backside, pickup areas and connectors
- (outer barrel only)
  tighter space for services → mechanical protection
  - 'canopee' element glued after parylene coating
  - conductive glue required
  - final design/procedure being finalised

Canopee



2. Module testing steps

Overview & Main challenges



- **Different tests part of quality control**
  - tests at room temperature → reception tests, first power-up, 'minimum health' tests
  - tests at controlled temperature → full characterization incl. ADC/DAC calibration and pixel tuning
  - thermal cycling → [-45, +40°C] and [-55, +60°C]
  - bump disconnection tests → w/ Sr-90 source, x-ray gun or using cross-talk effect – bef./aft. thermal cycling

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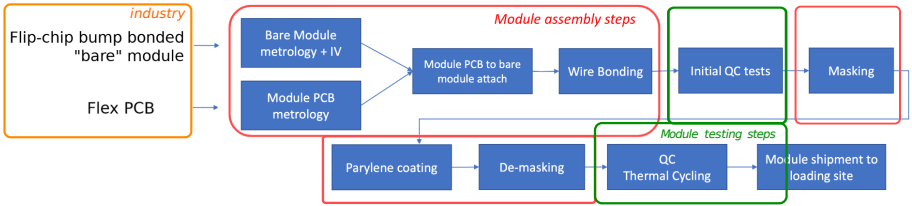

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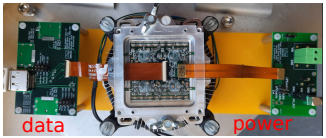
Main challenges (personal selection)

- fast/reliable detection of disconnected bumps
- process automation and parallelization
- 'fast' characterization (< few hrs w/o thermal cycles)

Generalities & Tests at room temperature



- **Module handling and interfaces during testing**
  - module remains in metallic carrier w/ power + data pigtails connected
  - specific adapter cards for individual module testing
- **Common measurement + analysis software**
  - collection of python packages maintained/developped collaboratively

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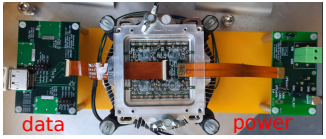
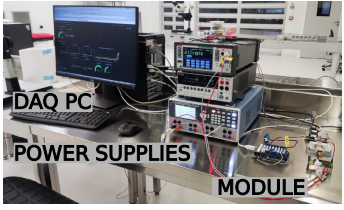
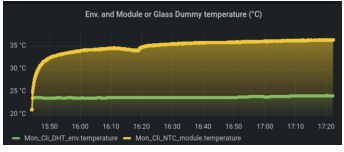
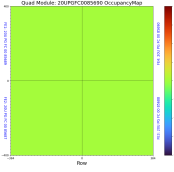




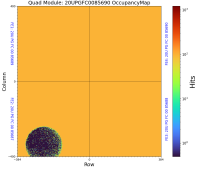


- **Module handling and interfaces during testing**
  - module remains in metallic carrier w/ power + data pigtails connected
  - specific adapter cards for individual module testing
- **Common measurement + analysis software**
  - collection of python packages maintained/developped collaboratively
- **Room temperature: simple test bench w/ passive cooling**
  - used for first power-up and ‘minimum health’ tests
  - typically located in ISO7 assembly cleanroom
  - power dissipated by aluminium plate or cooling fins

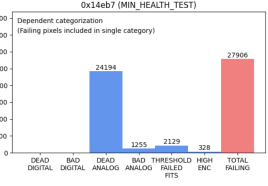
digital scan



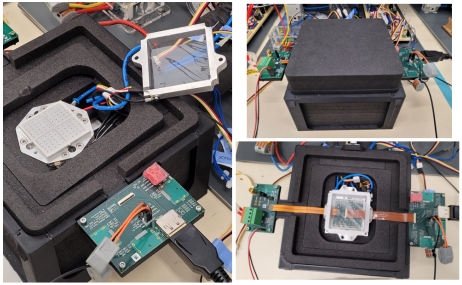
analog scan



analysis results for chip 2

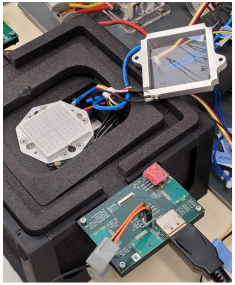


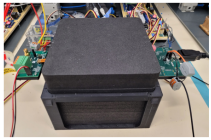
Tests at controlled temperature

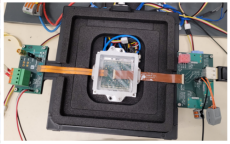


- **Common cooling unit & vacuum chuck design**
  - used for full characterization and tuning
  - active cooling w/ peltier, chiller unit and dry air
    $\rightarrow$ typically can go down to T= -35°C
  - a couple of designs exist, being harmonised

Tests at controlled temperature







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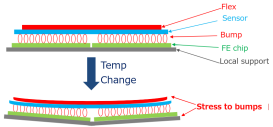
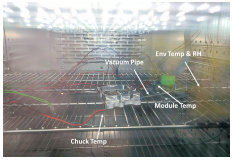
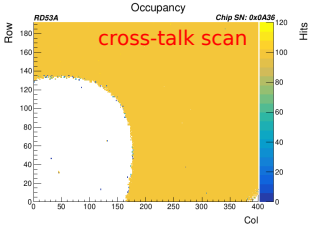
  - used for full characterization and tuning
  - active cooling w/ peltier, chiller unit and dry air
    $\rightarrow$ typically can go down to T= -35°C
  - a couple of designs exist, being harmonised

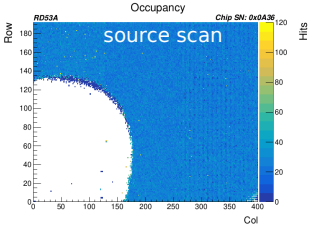
- **Climate chamber for thermal cycles**
  - used for 10 (1) thermal cycles at -45, +40°C (-55, +60°C)
  - bump bonding are stressed when temperature changes
  - vacuum applied to mimic cell-loaded modules

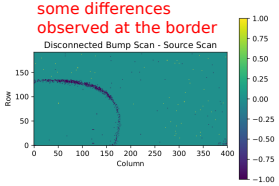




Tests of bump bonding delamination



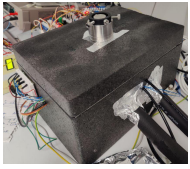




- **3 techniques being explored**
  - Sr-90 source or x-ray gun scan: robust but heavy infrastructure (MBq, shielding)
  - cross-talk scan: inject neighbouring pixels and read central pixel, easy but less reliable
  - no-bias scan: check noise/threshold variation with HV ON/OFF, not usable after loading

x-ray gun

Sr-90 source in use



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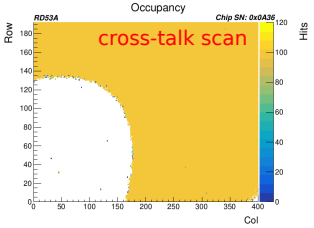
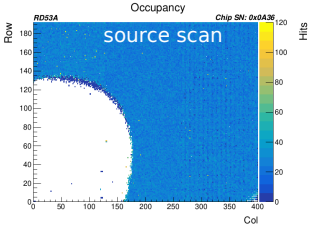
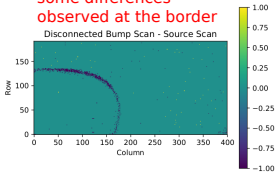




some differences
observed at the border



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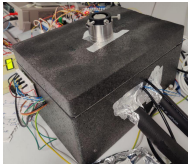
- **Measurement performed before/after thermal cycling**
  - modules w/ too weak bumps will be excluded
  - final criteria to be derived from data being collected now

x-ray gun

Sr-90 source in use



3. Summary & next steps

Getting ready for production start-up

- **Production site qualification in progress**
  - prerequisite to join for preproduction
  - about 20 site candidates[1] $\rightarrow$ 'regional clusters' being organised
- **Pre-production to be finalised by the end of the year, production will follow**
  - $\sim$ 12,000 modules to be assembled & tested during production
  - $\times$2 production rates w.r.t pre-production

Points of attention (personal selection)

- **schedule:** pixel module production close to critical path
- **flex PCB:** pad contamination
- **testing rates:** high level of automation required

[1] often to a subset of operations only

Thank you for your attention

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91 191 Gif-sur-Yvette Cedex
France
matthias.saimpert@cea.fr

Appendices

4. **Flex attach validation**

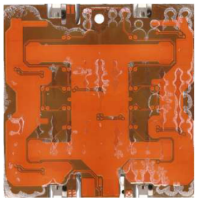
5. **Anomaly detection on flex PCB**

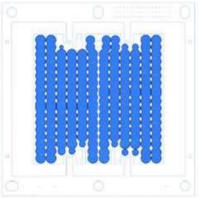
6. **Bump bond stress tests**

7. **Readout w/ data merging**

Focus on: flex attach validation





Glue pattern after using the final prototype stencil: continuous glue layer

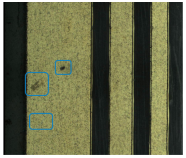
- **Glue pattern & HV hole**
  - continuous layer w/ coverage $>$ 80% achieved w/ stencil glue dots, no seapage
  - validation w/ glass dummy modules
- **Delamination tests**
  - thermal cycling of silicon dummy modules: up to 1000 extreme cycles (-55, +60°C), 1 module put in a -40°C freezer during 10 months ...
  - $\sim$ 160 RD53A prototype modules assembled and cycled
  - 10 modules irradiated w/ test beams
  - no detachment or any visible failure of the adhesive

talk at PIXEL2022

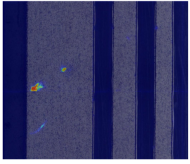
Focus on: anomaly detection on flex PCB

work of V. Maiboroda (CEA Saclay)

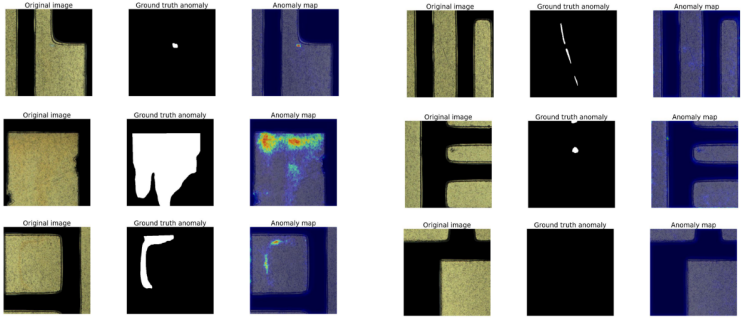
- **Goal: automate visual inspection on ITk pixel module before wirebonding**
- Various anomaly detection algorithms being compared
- Larger dataset to be acquired during preproduction



Chemical contaminations and scratch on a pad.

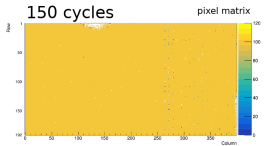


Heat anomaly map from the algorithm. The higher the "temperature", the higher the probability of defectiveness.



Examples of the input data with results in the form of binary masks and heatmaps.

Focus on: bump bond stress tests



Sample	Vendor	Substrate	Parylene	Module	Chip	Number of thermal cycles with <0.1% disconnects	Max. number of cycles/number of disconnects
DCM34	C	OB TPG	no	Dual	2	50-100	500/985
GD02	C	OB TPG	no	Dual	1	10-50	700/2539
GD02	C	OB TPG	no	Dual	2	10-50	700/13594
GD01	C	EC CFRP	no	Dual	1	100-250	500/1523
GD01	C	EC CFRP	no	Dual	2	100-250	500/583
DCM32	C	EC CFRP	no	Dual	1	>1000	1000/46
DCM32	C	EC CFRP	no	Dual	2	>1000	1000/17
KEKQ14	C	OB Pyrod	yes	Quad	1-4	>100	100/0
KEKQ17	C	OB Pyrod	yes	Quad	1-4	>100	100/0
KEKQ18	C	OB Pyrod	yes	Quad	1-4	>100	100/0
GLA2	C	EC CFRP	no	Quad	1-4	>100	100/0
GLA3	C	EC CFRP	yes	Quad	1-4	>100	100/0
GLA4	C	EC CFRP	yes	Quad	1-4	>100	100/0
RD08	A	EC CFRP	no	Dual	1	>1000	1000/0
RD08	A	EC CFRP	no	Dual	2	500-1000	1000/155
RD05	A	EC CFRP	no	Dual	1	>1000	1000/31
RD05	A	EC CFRP	no	Dual	2	>1000	1000/0
RD04	A	EC CFRP	no	Dual	1	>1400	1400/26
RD04	A	EC CFRP	no	Dual	2	1200	1600/81
DCM2	A	OB TPG	no	Dual	1	>100	100/42
DCM2	A	OB TPG	no	Dual	2	250-500	1000/248
DCM5	A	OB TPG	no	Dual	1	10-50	250/354
DCM5	A	OB TPG	no	Dual	2	50-100	500/136
B10	B	EC CFRP	no	Dual	1	>50	50/0
B10	B	EC CFRP	no	Dual	2	50-100	1000/37490
B15	B	EC CFRP	no	Dual	1	500-1000	1000/855
B15	B	EC CFRP	no	Dual	2	100-250	500/41497
B17	B	EC CFRP	no	Dual	1	0-10	1000/8027
B17	B	EC CFRP	no	Dual	2	100-500	1000/11699

0.1% = 77 bonds

Test	Vendor and module type	Test type	Surface preparation	Bumps per FE	Ultimate force per chip (N)	Ultimate bump strength (N)
1	Vendor-A single-chip module	Double lap shear test	Acetone cleaning	400*336	>652.8	> 0.0049
2	Vendor-A single-chip module	Single lap shear test	Plasma cleaning	400*336	>693	> 0.0052
3	Vendor-A single-chip module	Single lap shear test	Heavy acetone and alcohol cleaning	400*336	>1060	> 0.0079
4	Vendor-A single-chip module	Single lap shear test	Scotch-brite	400*336	>1450	> 0.0108
5	Vendor-B quad module 1st FE	Single lap shear test	Scotch-brite	400*384	853	0.0056
6	Vendor-B quad module 2nd FE	Single lap shear test	Scotch-brite	400*384	219	0.0016

Summary of the results of lap shear-stress tests.

- **Coefficient thermal expansion mismatch between module components**
  - temperature variations expected during operation: CO_2 cooling, power cycles, ...
  - induces mechanical stress on bump bondings
- **Up to 1000 cycles performed at -55, +60°C on various module types**
  - bump bonds demonstrated to survive 100 cycles w/ $< 0.1\%$ disconnection
  - variations across vendors and carbon support material, in agreement w/ shear tests
  - less delamination observed aft. parylene coating

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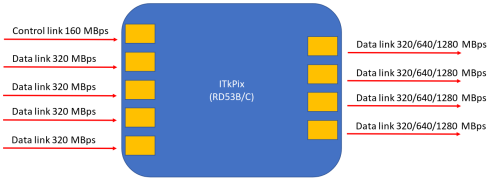
Focus on: readout w/ data merging



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- ITkPix has a complex interconnection feature enabling chip-to-chip communication allowing to optimize data link utilisation
- Data merging required to operate the ITk
- Quality control procedure being defined: eye diagram, test $2 > 1$ and $4 > 1$ modes

Layer	Section	Number of Links/FE
0	Flat barrel	4
	Barrel rings	3
	End-cap rings	2
1	Flat barrel	0.5
	Barrel rings	1
	End-cap rings	1
2	Flat barrel	0.5
	Barrel rings	0.5
	End-cap rings (1-5)	0.5
	End-cap rings (6-11)	1
3	Flat barrel	0.25
	Barrel rings	0.25
	End-cap rings	0.5
4	Flat barrel	0.25
	Barrel rings	0.25
	End-cap rings (1-7)	0.25
	End-cap rings (8-9)	0.5

Table 3: Number of links/FE for the different regions of the pixel detector. A fractional number of links/FE means that the same link is shared between multiple chips to send data out.