

## The DEPFET based all-silicon module for the Belle II Pixel Detector PXD

▷ PXD at Belle II

└→ Construction, performance, and lessons learned

▷ Very brief outlook beyond HEP application

DEPFET PXD Collaboration and the team at the Semiconductor Laboratory of the Max Planck Society







- $\triangleright$  Higher luminosity, KEKB  $\rightarrow$  SuperKEKB "B factory"
  - $\rightarrow$  goal Lumi 6 x 10<sup>35</sup> cm<sup>-2</sup>s<sup>-1</sup>, achieved 4.7 x 10<sup>34</sup> cm<sup>-2</sup>s<sup>-1</sup> in June 2022
  - → Higher event rate, higher background, higher radiation damage ...
  - → Ongoing long shutdown since July 2022 until end 2023



- $\triangleright$  Belle II
  - └→ Upgraded detector
  - → Physics data-taking since March 2019
    - $\rightarrow$  427.8 fb<sup>-1</sup> recorded until June 2022
  - $\rightarrow$  Goal is 50 ab<sup>-1</sup> during lifetime (203x)



## Belle II PXD

 $\sim 2\,\mathrm{m}$ 

Capacitors





	L1	L2
# ladders (modules)	8 (16)	12 (24)
Distance from IP (cm)	1.4	2.2
Thickness (μm)	75	75
#pixels/module	768x250	768x250
#of address and r/o lines	192x1000	192x1000
Total no. of pixels	3.072x10 <sup>6</sup>	4.608x10 <sup>6</sup>
Pixel size (μm²)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Sensitive Area (mm <sup>2</sup> )	44.8x12.5	61.44x12.5





#### DAQ, data reduction Data Optical fiber **ROI** selection $\sim 0.5\,\mathrm{m}$ Handling Optical transmitter Dock Box Hub ■ Optical fiber FTSW, clock, trigger Camera link cable (DHH) Ethernet cable Optical fiber (High speed data) Patch ∎ Ethernet Infiniband cable Slow control Panel Power cable Power cable Ethernet $\mathbf{LMU}$ Power cable $\mathbf{PS}$ Capacitors

 $\sim 15\,{\rm m}$ 

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#### **DCDB** (Drain Current Digitizer)

Amplification and digitization

- UMC 180 nm
- 256 input channels
- 8-bit ADC per channel

**DHPT** (Data Handling Processor) First data compression

- TSMC 65 nm
- CM and pedestal correction
- Data reduction (zero suppression)
- Drives data link

#### **SwitcherB**

- AMS/IBM HVCMOS 180 nm
- Gate and Clear signal
- 32x2 channels

#### ▷ Pixel array operated in "rolling shutter" mode, 20µs/f

 $\rightarrow$  Only 4/768 rows active a time  $\rightarrow$  low power in active area













#### module assembly overview



#### Flip Chip of ASICs (~240°C):

- Bumped ASICs have the same solder balls (SnAg)
  DHP bumping at TSMC, DCD bumping via Europractice
  - SWB bumping on chip level
- ▷ Flip Chip of PXD modules on custom made support plates

SMD placement (~200°C):

- ▷ Passive components (termination resistors, decoupling caps)
- ▷ Dispense solder paste, pick, place and reflow

Kapton attachment (~170°C), wire bonding:

- ▷ Solder paste printing on kapton,
- $\triangleright$  Wire-bond, wedge-wedge, 32  $\mu$ m Al bond wires























#### > 71 modules (+46 for PXD2) attached to pre-tested kapton cables

- → Module assembly yield ~96% (after rework)
- $\rightarrow$  ~50% contingency, both for PXD1 and PXD2
- ▷ collaborative effort (Bonn, Göttingen, HLL, MPP, IFIC, DESY)
  - → script based, automated procedure
  - → optimize/confirm ASIC and DEPFET parameters
    - → linear response of the ADC, pedestal compression
    - → Off-module link of DHP
  - → charge collection (DEPFET voltages: Drift, HV, Clear-Off)
- ▷ Damage and repair after testing (PXD1 and PXD2)
  - → 2 x kapton cables revealed shorts (modules ok after kapton exchange)
  - $\rightarrow$  1 x module: mechanically damaged (can not be depleted)
  - → 2 x modules: SwitcherB damaged at test
  - $\rightarrow$  4 x modules suffered from cooling malfunction (condensation)



After characterization: Sr90 spectrum (Bonn Uni)

- ✓ 291 unresponsive single pixels
- ✓ 251 noisy pixels
- ✓ 99.85% active pixels



## ladder assembly and installation





- $\triangleright$  Join two modules to a ladder  $\rightarrow$  "ladder gluing"
  - $\mapsto$  v-grooves for small ceramic inserts on the back side  $\rightarrow$  Reinforcement of the joint
- > **Yield issue**: out of 17 assembled ladders, 5 were lost due to damage at assembly
  - → Resolved for PXD2
- ▷ Install de-scoped PXD1 to meet the schedule for the start of data taking (March 2019)
  - → Full L1 (8 ladders) and 2/12 ladders in L2



▷ Completion of PXD ("PXD2") with new modules accomplished 2023







#### PXD1: operation in Belle II

- ▷ PXD in operation in Belle II March 2019 until June 2022 with good performance
  - → First application of DEPFET sensors in HEP!
- ▷ S/N around 40, stable over time and with good homogeneity
  - $\mapsto$  Narrow and stable pedestals and noise
- $\triangleright$  Efficiency to find in L1 or L2 ~ 96%
  - → ~99% efficiency in fiducial region
- ▷ Impact parameter resolution close to expectations  $\rightarrow$  data:  $\sigma(d_0) = 14.2 \mu m \rightarrow$  about 2x better than Belle









# PXD1: Physics Performance



#### VXD Physics Performance



- Belle II proper time resolution ~2x better than Belle
- thanks to PXD precision and smaller beam pipe diameter
- Belle II published world-leading lifetime measurements on charmed mesons: D<sup>0</sup>/D<sup>+</sup>







#### surprises I



- ▷ Damage due to beam losses/incidents
  - → Origin of beam losses not completely clear (beam-dust events? machine glitches?)
- $\triangleright$  Resulted in collimator damage, quench of the QCS magnet system ...
- $\triangleright$  Huge instant radiation dose of about 300 rad in ~40  $\mu$ s in the PXD
  - $\mapsto$  Permanent damage of entire rows  $\rightarrow$  "dead", inefficient regions
  - → Overall efficiency loss of about **3 percentage points** at the end of run1
- $\,\triangleright\,\,$  Origin of PXD damage traced back to SEE in the Switcher HV-CMOS chip
  - □→ Reproduced at MAMI accelerator in Mainz
    - $\mapsto$  electron pencil beam scanned over DEPFET array and Switcher chip



- ▷ Mitigation (from PXD side and SuperKEKB) ongoing
  - $\mapsto$  Accelerate beam abort signal and power-down of modules
  - → Root cause in the switcher chip understood (new version under production, tests pending)





L1 hitmaps after beam loss in May '21





#### surprises II



- $\triangleright$  Backplane (HV, depletion) is increasing from tens of  $\mu$ A to >1mA
  - → Most affected modules are currently in +x direction
  - $\rightarrow$  This is where the background is 2x higher ...
- ▷ Module performance not affected, noise and signal stable
  - → Also negligible contribution to overall power consumption
- arepsilon Issue: the power supply system is not designed to supply that high current
  - → Some PS upgraded already in PXD1, for PXD2 PS will be able to supply up to 28 mA
- $\triangleright$  Root cause
  - $\mapsto$  Guard rings on the back side not fully functional at higher radiation doses
- $Descript{Confirmed}$  by dedicated photon irradiations on test modules



- x-ray lab campaigns: expect currents saturate at certain dose
- not observed in PXD yet











- $\triangleright$  (incomplete) PXD1 in operation from May 2019 until June 2022
- ▷ (complete) PXD2 assembled with leftover modules from PXD1 and newly produced sensors and assembled modules and ladders
- ▷ Installed in Belle July 2023, currently under commissioning, run2 start scheduled December 2023







PXD2 - Pedestals (200 frames)







## Same module concept, different application



- ▷ Ultrafast direct electron detection for 300 keV TEM 80 kHz frame rate for 1 Mpix camera
  - $\rightarrow$  Sensor 50 µm (optionally 30 µm)
  - → Optimized 60 µm DEPFET pixel cell with high dynamic range (800 k signal electrons)
  - └→ Challenging operation in in very narrow UHV chamber















- ▷ Belle II PXD: the first full vertex detector based on DEPFETs!
  - → Overall performance of the modules meets the requirements at SuperKEKB
  - → Run1 successfully finished with descoped PXD1
  - → Run2 with complete PXD2 scheduled to start end 2023
  - → There were a few surprises, many lessons learned
    - → One of the most important ones: have to make the system more user friendly!
- > The concept of the DEPFET all-silicon module finds now new applications in a different field
- $\triangleright$  This is not the end, there is more to come
  - → Integration of micro-channels for cooling under way
  - → New generation of DEPFETs with improved characteristics finished and being tested
    - → Higher amplification, smaller pixels, high dynamic range, improved radiation tolerance ....





