#### **TECHNOLOGY IN INSTRUMENTATION & PARTICLE PHYSICS CONFERENCE (TIPP2023)**

Cape Town International Convention Center (CTICC), South Africa, 4-8 September 2023



## Applications of CMOS technology at the ALICE experiment





on behalf of the ALICE Collaboration

TIPP23 | 4-8 September 2023 | Domenico Colella - University and INFN Bari

## Evolution of silicon pixel sensor application in ALICE from LHC Run1 to the future



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## **Evolution of silicon pixel sensor application** in ALICE from LHC Run1 to the future



closed

ALICE 3

beyond LHC Run4

massless detector

# MAPS

(Monolithic Active Pixel Sensor)

## for tracking and timing layers

## ALPIDE leap

- ➡ 180 nm CMOS
- from partially to fully depleted sensor

## ITS3 developments

- ➡ 65 nm CMOS
- stitching technique
- sensor bending

## ALICE3 developments

- in vacuum retractible vertexer
- ➡ timing performance for TOF



ALPIDE sensor mounted on carrier board

## ALICE upgrade for the LS2

High-precision measurements of rare probes at low  $p_T$  requires:

- Improved vertex reconstruction and tracking capabilities
- Gain factor 100 in statistics for minimum-bias trigger
  - the very low S/B ratio prevents selection with hardware trigger
  - read out all interactions up to the maximum LHC Pb-Pb collision rate of 50 kHz





New Inner Tracking System (ITS2)

New Muon Forward Tracker (MFT)



New TPC Readout Chambers (ROCs)



New Fast Interaction Trigger (FIT) detector



Readout upgrade for other detectors

Integrated Online-Offline system (O<sup>2</sup>)

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#### Inner Tracking System upgrade

#### **Requirements**

- » Improve impact parameter resolution
  - Reduce IP-to-first layer distance (new beam pipe)  $\rightarrow$  22 mm
  - Reduce material budget  $\rightarrow$  0.36% X/X<sub>0</sub> (Innermost layers)
  - Reduce pixel size  $\rightarrow$  ~30 x 30  $\mu m^2$
- » Improve tracking efficiency and  $p_T$  resolution at low  $p_T$ 
  - Increase granularity  $\rightarrow$  from 6 to 7 layers, all pixels
  - Increase readout capabilities  $\rightarrow$  from 1 kHz to 100 kHz





10 m<sup>2</sup> active silicon area 12.5×10<sup>9</sup> pixels



## Inner Tracking System upgrade

#### **7-layer barrel geometry based on MAPS**

- » Inner Barrel (IB) : 3 layers
- » Outer Barrel (OB) : 4 layers
- » r coverage: (min) 22 (max) 394 mm
- » η coverage: (min) 1.3 (max) 2.5







#### **Inner Tracking System upgrade**

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ITS Outer Barrel surrounding the beam pipe, MFT in the back



**ITS Inner Barrel Bottom and Outer Barrel** 

#### **Inner Tracking System upgrade**





**Conceptual Design Report** 

#### Ten years from conceptual design to first event reconstruction and almost 30 institutes from more than 10 countries involved!

#### 180 nm CMOS technology: sensor details



J. NIMA 765 (2014) 177–182

» MAPS development for ALICE ITS2 detector @LHC (2021) → ALPIDE

- pixel dimensions: 28 x 28 µm<sup>2</sup>
- matrix: 512 × 1024 pixels (524k)
- CMOS technology: TowerJazz 0.18 µm
- power budget: 40 mW/cm<sup>2</sup>

- Detection layer: 25 μm high-resistivity (> 1 kΩcm) epitaxial layer
- DEEP P-WELL to shield CMOS circuitry and avoid loss of efficiency
  - $\rightarrow$  charge collected from the non-depleted zone by diffusion and prone to trapping after irradiation
- Total thickness: 50 µm



#### 180 nm CMOS technology: sensor details



- » In-pixel front-end
  - Analog signal formation (9 transistors, full-custom)
  - Multiple-event memory: 3 stages (62 transistors, full-custom)
  - Configuration: pulsing & masking registers (31 transistors, full-custom)
  - Testing: analogue & digital pulse circuitry (17 transistors, full-custom)

O(200) transistors / pixel

#### Single pixel readout mechanism



#### 180 nm CMOS technology: sensor details



#### **Rolling Shutter**



#### **Global Shutter**



#### » Pixel matrix read-out

- Fully integrated in the sensor
- Global shutter and zero suppression realised through priority encoding
- Single pixel multi-event memory and global strobing allow triggered or continuous read-out

#### **Sensor performances**

- » Low fake-hit rate: «10-6 hits/pixel/event
- » Radiation tolerance:
  - TID: > 270 krad
  - NIEL: >  $1.7 \cdot 10^{13}$  1 MeV n<sub>eq</sub>/cm<sup>2</sup>
- » Spatial resolution:  $\sim 5 \ \mu m$



#### **Sensor performances**

» Fake-hit rate measured during ITS2 commissioning: 10<sup>-10</sup> hits/pixel/event, after masking 100 noisy pixels over 10<sup>8</sup> total pixels





- » Noise pattern on ITS2 modules → <sup>210</sup>Pb radioactive decay from solder used to mount decoupling capacitors
  - Simulation demonstrated that β-particles from the <sup>210</sup>Bi (<sup>210</sup>Pb daughter) can penetrate the FPC and reach the sensor

J. Phys.: Conf. Ser. 2374 012062

## **Other ALPIDE applications**

#### » ALICE Muon Forward Tracker (MFT)

- Based on the same ALPIDE sensors
- Add vertex capability at forward muon arm





#### » ALICE Forward Calorimeter (FoCal)

- · Measure gluon density in proton/nuclei collisions at small x and Q value
- To be installed during LHC LS3
- ALPIDEs used to provide spatial resolution in the FoCal-E





## **Other ALPIDE applications**

#### » sPHENIX MVTX @RHIC

• Replica of the ITS2-IB detector



#### ... and many more, also in medical applications

#### Technology improvements: toward fully depleted sensor

- » Standard process: partially depleted epitaxial layer
  → doesn't allow full charge collection by drift, mandatory for more extreme radiation tolerance
  - Operational up to 10<sup>13</sup> 1 MeV n<sub>eq</sub>/cm<sup>2</sup>



#### Technology improvements: toward fully depleted sensor

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  - Operational up to  $10^{13}$  1 MeV  $n_{eq}/cm^2$
- » **Modified** process: toward fully depleted epitaxial layer (still keepings small collection electrode)  $\rightarrow$ planar junction separated from the collection electrode in the epitaxial layer through a low dose deep *n*-type implant
  - Operational up to: 10<sup>14</sup> 1 MeV n<sub>eq</sub>/cm<sup>2</sup>



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## **ALPIDE** leap

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    - » **Modified with gap** process: a gap in the deep n-implant increases the lateral electric field at the pixel borders
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NIMA 871 (2017) 90–96 NIMA 958 (2020) 162404

epitaxial lave

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Optimisation in 65 nm CMOS: https://doi.org/10.22323/1.420.0083



epitaxial lave



Large dimension silicon pieces bent in cylindrical shape at ITS3 target radii





#### LICE3 developments



#### LICE3 developments



Letter of Intent for an ALICE ITS Upgrade in LS3: https://cds.cern.ch/record/2703140

#### **Tracking efficiency Pointing resolution** 100 **ITS2** standalone ITS2+TPC ITS<sub>2</sub> ITS3 ITS2+TPC (full MC) 80 ITS3 standalone pointing resolution $[\mu m]$ $10_{1}$ ITS3+TPC Lracking efficiency [%] ITS3+TPC (full MC) 60 Ð **ITS2** standalone 20 ITS2+TPC ITS3 standalone ITS3+TPC 10 0.1 0.2 0.3 0.5 0.05 0.1 0.2 0.3 0.5 20 30 0.05 2 3 10 1 5 Transverse momentum [GeV/c] Transverse momentum [GeV/c]

Improved pointing resolution and tracking efficiency for low momenta (×2 at all  $p_T$ )

.......................

#### Study of the enhancement of charm quarks in heavy-ion collisions



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#### Key ingredients

- » Wafer-scale chips (up to  $\sim 28 \times 10 \text{ cm}^2$ )
  - $\rightarrow$  fabricated using stitching (to connect metal traces)
- » MAPS sensor based on 65 nm CMOS technology
  - $\rightarrow$  TPSCo largest (300 mm) wafer in this node
  - $\rightarrow$  potentially smaller pixel size (with same in-pixel integrated electronics)
  - $\rightarrow$  potentially low power consumption
- » Chips bent in cylindrical shape
  - $\rightarrow$  sensor thickness  $\leq$  50 µm
  - $\rightarrow$  ultra light carbon foam structures
- » Air cooling
  - $\rightarrow$  power consumption limits to be established

The whole detector will comprise six chips and barely anything else!

#### LICE3 developments





65 nm CMOS



Stitching technique



**Bending silicon** 

#### LICE3 developments



#### 65 nm CMOS

ALICE Inner Tracking System Upgrade: characterization of first chips fabricated in 65 nm CMOS technology (A. Trifirò) Wed. 17:00 - E1 session



Stitching technique

The ALICE Inner Tracking System Upgrade (V. Sarritzu) Wed. 11:20 - D1 session



**Bending silicon** 

ALICE ITS3: how to integrate a large dimension MAPS sensor in a bent configuration detector (D. Colella) Wed. 12:20 - D1 session

## 65 nm CMOS technology qualification

- » First test structures submission (MLR1) for 65 nm in December 2020
  - 10 transistor test structures (3 x 15 mm<sup>2</sup>)
  - 60 chips (1.5 x 1.5 mm<sup>2</sup>)
    - Analog and digital blocks
    - Pixel prototype: APTS, CE65, DPTS
- » Main goals:
  - Learn technology features
  - Characterise charge collection
  - Validate radiation tolerance
- » Testing since September 2021
  - Huge effort shared among many institutes
  - Laboratory tests with <sup>55</sup>Fe source
  - Beam tests @ PS, SPS, Desy, MAMI







- 6x6 pixel matrix
- Direct analogue readout of central 4x4
  submatrix
- Two types of output drivers:
  - 1. Traditional source follower (APTS-SF)

**APTS** 

DPTS

- 2. Very fast OpAmp (APTS-OA)
- 4 pixel pitches: 10, 15, 20, 25 μm



- 1. AC-coupling
- 2. DC-coupling
- 3. Source follower
- 3. Source follower
- 2 pixel pitches: 15, 25 µm



- Asynchronous digital readout
- Time-over-threshold information
- Pixel pitch: 15 µm
#### p ITS3 developments ALICE3 develo

#### 65 nm CMOS technology qualification



»Moving from *Standard* to *Modified with gap* process, the fraction of charge collected by the seed pixel increases »Moving from Standard to Modified with gap process, the efficiency degrading limit (< 99%) moves to higher threshold</p>



#### ITS3 developments AL

#### 65 nm CMOS technology qualification

#### » Pixel pitch

→ For modified with gap process charge collection doesn't depend on pixel pitch (10, 15, 20 and 25 µm)

#### » Radiation hardness

- $\rightarrow$  full digital sensor implementation does satisfies ALICE ionising (10 kGy) and nonionising (10<sup>13</sup> 1 MeV n<sub>eq</sub> cm<sup>-2</sup>) dose for LHC Run 4
- $\rightarrow$  can be operated at the temperature of +20°C (99% efficiency) after 10<sup>15</sup> 1 MeV  $n_{eq}$  cm<sup>-2</sup> and inefficiency comes from particle track away from the collection diode

## 65 nm CMOS TPSCo technology fully validated for ALICE application!

## \_PIDE leap ITS3 developments ALICE3 developments

#### Wafer-size sensors: 2D stitching

- » Chip size limited by field of exposure of photolithography equipment (~20 x 20 mm<sup>2</sup>)
- » Stitching technique allow sensor size exceeding the photolithography limitations
  - Building blocks are integrated in the photolithography mask as different mask regions
  - During photo-lithographic patterning, wafers are selectively exposed onto adjacent locations according to a pre-established pattern → very accurate translation and alignment required
  - Metal traces are used to create connections (power distribution and buses for control/data readout) across adjacent matrices (repeated units)

ц	Electronics	TR
L-drive	<i>r</i> by s PIXELS	R-drive
BL	Readout	BR

Sketch of an image sensor design



Isolated building blocks put separately on the reticle

Ţ	Electronics	Electronics	Electronics	TR
L-drive	r by s PIXELS	r by s PIXELS	r by s PIXELS	R-drive
L-drive	r by s PIXELS	r by s PIXELS	r by s PIXELS	R-drive
ВL	Readout	Readout	Readout	BR

Extending the size of the sensor beyond the reticle field of view

Tower Semiconductor Ltd, Stitching design rules for forming interconnect layers, US Patent 6225013B1 (2001)

#### **LPIDE** leap

#### **ITS3 developments**





#### Wafer-size sensors: 2D stitching

- » Two stitched sensor prototypes (ER1):
  - Monolithic Stitched Sensor (MOSS)
    - Size: 1.4 x 25.9 cm<sup>2</sup> 6.72 MPixels
    - Pitches: 22.5 x 22.5  $\mu m^2$  and 18 x 18  $\mu m^2$
    - Conservative design: separated powered sub-matrices
  - Monolithic Stitched Sensor with Timing (MOST)
    - Size: 0.25 x 25.9 cm<sup>2</sup> 0.9 MPixels
    - Pitch: 18 x 18 µm<sup>2</sup>
    - More dense design: global power network
- » Primary goals
  - Learn stitching technique to make a particle detector
  - Interconnect power and signals on wafer scale sensor
  - Learn about yield





#### **ITS3 developments**

#### Wafer-size sensors: 2D stitching



## p ITS3 developments ALICE3 developments

#### Wafer-size sensors: 2D stitching

#### » MOSS qualification

#### • First successful contact and readout on May!

- using dedicated probe card on wafer

#### • First operation in a telescope under beam in August!

- correlation with reference planes already visible







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ITS3 developments

Wafer-size sensors: 2D stitching

## Really exciting initial results from first stitching sensor!

» Path to the final sensor for ITS3:

- ER1 validation during 2023
- submission of ER2, compliant with ITS3 requirements, beginning 2024
- submission of final sensor (ER3) in 2025



#### **ITS3 developments**

## **Bending effect on MAPS**



- » Laboratory and test beam measurements (Jun 2020) allow to conclude that chip (180 nm CMOS) performance doesn't change after bending
  - Pixel matrix threshold distribution does not change when sensor is bent
  - Efficiency above 99.9% at a threshold of 100 e-



#### leap ITS3 developments



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## ALPIDE leap ITS3 developments ALICE3 development

## **Bending effect on MAPS**

- » Comparison between flat and bent MLR1 (65 nm) sensors (both APTS and DPTS) ongoing
  - · Bending procedure developed and proximity board adapted to bent configuration
  - Few samples prepared and under measurements in laboratory with <sup>55</sup>Fe source



## ALPIDE leap ITS3 developments ALICE3 developments



ALICE3: a silicon sensor based experiment



A next generation LHC HI (soft-QCD experiment) giving unprecedented insight into QGP



#### **Compact all-silicon nearly massless detector!**

- » Core will be a 70 m<sup>2</sup> MAPS tracker
  - innermost layers based on wafer-scale silicon sensors in vacuum and retractible
  - outer tracker based on modules
- » Extensive particle identification, including time-of-flight based detector
  - silicon based sensor with timing resolution of ~20 ps
  - technology choices include MAPS

Expression of Interest (2019): <u>https://arxiv.org/abs/1902.01211</u> Lol (2022) [LHCC-2022-009]: <u>https://cds.cern.ch/record/2803563?ln=fr</u>

#### ALPIDE leap ITS3 developments ALICE3 developments



Total MAPS surface ~70 m<sup>2</sup>



#### LEGO like interlocking concept





- » Stave based layers, like ITS2, but one order of magnitude larger surface
- » Module (O(10 x 10 cm<sup>2</sup>)) concept based on industry-standard processes for assembly and testing
- » Basic requirements
  - large coverage: ±4η
  - high-spatial resolution:  $\approx 10 \ \mu m$
  - very low material budget X/X<sub>0</sub> (per layer):  $\approx 1\%$

## ALPIDE leap ITS3 developments ALICE3 developments

#### **Inner tracker - IRIS tracker**

- » Based on wafer-scale, ultra-thin, curved MAPS
- » Basic requirements
  - radial distance from interaction point: 5 mm (inside beam pipe, retractible configuration)
  - unprecedented spatial resolution: ≈ 2.5 µm
  - unprecedented low material budget X/X<sub>0</sub> (per layer):  $\leq 0.1\%$
  - radiation tolerance:  $\approx 10^{16}$  1 MeV n<sub>eq</sub>/cm<sup>2</sup> + 200 Mrad
  - hit rates up to: 94 MHz/cm<sup>2</sup>
- » R&D will largely leverage on the ITS3 developments and push improvements on a number of fronts



# ALICE3 developments **Inner tracker - IRIS tracker** 4 x Petals Single petal Sensors (Layers and disks)

Carbon foam

and cold plate

Secondary

vacuum case



## ALPIDE leap ITS3 developments ALICE3 developments

## **Timing performance for TOF**

- » TOF separation power  $\propto L/\sigma_{TOF}$ • distance and time resolution crucial
- » 2 barrel + 1 forward layers
  - outer TOF at R ≈ 85 cm
  - inner TOF at R ≈ 19 cm
  - forward TOF at z ≈ 405 cm
- » Sensor basic requirements
  - timing resolution: ≈ 20 ps
  - material budget X/X<sub>0</sub> (per layer): 1-3%
  - power consumption: < 50 mW/cm<sup>2</sup>



Total TOF surface ~45 m<sup>2</sup>



- Timing resolution:  $\approx$  20 ps only for photons
- Feasibility to be demonstrated with charged particles



- Timing resolution of  $\approx 30~ps$  demonstrated with 50  $\mu m$  up to (1-2)  $10^{15}~1~MeV~n_{eq}/cm^2$
- Thinner LGADs produced by different manufacturers



- Advantages: low material budget, high SNR
- Investigation on innovative design to proof timing performance

## ALPIDE leap ITS3 developments ALICE3 developments

## **Timing performance for TOF - MAPS**

» Several monolithic projects targeting enhanced timing resolution



Y. Degerli et al., 2020 JINST 15 P06011



G. Iacobucci et al., 2019 JINST 14 P11008



T. Kugathasan et al., Nucl. Inst. Meth. A Vol. 979, Nov. 2020

» Project with application in ALICE

#### **ARCADIA** sensor

- Developed between INFN and LFoundry
- 110 nm CMOS, 6 metal layers
- Adding gain layer (gain 10-20) to reach **20 ps** resolution
- First prototype received in January 2023
  - pixel size: 250 x 100 μm<sup>2</sup>
  - diode area: 220 x 70 μm<sup>2</sup>
  - sensor capacitance: 127 fF
  - electronics size: 280 x 8 µm<sup>2</sup>
  - active thickness: 50  $\mu m$
- Test beam campaign ongoing, results in Q4 2023



#### Summary

#### CMOS sensors in 180 nm technology successfully used for trackers

- used in ALICE (ITS2, MFT), sPHENIX and considered for other experiments (modified process)
- limited by slow charge collection
- process modification needed  $\rightarrow$  many development ongoing

#### Future developments rely on wafer scale sensors (ITS3, ALICE 3)

- 65 nm TPSCo technology validated
- first successful contact and readout of ER1 stitched sensor prototype (MOSS)
- next stitched sensor submission (ER2), ITS3 requirements compatible, in preparation

#### Extensive R&D ongoing

- bending of wafer scale sensors
- characterization of 65 nm bent structures
- mechanical support and cooling studies
- conceptual design of industry-standard processes for module assembly and test
- MAPS with high timing performance development



## Evolution of the ALICE Inner Tracking System from LHC Run1 to the future





ALICE 3 Tracker + IRIS

Detector	Technology	Innermost layer radius (cm)	$X/X_0$ (%) for lighter layer	Total surface (m <sup>2</sup> )	Operation
SPD	hybrid	3.9	1.14	0.21	Run 1+2
ITS2 + MFT	MAPS	2.2	0.35	O(10)	Run 3 + (4)
ITS3	MAPS	1.8	<0.1	0.24	Run 4
ALICE 3 tracker + IRIS	MAPS	0.5 (closed)	<0.1	O(70)	> Run 4

#### Hybrid vs Monolithic sensors

#### Characteristics of a sensor for tracking/vertexing

- » High space point resolution (~10  $\mu$ m)
- » High detection efficiency (~100%) and low fake-hit rate
- » Low material budget (< 0.1%)
- » Low power density ( $\rightarrow$  material budget  $\uparrow$
- » Time resolution
- » Radiation hardness (HL-LHC ~2×10<sup>16</sup> 1 MeV n<sub>eq</sub>/cm<sup>2</sup>)



#### **First MAPS based HEP detector**

- » First application of MAPS technology in a collider environment for STAR HFT PXL detector @RHIC/BNL (2014) → Mimosa28
  - developed by IPHC Strasbourg
  - pixel sizes: 20.7 × 20.7  $\mu$ m<sup>2</sup>
  - matrix: 928 × 960 pixels (890k)
  - CMOS technology: twin well, AMS 0.35 μm
  - readout: rolling-shutter fashion in 185.6 µs
  - power budget: 170 mW/cm<sup>2</sup>





http://dx.doi.org/10.3204/DESY-PROC-2014-04/83

#### Technology improvements: toward fully depleted sensor

Four splits implemented in the 65 nm MLR1

- **split 1** with the standard process without modifications
- **split 2** with first modification of the deep p-well to improve isolation between circuitry and sensor to prevent punch-through between deep n-well and circuitry,
- **split 3** adding to split 2 deep n-well adjustment in the pixel to allow full depletion
- split 4 adding to split 3 an additional deep p-well modification to prevent potential wells created by the additional in-pixel circuitry



https://doi.org/10.22323/1.420.0083

## 65 nm CMOS technology: first prototypes characterization



- 2. Very fast OpAmp (APTS-OA)
- 4 pixel pitches: 10, 15, 20, 25 μm

»Moving from *Standard* to *Modified with gap* process, the fraction of charge collected by the seed pixel increases



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### 65 nm CMOS technology: first prototypes characterization



• 4 pixel pitches: 10, 15, 20, 25 μm

»For *Modified with gap* process charge collection doesn't depend on pixel pitch

#### <sup>55</sup>Fe signal amplitude for different pixel pitch



## 65 nm CMOS technology: first prototypes characterization



DPTS

- 32x32 pixel matrix
- Asynchronous digital readout
- Time-over-threshold information
- Pixel pitch: 15 µm

» Non-ionising irradiation leads to a decrease in the detection efficiency

#### **Detector efficiency and FHR for different irradiation level**



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Gianluca Aglieri Rinella et al. arXiv:2212.08621v2

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#### **Detector efficiency and FHR for different irradiation level**



### 65 nm CMOS technology: first prototypes characterization



Beam: 5.4 GeV/c electrons Trigger by scintillators or one of the two DPTS



#### **DPTS timing resolution**

» Time residual distributions of two DPTSs with no corrections (blue) and with readout scheme and time walk corrections applied (orange)

» Timing resolution:

 $\sigma_{gauss}/\sqrt{2} = 6.3 \pm 0.1 \text{ ns}$ 

» FE parameters not optimised for timing performance (I<sub>bias</sub> = 10 nA)

#### 65 nm CMOS technology: first prototypes characterization



- 1. Traditional source follower (APTS-SF)
- 2. Very fast OpAmp (APTS-OA)
- 4 pixel pitches: 10, 15, 20, 25 μm

#### APTS-OA timing response: standard vs modified with gap



» Fast readout allows to estimate the charge collection time via signal fall time

» In *modified with gap* process charge collection is faster and amplitude in larger

#### 65 nm CMOS technology: first prototypes characterization



APTS

6x6 pixel matrix Direct analogue readout of central 4x4

submatrix

- Two types of output drivers:
  - 1. Traditional source follower (APTS-SF)
- 2. Very fast OpAmp (APTS-OA)
- 4 pixel pitches: 10, 15, 20, 25 μm



#### **APTS-OA** timing response

#### » CFD Time stamp $t = t_{10\% CFD}$

- » Time difference  $\Delta t = t_{OPAMP1} t_{OPAMP0}$ distribution fitted with a Gaussian function
- »Efficiency on both OPAMP plane ~99% (at threshold 5.5 mV = 150e)
- » Time resolution: 77 ± 5 ps without time walk/jitter corrections

### **R&D** activities - ALPIDE chip bending

- » MAPS at thickness used in current detectors (~50 µm) are quite flexible
- » Large benefit from going even a bit thinner: the bending force scales with thickness to the third power
- » The breaking point moves to smaller bending radii when going thinner
- » Project goal thicknesses and desired bending radii are in a "not breaking" regime


## **R&D** activities - Wafer-scale silicon bending

» Developed procedure allows silicon bending in a repeatable reliable way
» Bending tool: tensioned mylar foil wrapping around a cylindrical mandrel



### **R&D** activities - Carbon foam characterisation

» Different foams characterised for machinability and thermal properties







#### Fleece to reduce glue



#### **R&D** activities - Carbon foam characterisation







- » Analysis of the kink angle distributions at the position of a scatterer
- » Material budget image: represents the widths of the scattering angle distribution of all particles traversing a given bin

# **R&D** activities - Layer assembly procedure

» Different options under study (including vacuum clamping)
» Currently working solution based on adhesive caption tape





## **R&D** activities - Layer assembly procedure

» Different options under study (including vacuum clamping)
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Wedges replaced with half-ring due to excessive deformation from cylindrical shape







#### Data taking strategy

#### » Record large minimum-bias data sample

- $\rightarrow$  read out all Pb-Pb interactions up to maximum LHC collision rate of 50 kHz (was ~1 kHz in the central barrel)
- $\rightarrow$  increase Pb-Pb Run 2 minimum-bias sample by factor 50-100

Colliding System	Integrated luminosity	Comment
Pb-Pb @ $\sqrt{S_{NN}}$ = 5 - 5.5 TeV	13 nb <sup>-1</sup>	Plus pp reference data
p-Pb @ √S <sub>NN</sub> = 8 - 8.8 TeV	0.6 pb <sup>-1</sup>	Plus pp reference data
pp @ √S = 14 TeV	200 pb <sup>-1</sup>	Focus on high multiplicity and rare signals

#### » Improve tracking efficiency and resolution at low- $p_T$

- $\rightarrow$  increase tracking granularity
- $\rightarrow$  reduce material thickness

#### » Preserve Particle IDentification (PID)

 $\rightarrow$  consolidate and speed-up main ALICE PID detectors

Programme is presented in CERN Yellow Report (<u>https://arxiv.org/abs/1812.06772</u>) Future high-energy pp programme with ALICE (<u>https://cds.cern.ch/record/2724925/files/ALICE\_HEpp\_PublNote.pdf</u>) <u>LHC schedule</u>







#### **Physics program**

- » Charm and beauty hadrons correlation over a wide rapidity range
- » Systematic measurements of multiply heavy-flavoured hadrons (expected enhanced production from the QGP)
- » Production and behaviour of the charmed exotic states in the QGP and their structure
- » Multi-differential measurements of electromagnetic radiation from the QGP (probe early evolution and restoration of chiral symmetry)
- » Measurements of net-quantum number fluctuations over a wide rapidity range (constrain susceptibilities of QGP and to test the realisation of a cross-over phase transition)

Expression of Interest (2019): <u>https://arxiv.org/abs/1902.01211</u> Lol (2022) [LHCC-2022-009]: <u>https://cds.cern.ch/record/2803563?ln=fr</u>