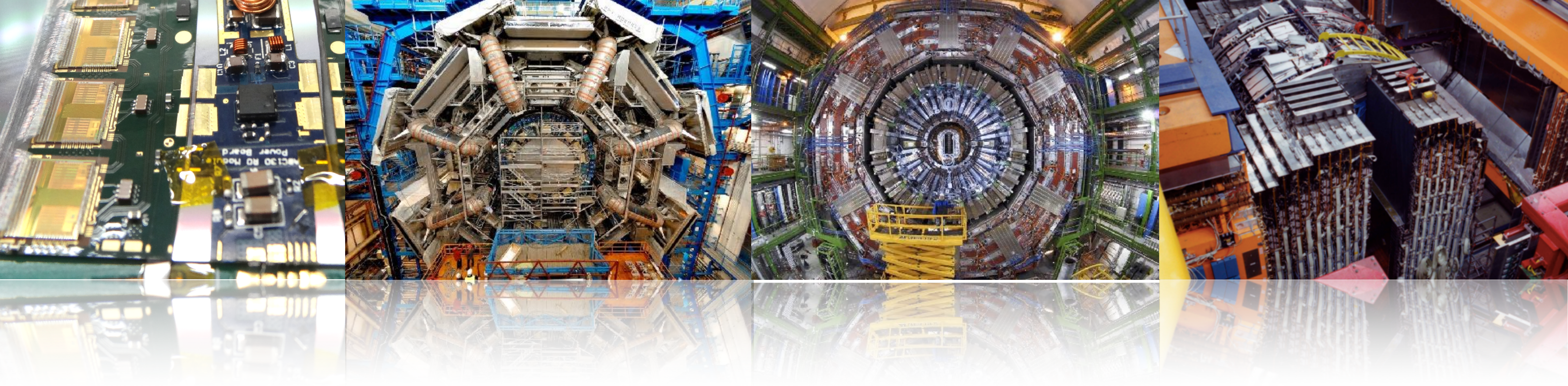

INTRODUCTION TO SILICON DETECTORS

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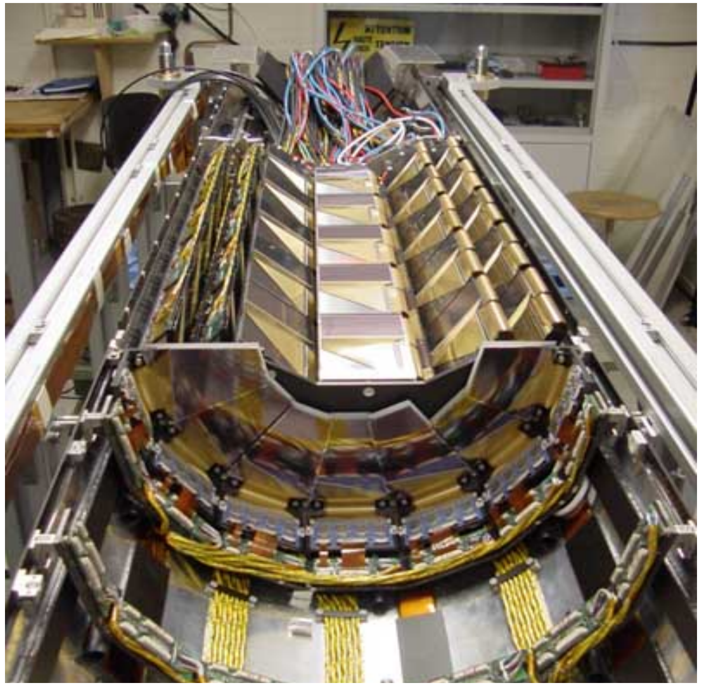
science & innovation
Department:
Science and Innovation
REPUBLIC OF SOUTH AFRICA
CERN
DESY
IJCLab Irène Joliot-Curie Laboratoire de Physique des 2 Infinis
NRF National Research Foundation
iThemba LABS Laboratory for Accelerator Based Sciences

INTRODUCTION

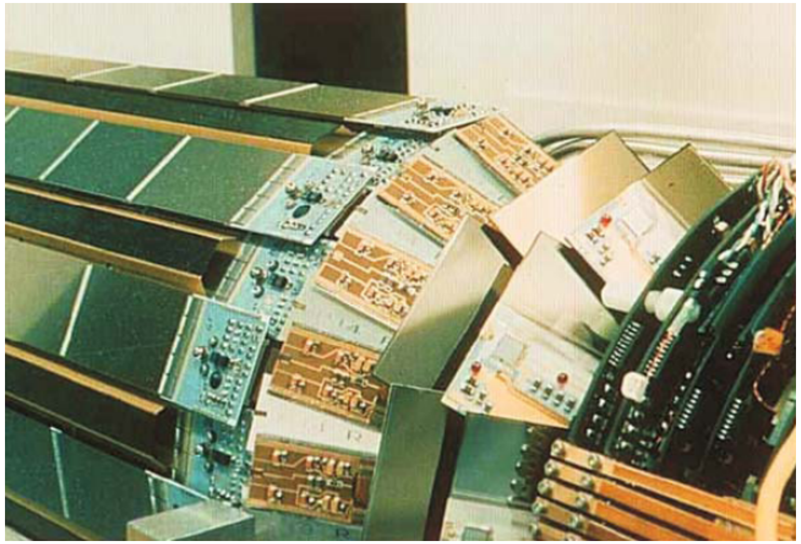
MOTIVATION

- Semiconductors have been used in particle identification for many years:
  - ~1950: Discovery that pn-Junctions can be used to detect particles.
- Semiconductor detectors used for energy measurements (Germanium).



ZEUS MVD 2000

- Since ~ 45 years: Semiconductor detectors for precise position measurements
  - precise position measurements possible through fine segmentation (10-100µm)
  - multiplicities can be kept small (goal:<1%)
- Technological advancements in production technology
  - developments for micro electronics



DELPHI VFT 1996

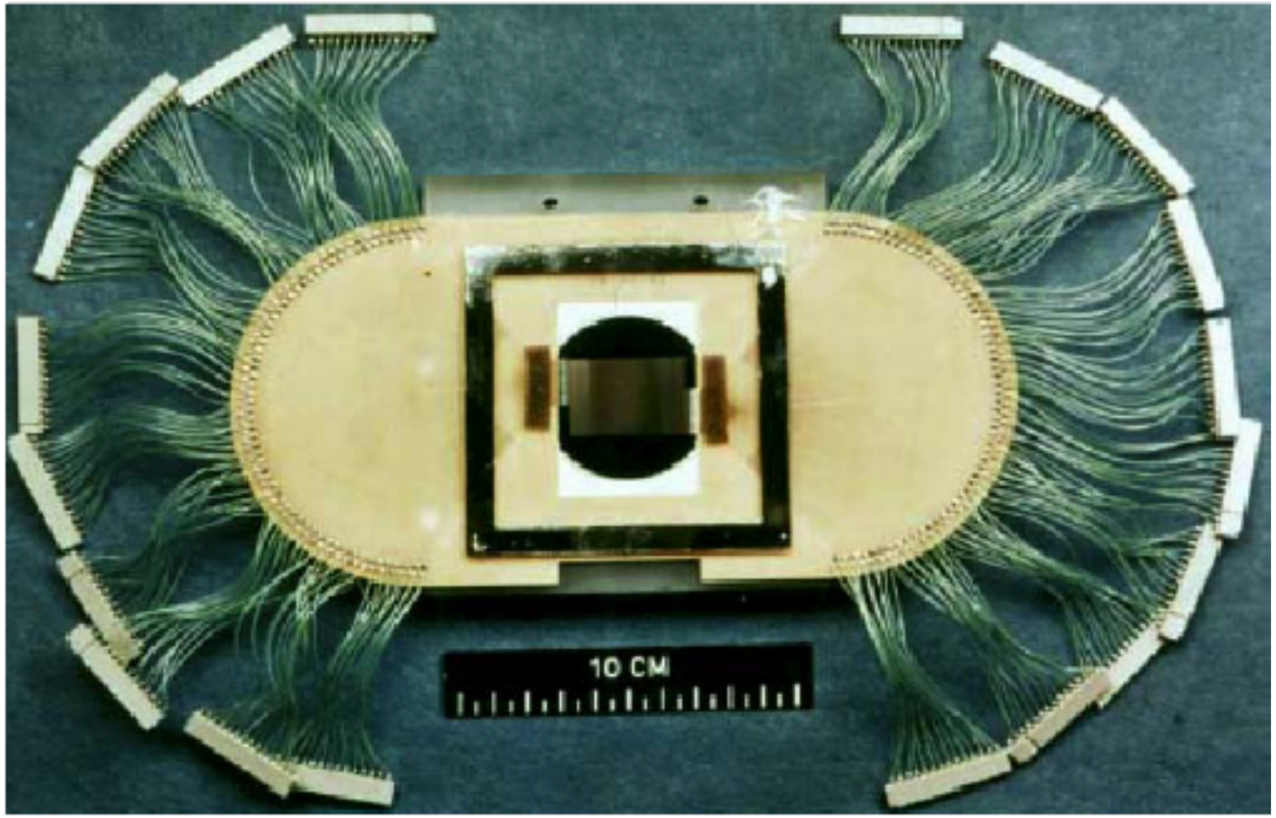
FIRST HEP APPLICATION: NA11

- After discovery of charm (1974), τ-lepton (1975) and beauty (1977) with lifetimes cτ ~100 μm: need fast (ns), and precise (μm) electronic tracking detectors

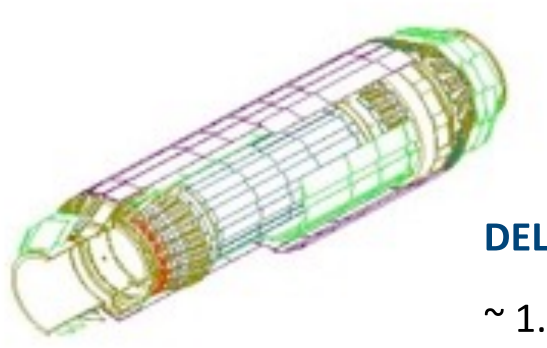
- Strip detector for NA11 in 1981
    - 1200 strip-diodes
    - 20 μm pitch
    - 60 μm readout pitch
    - 24 x 36 mm^2 active area ~0.01m^2
    - position resolution ~5.4 μm
    - 8 layer at the start

➔ precise track reconstruction

- readout electronic: **~1m^2**



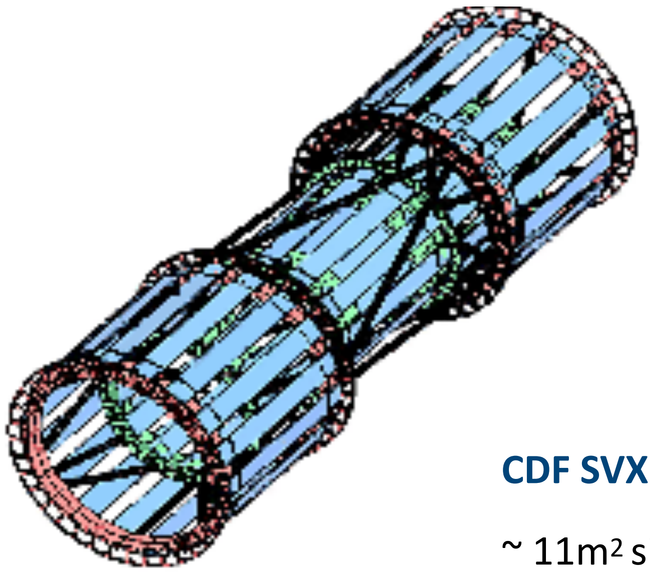
Large Silicon Systems



DELPHI (1996)

~ 1.8m^2 silicon area

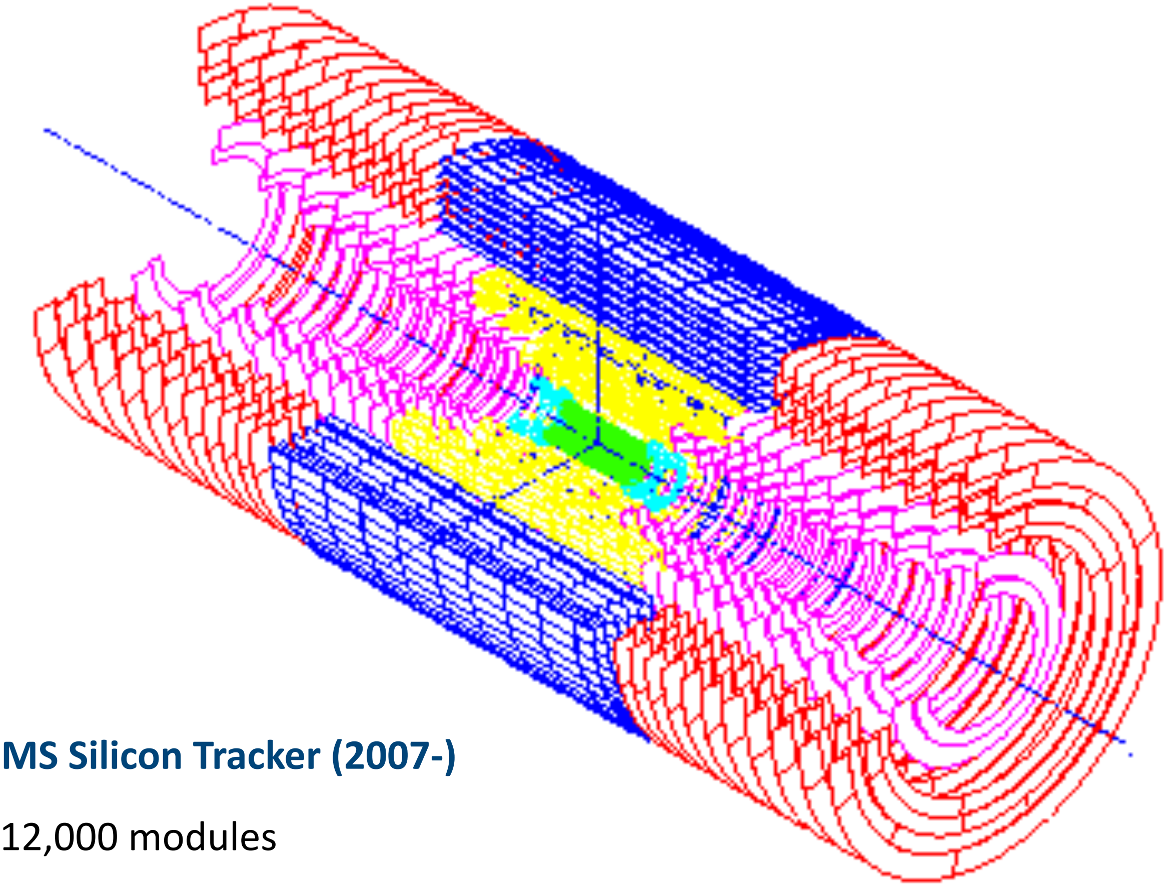
~ 175 000 readout channels



CDF SVX IIa (2001-2012)

~ 11m^2 silicon area

~ 750 000 readout channels



CMS Silicon Tracker (2007-)

~12,000 modules

~ 223 m^2 silicon area

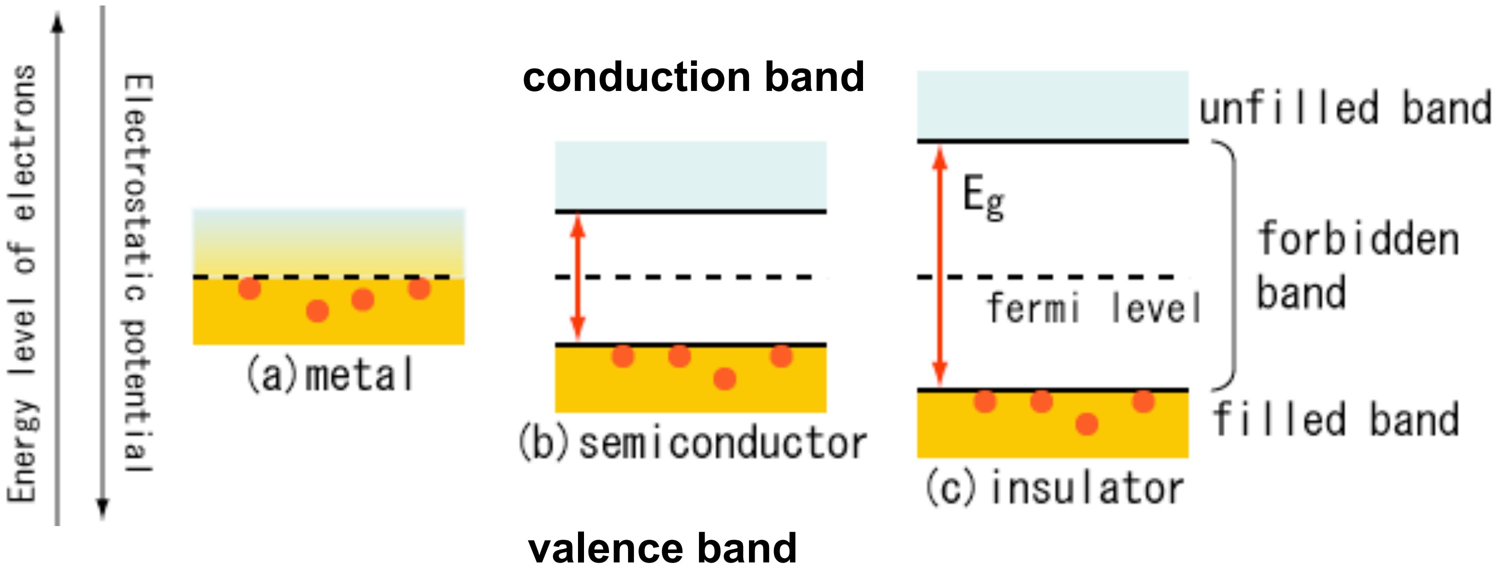
~25,000 silicon wafers

~ 10M readout channels

SEMICONDUCTORS

SEMICONDUCTOR BASICS

- In free atoms electron energy levels are discrete.
- In a solid, energy levels split and form a nearly-continuous band.



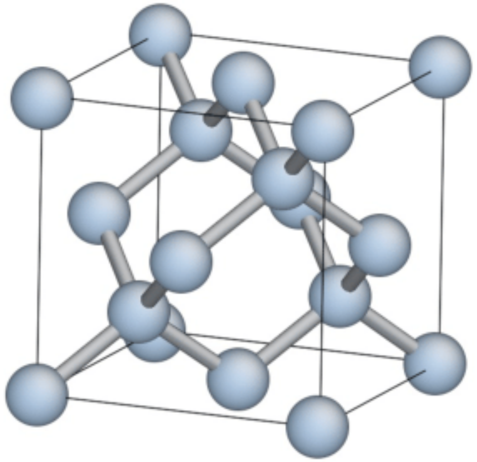
- Large gap: the solid is an insulator.
- No gap: it is a conductor.
- Small band gap: semiconductor

- For silicon, the band gap is 1.1 eV, but it takes **3.62 eV** to ionise an atom
  - Remaining energy goes to phonon excitations (heat).

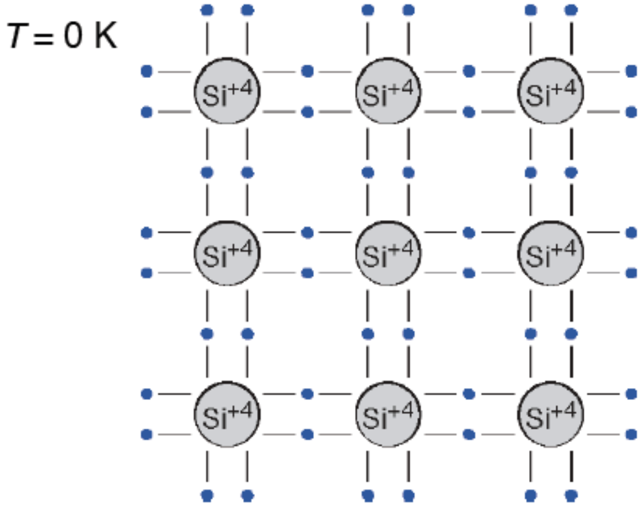
BAND MODEL FOR ELEMENTS IV (EXAMPLE FOR SI)

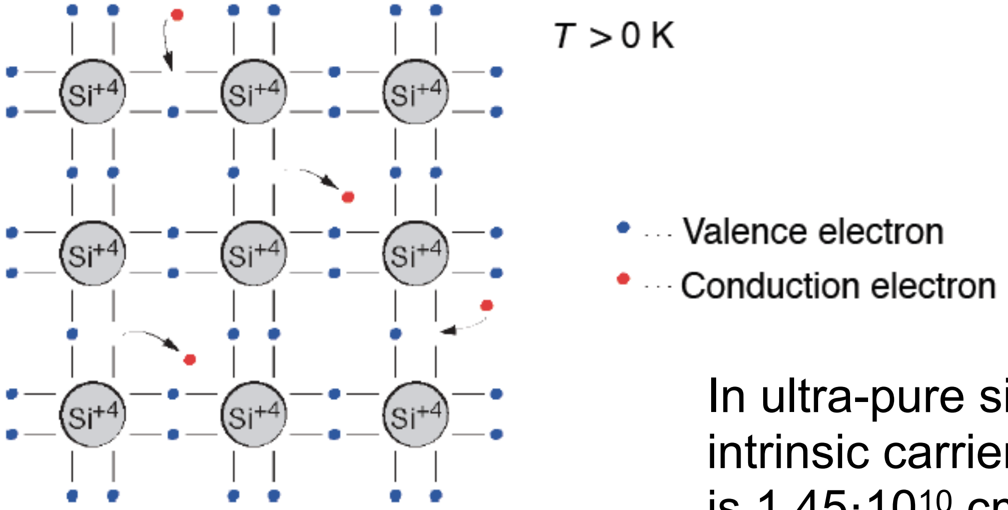
Each atom has 4 closest neighbours, the 4 electrons in the outer shell are shared and form covalent bonds.

- At low temperature all electrons are bound
- At higher temperature, thermal vibrations break some of the bonds
- Free electrons cause conductivity (electron conduction)
- The remaining open bonds attract other e- ➔ the “holes” change position (hole conduction)



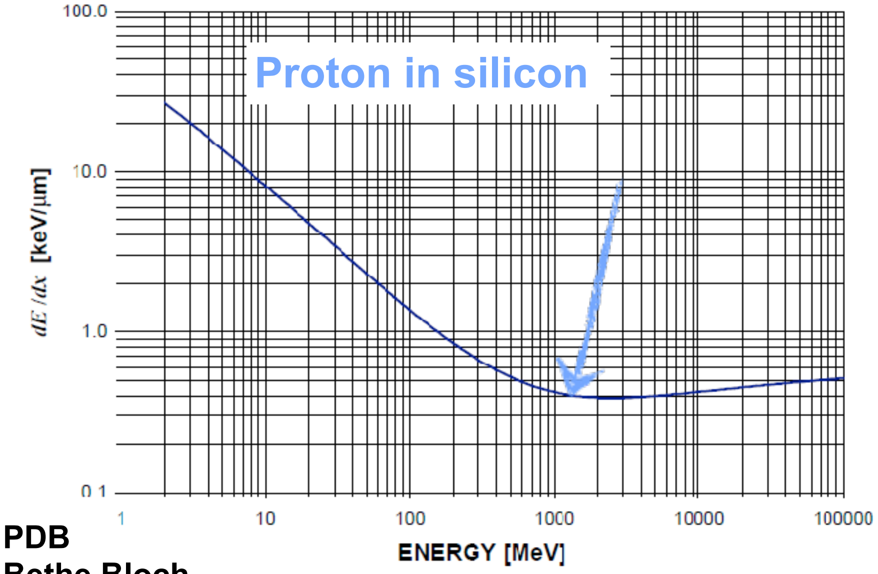
Crystal structure





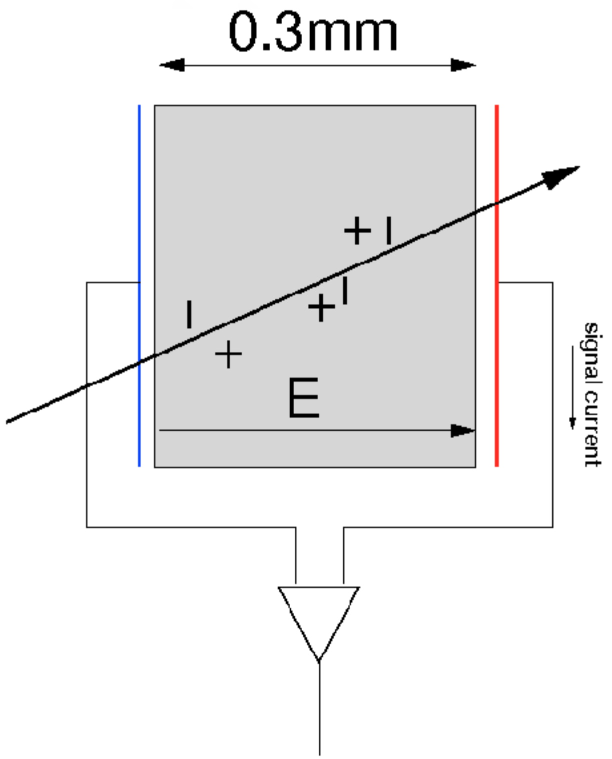
In ultra-pure silicon the intrinsic carrier concentration is $1.45 \cdot 10^{10}$ cm^{-3} at room temperature.

CONSTRUCTING A DETECTOR



PDB
Bethe Bloch

Si detector:
Thickness: 0.3 mm
Area: 1 cm^2



- Mean ionisation energy ***I_0* = 3.62 eV**
- Mean energy loss per flight path of a mip ***dE/dx* = 3.87 MeV/cm**

Signal of a mip in detector:

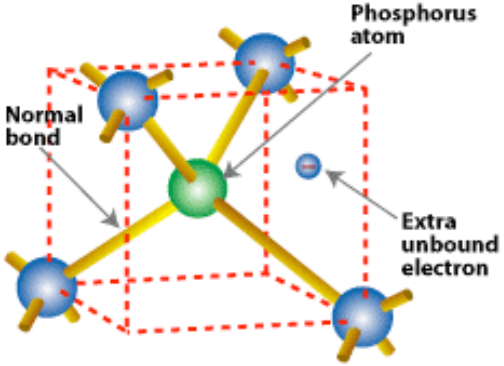
$$\frac{dE/dx\cdot d}{I_0}=\frac{3.87\cdot 10^{6}\,\mathrm{eV/cm}\cdot 0.03\,\mathrm{cm}}{3.62\,\mathrm{eV}}\approx 3.2\cdot \underline{10^{4}}\;\mathrm{e^{-}h^{+}-pairs}$$

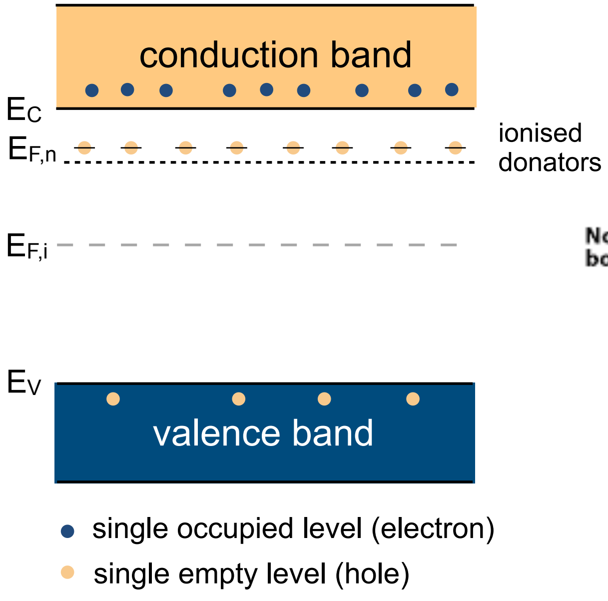
Intrinsic charge carrier in a volume of same thickness and A=1cm^2 (*T* = 300 K):

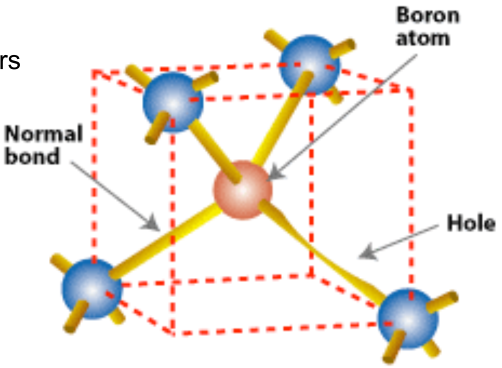
$$n_i\,d\,A=1.45\cdot 10^{10}\,\mathrm{cm^{-3}}\cdot 0.03\,\mathrm{cm}\cdot 1\,\mathrm{cm^{2}}\approx 4.35\cdot \underline{10^{8}}\;\mathrm{e^{-}h^{+}-pairs}$$

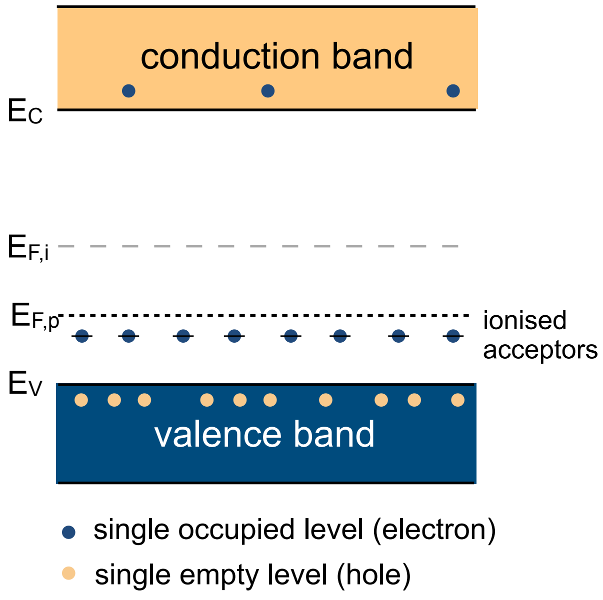
Result: The number of thermal created e–h+-pairs (noise) is four orders of magnitude larger than the signal

DOPING SILICON









n type semiconductor:

- **N**egative charge carriers (electrons) by adding impurities of donor ions (e.g. Phosphorus (type V))
- **Donors** introduce energy levels close to conduction band thus almost fully ionised (E_F closest to CB)

Electrons are the majority carriers.

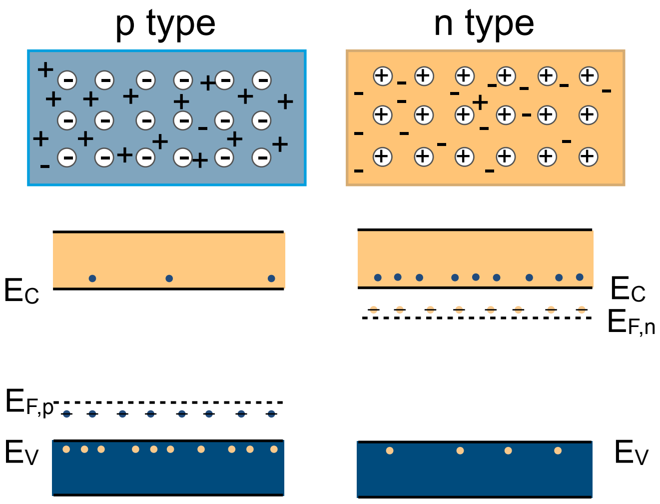
p type semiconductor:

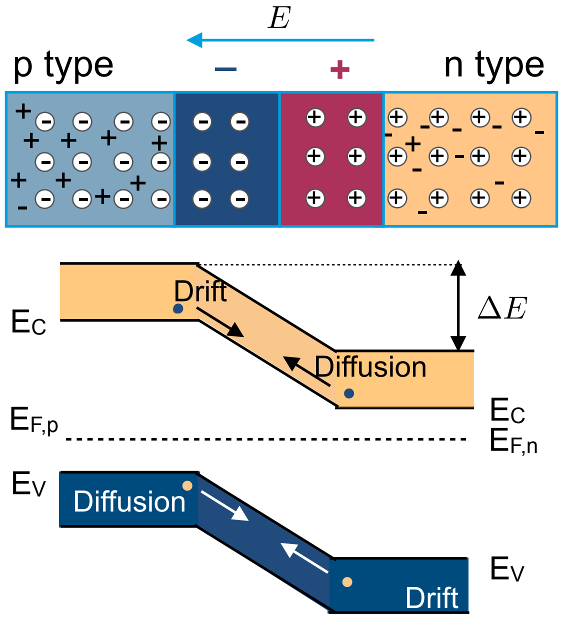
- Positive charge carriers (holes) by adding impurities of acceptor ions (e.g. Boron (type III)).
- Acceptors introduce energy levels close to valence band thus 'absorb' electrons from VB, creating holes (E_F closest to VB).

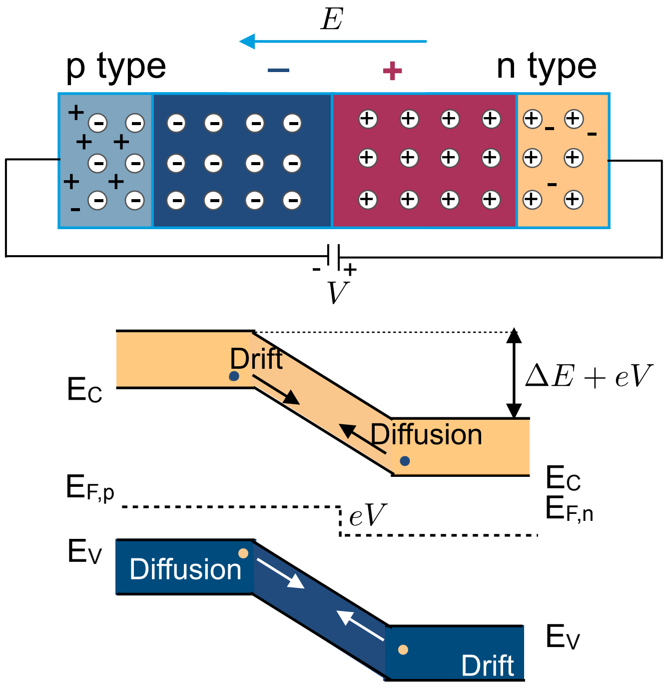
Holes are the majority carriers.

BASIS OF SILICON DETECTOR: PN JUNCTION

- At interface of p type and n type semiconductor diffusion of excessive carriers to the other material until thermal equilibrium
- Stable space charge region free of charge carriers: **depletion zone**.







Applying an external voltage V with the cathode to p and the anode to n (reverse biasing), e-h pairs are pulled out of the depletion zone. ➔ **larger depletion zone** ➔ suppress current across the junction

pn-junction with reverse bias

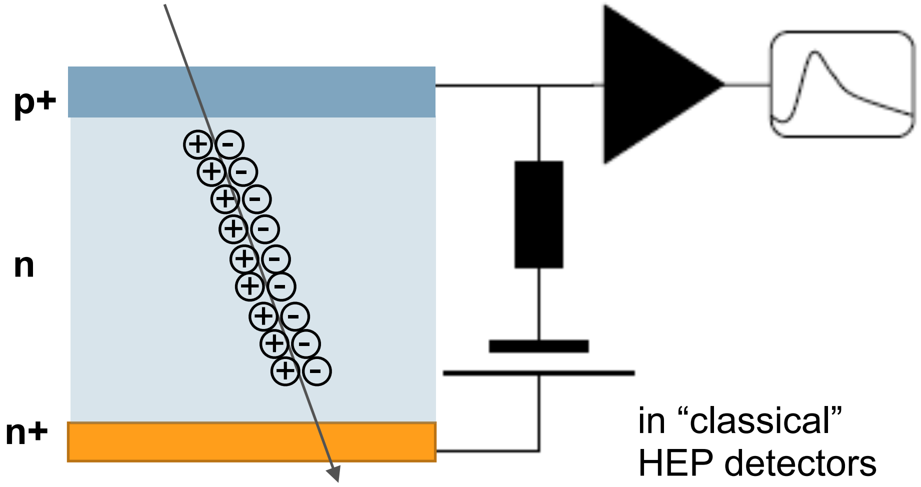
PRINCIPLE OF SEMICONDUCTOR DETECTORS

- Creation of electric field: voltage to deplete thickness d

with $n_A >> n_D$

$$d = \sqrt{\frac{2\epsilon\epsilon_0 V_{dep}}{e n_D}}$$

for $d = 300\mu m$: $V_{dep} \approx 160V$



in “classical” HEP detectors d=100-300 µm

Typical numbers

- Passage of a charged particle: Electron-hole pairs formed in the depletion zone
  - Drift under the influence of the electric field
  - Signal depends on width of depletion zone

> The signal is induced by the motion of charge after incident radiation (not when the charge reaches the electrodes).

Doping concentration

$n_A \approx 10^{19} cm^{-3}$	Acceptors
$n_D \approx 2 \cdot 10^{12} cm^{-3}$	Donators

ELEMENTAL SEMICONDUCTORS

	Si	Ge	GaAs	CdTe	Diamond	SiC
band gap	1.12	0.67	1.42	1.56	5.48	2.99
energy for e-p pair [eV]	3.6	2.9	4.2	4.7	13.1	6.9
e- for MIP (300µm)	24000	50000	35000	35000	9300	19000
Z	14	32	31+33	48+52	6	14+6

Germanium:

Needs cooling due to small band gap of 0.66 eV (liquid N_2 at 77 K) mainly used in nuclear physics: Very good energy resolution!

Silicon:

Can be operated at room temperature (band gap of 1.12 eV). Synergies with micro electronics industry. Standard material for detectors in high energy physics

Diamond

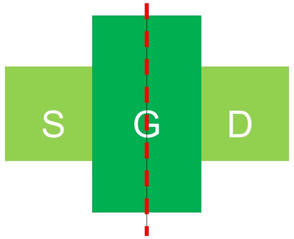
(CVD* or single crystal): Allotrope of carbon
Large band gap of 5.5 eV (requires no depletion zone)
Very radiation hard
Disadvantages: low signal and high cost

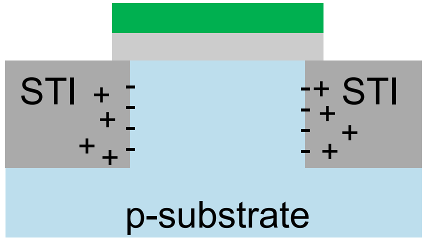
(*) CVD: Chemical Vapor Deposition

PROBLEM - RADIATION DAMAGES

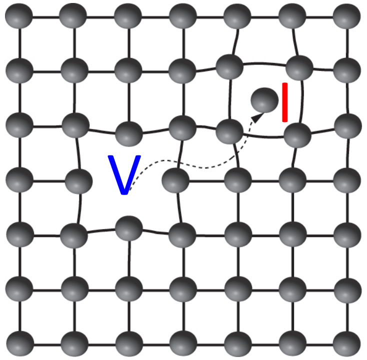
PROBLEM: RADIATION DAMAGE

In a nutshell!

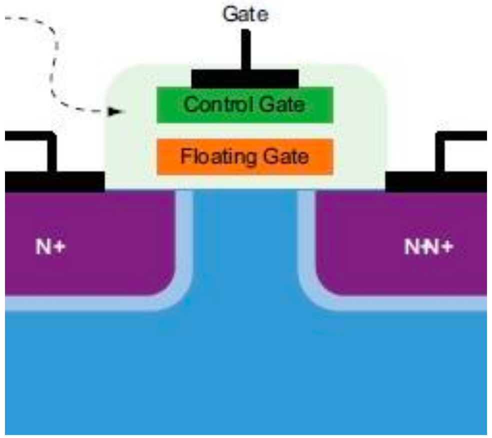




- Surface defects: **Total Ionising Dose (TID)**
  - mainly affect electronic circuits
- Bulk Damages: **Non Ionising Energy Loss (NIEL)**
  - mainly affect sensor like structures (pn junctions)



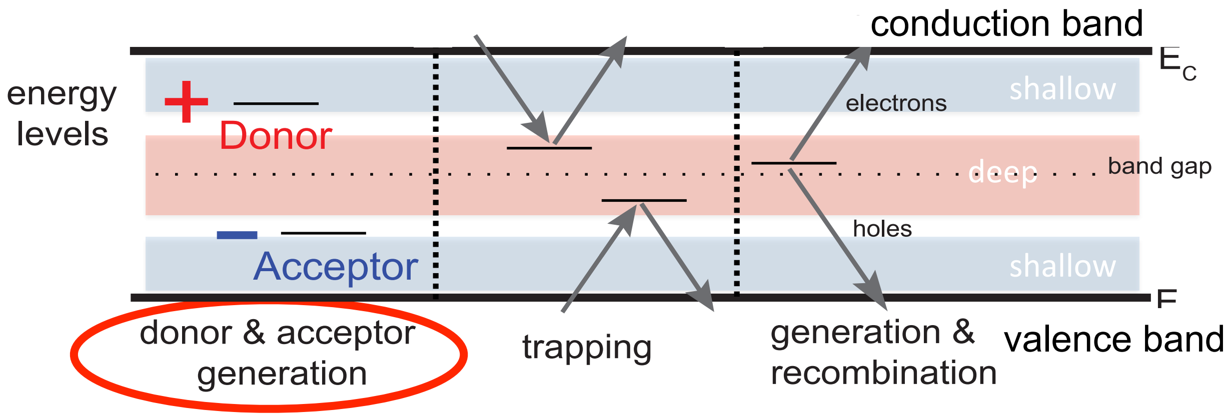
- **Single Event Effects (SEE)**
- **Transient Radiation Effects in Electronics (TREE)** associated with detonation of nuclear weapons



- **Radiation sensitive materials:**
  - semi-conductors
  - oxides
  - heavy elements at interconnections (W, Ta, Au, Pb, Pt, …)
  - but also all passive materials: glues, other important materials (not covered here)

RADIATION DAMAGE: MACROSCOPIC EFFECTS

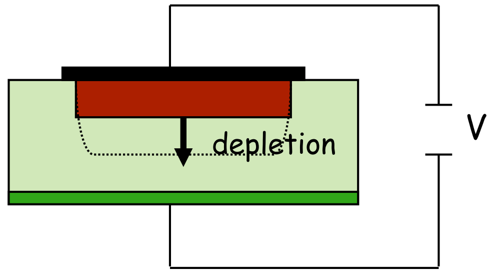
- Impact of defects on detector properties depends on defect level in band gap



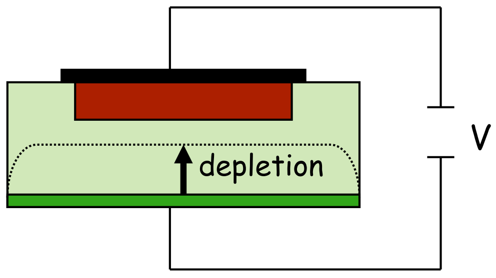
Donor&acceptor generation:
Change of effective doping concentration (N_{eff})

$$V_{dep} = d^2 N_{eff} \frac{q}{e\epsilon\epsilon_0}$$

- Increase of depletion voltage
- Under-depleted operation



Before type inversion

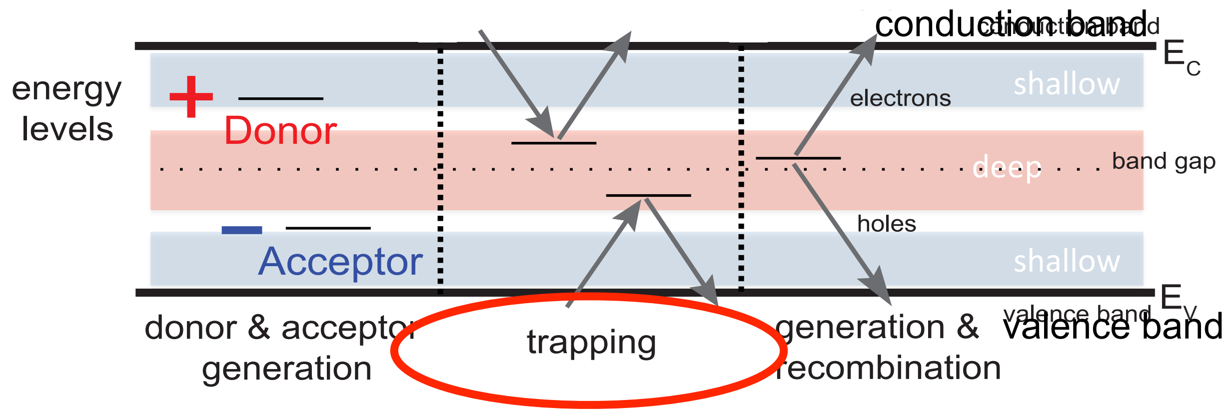


After type inversion

M. Moll, PhD thesis, Uni Hamburg 1999

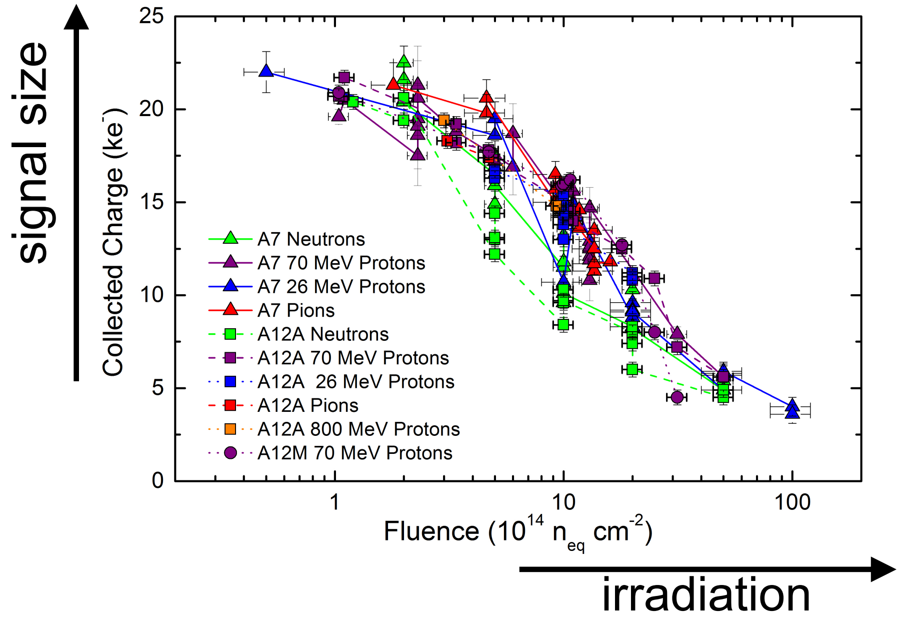
Radiation Damage: Macroscopic Effects

- Impact of defects on detector properties depends on defect level in band gap



Increased charge trapping

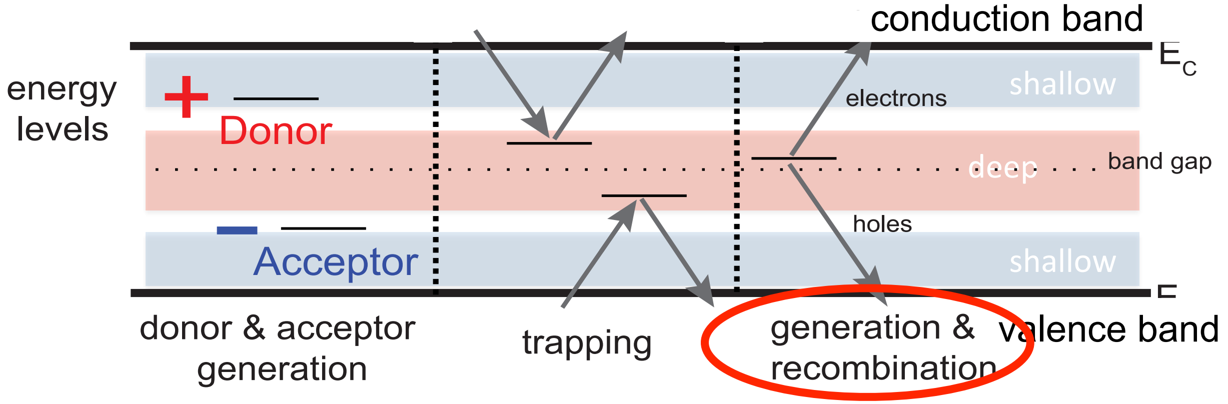
Lower signal (less charge)
Reduced charge collection efficiency



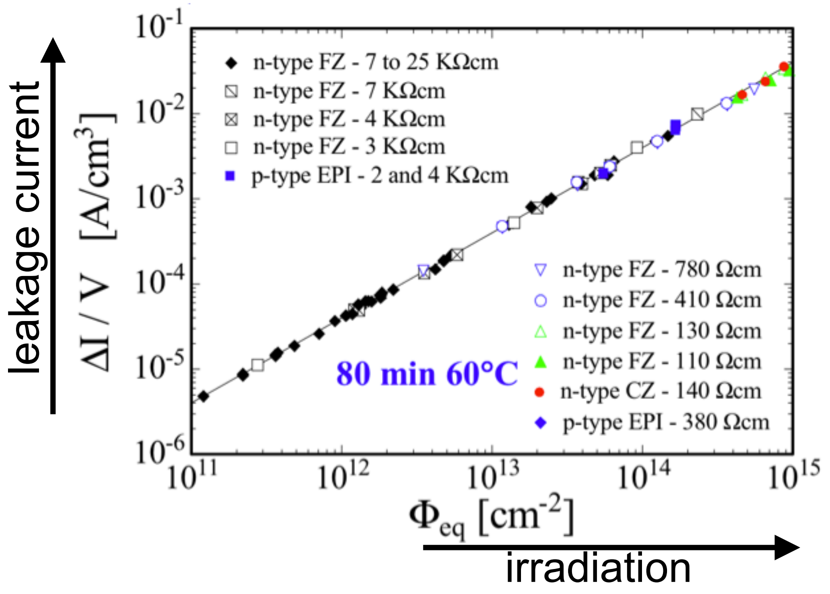
ATLAS ITk Strips TDR, April 2017

RADIATION DAMAGE: MACROSCOPIC EFFECTS

- Impact of defects on detector properties depends on defect level in band gap



Increase of leakage current
higher shot noise; thermal runaway
→ Cooling during operation helps
(leakage current depends on T)

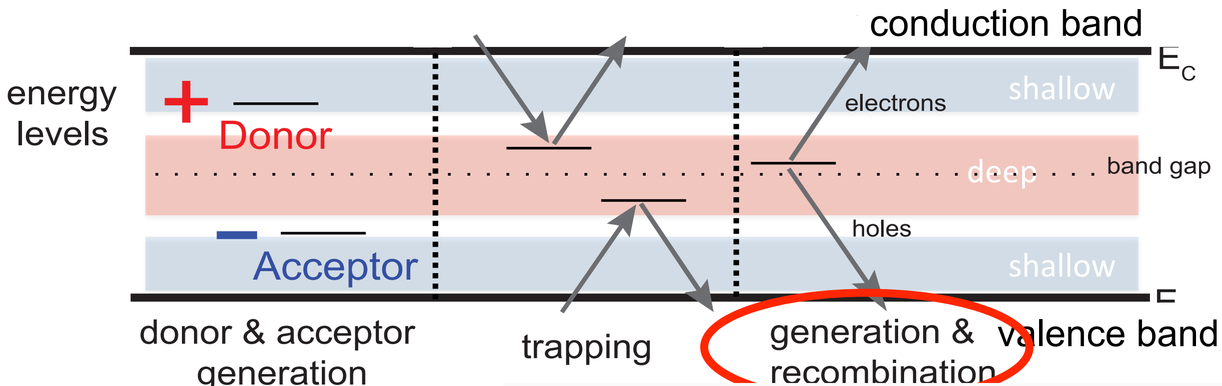


$$\alpha = \frac{\Delta I}{V \Phi_e}$$

α is constant over several orders of fluence and independent of impurity concentration in silicon

Radiation Damage: Macroscopic Effects

- Impact of defects on detector properties depends on defect level in band gap



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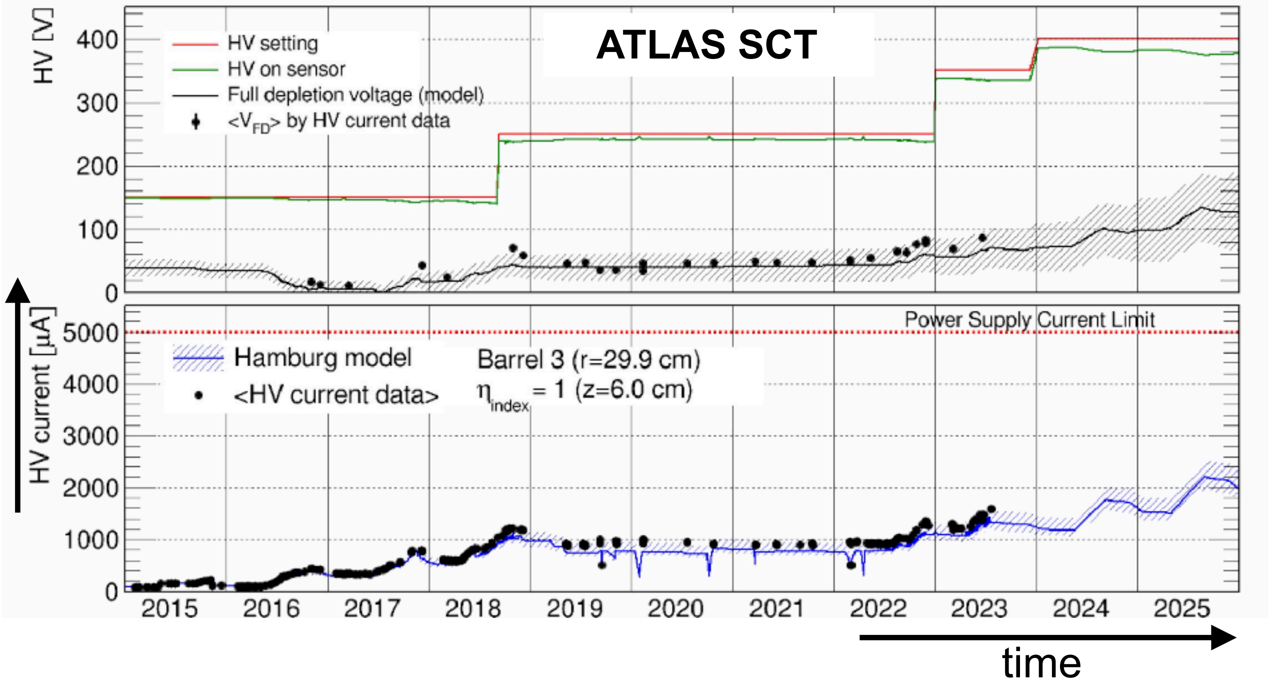
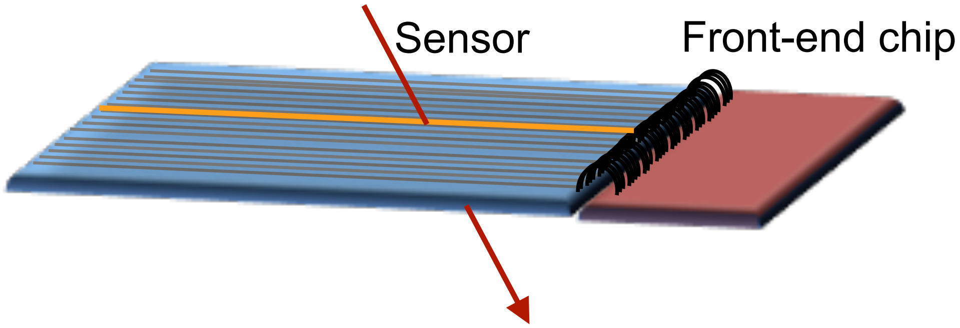
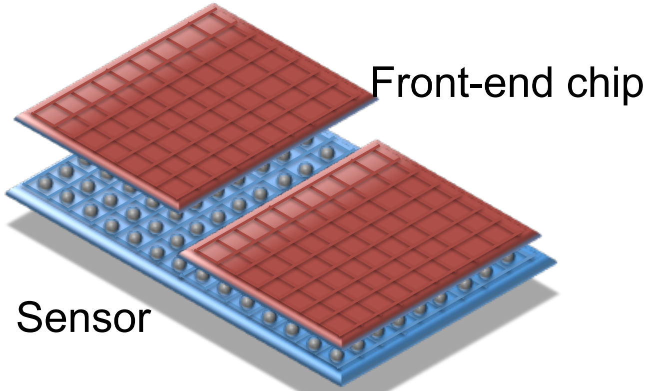


STRIPS AND PIXELS

- **Strips detector:** charge sensed by long narrow strips 1D information (typically 20 - 100µm)
  - 2D information by double sided processing or adding back to back second layer slightly rotated (stereo angle)
- In regions with higher track density one dimensional measurements can lead to ambiguities.



- **Pixel detector:** charge sensed by small pixels on one side of sensor
  - Hybrid pixels: sensors and readout joined via bump bonds
  - Monolithic pixels: sensor and readout on one substrate

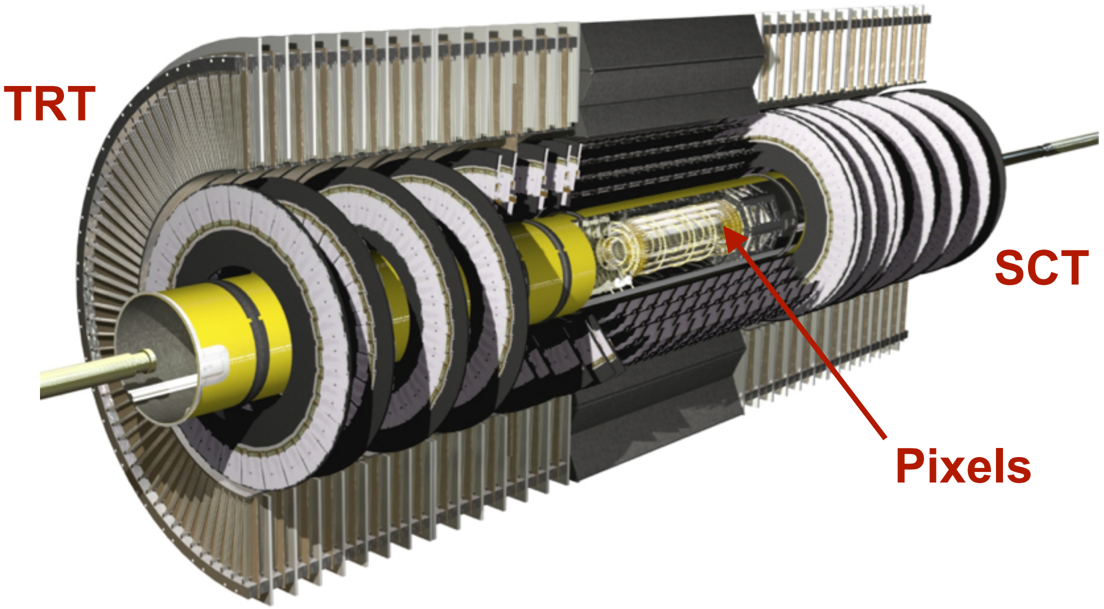


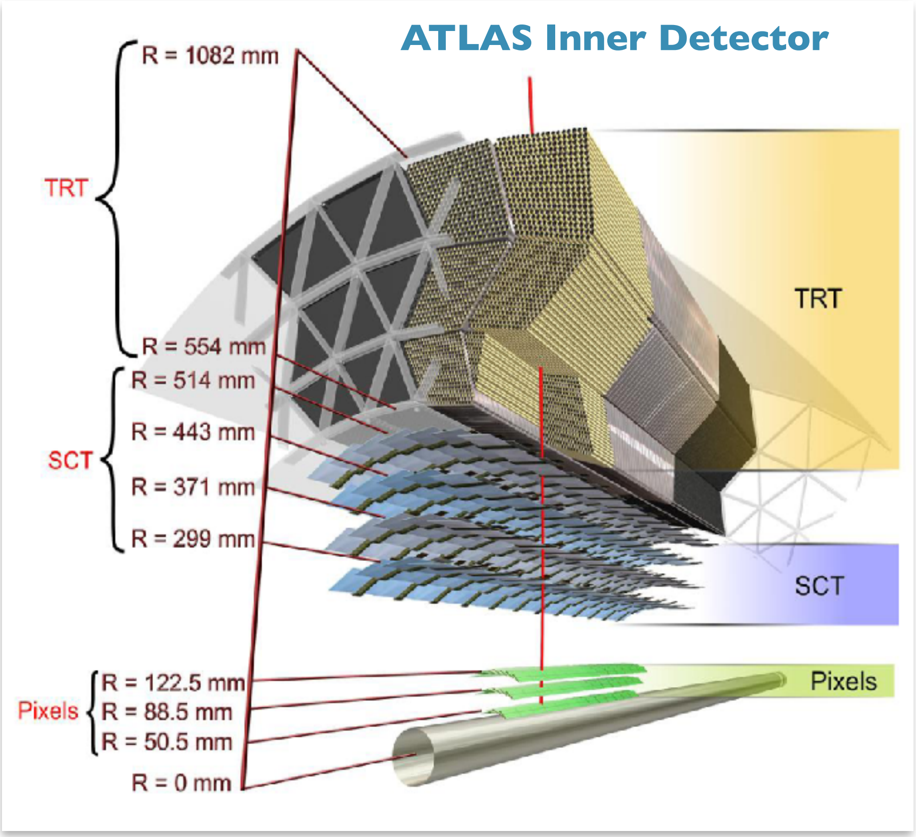
Hybrid pixel detector

SILICON STRIP DETECTORS

EXAMPLE: CURRENT ATLAS SILICON DETECTOR

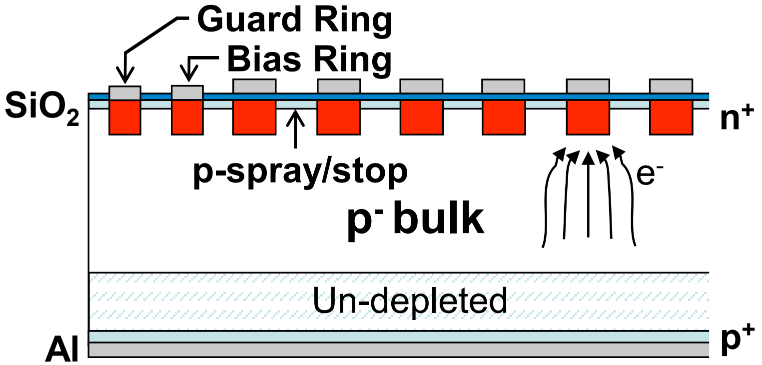
- Current tracking detector “the first meter”:
  - Silicon pixel detector
    - 4 layers, 8 disks
    - Pixel size: 50 x 400µm^2 (IBL: 50 x 250µm^2)
    - 2000 modules with 140M channels
  - SemiConductor Tracker (SCT)
    - Strips width: 70µm
    - 4088 modules with 6.3M channels, 62m^2



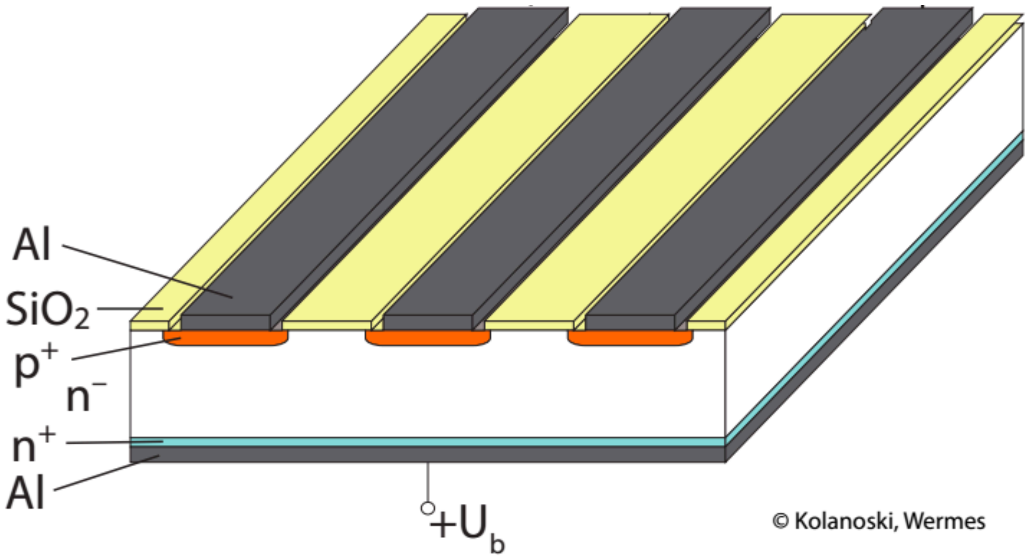


SILICON STRIP DETECTOR

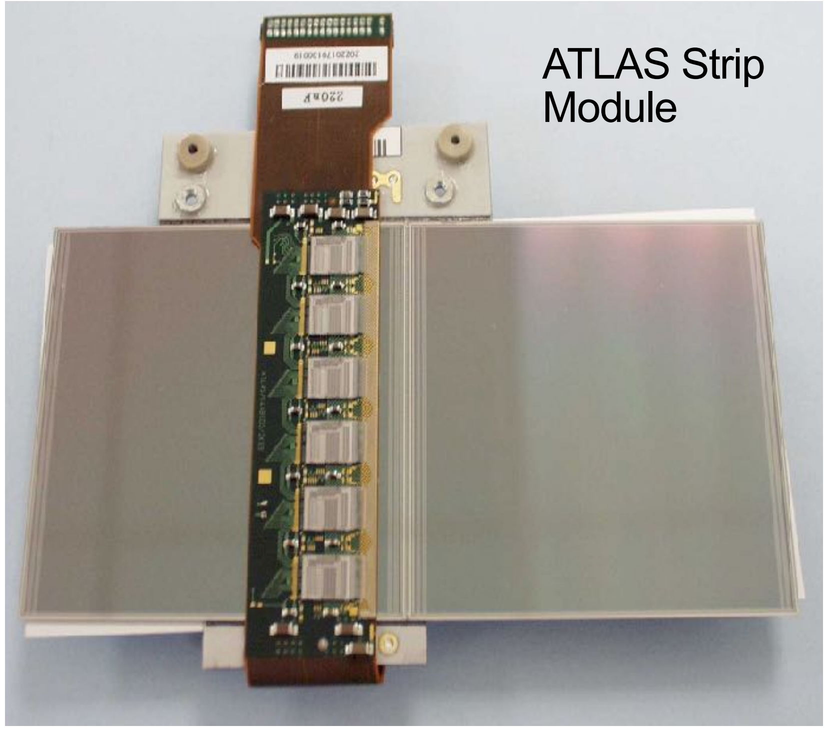
- Segmented p-n diode with applied bias voltage
- Particle creates charges
  - 81 e- per um.
- Charges drift to contacts
- Signal is read out - typically connected with wire-bonds



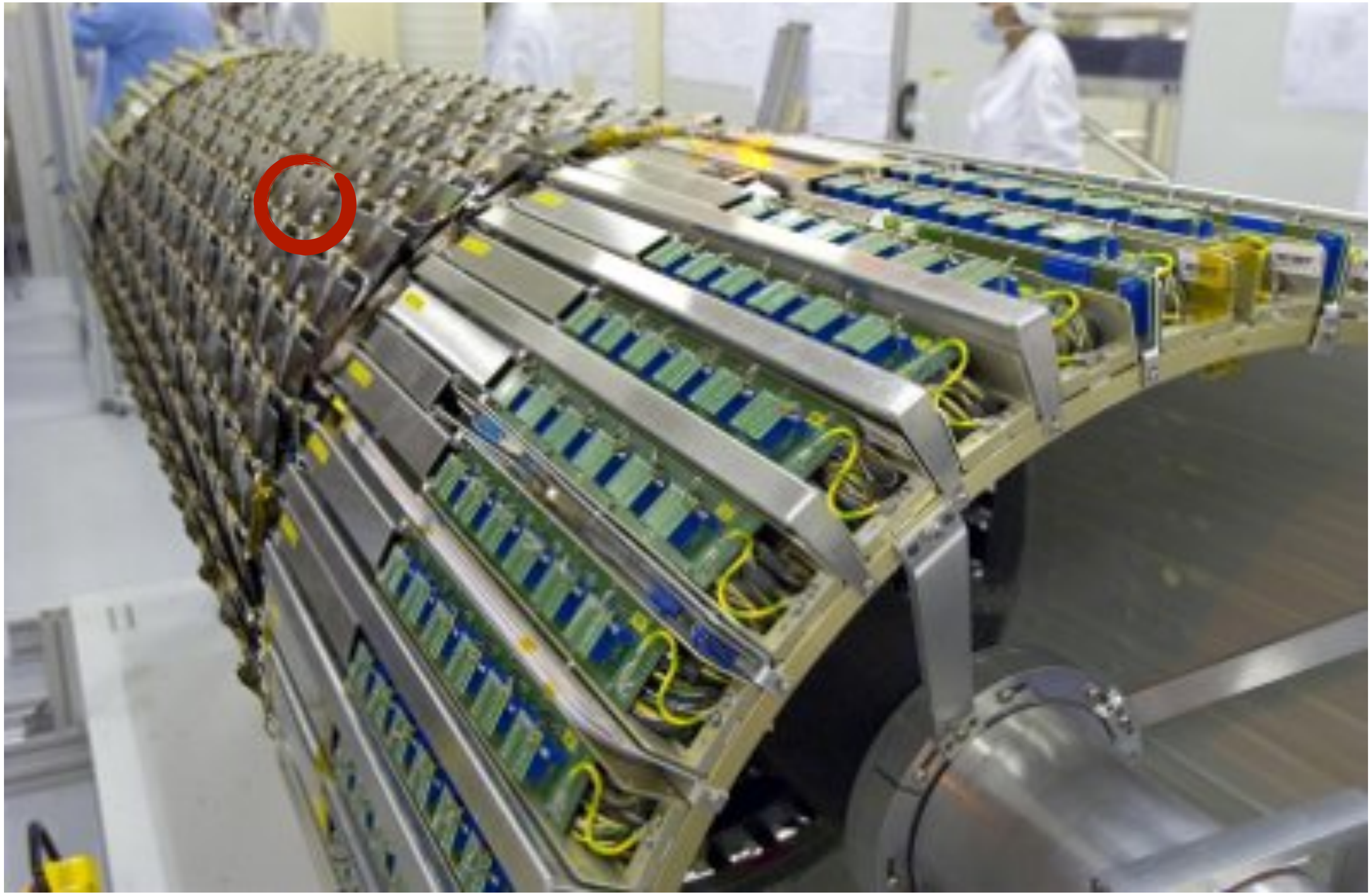
Cross-section through sensor



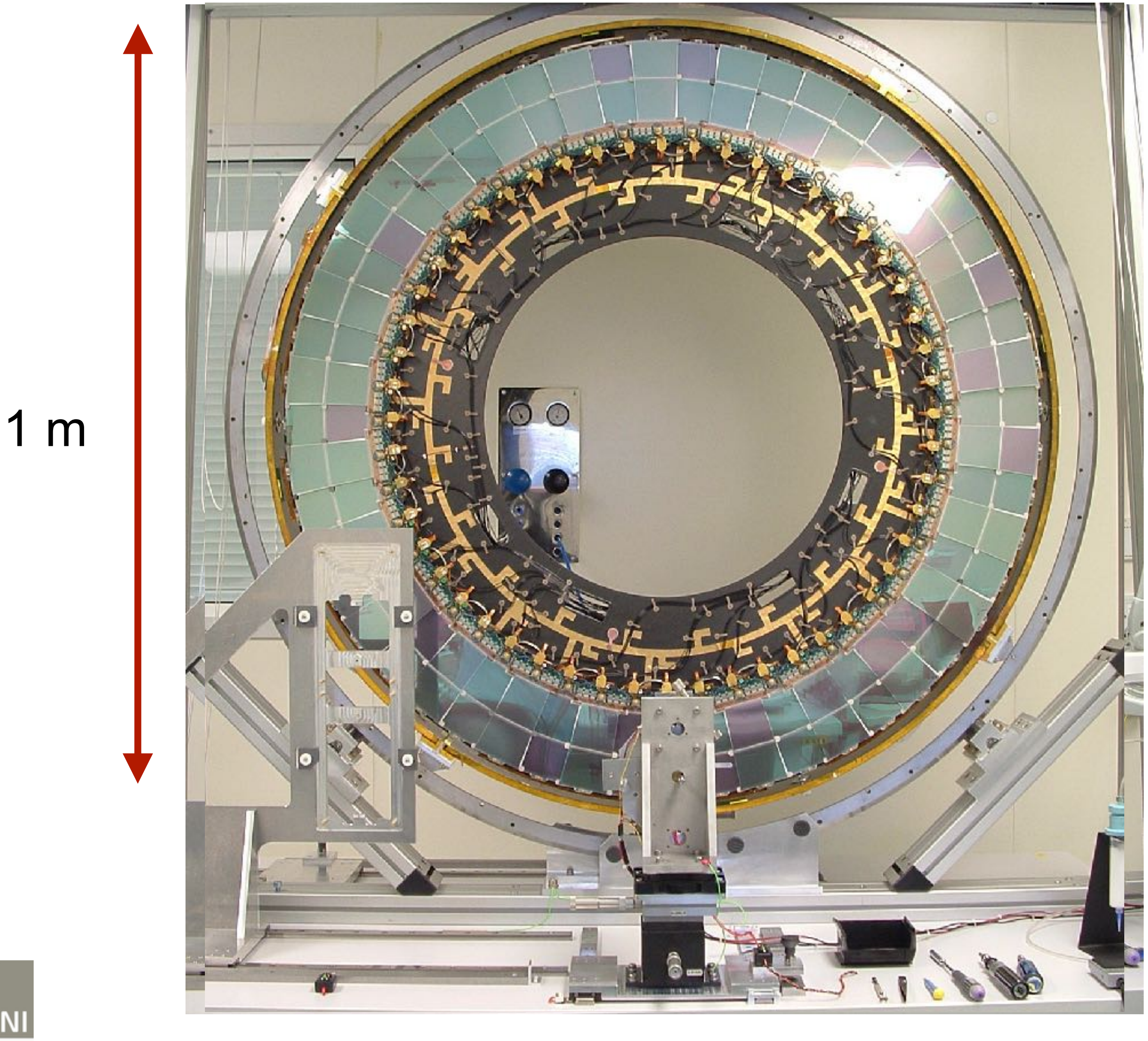
© Kolanoski, Wermes

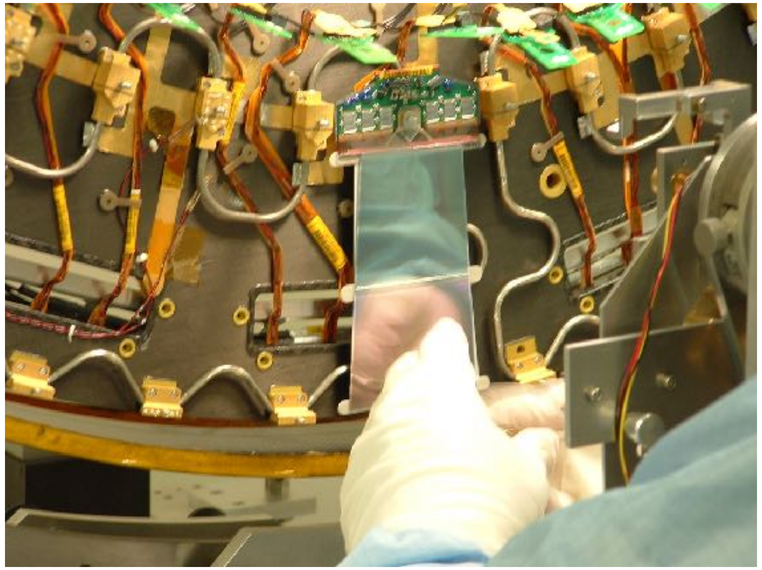

ATLAS Strip Module

ATLAS SCT BARREL SECTION

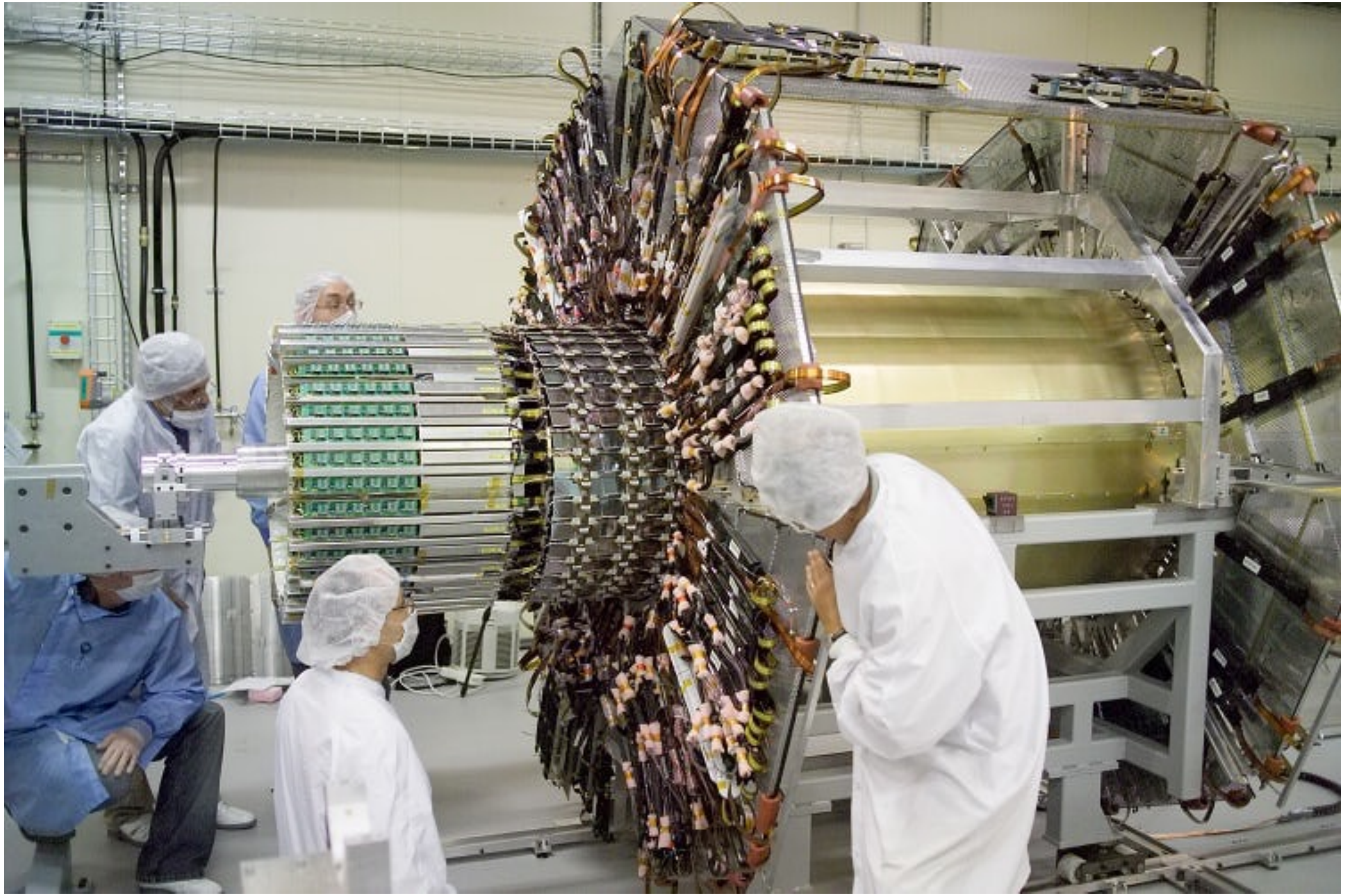


ATLAS SCT ENDCAP - BEAUTY SHOT



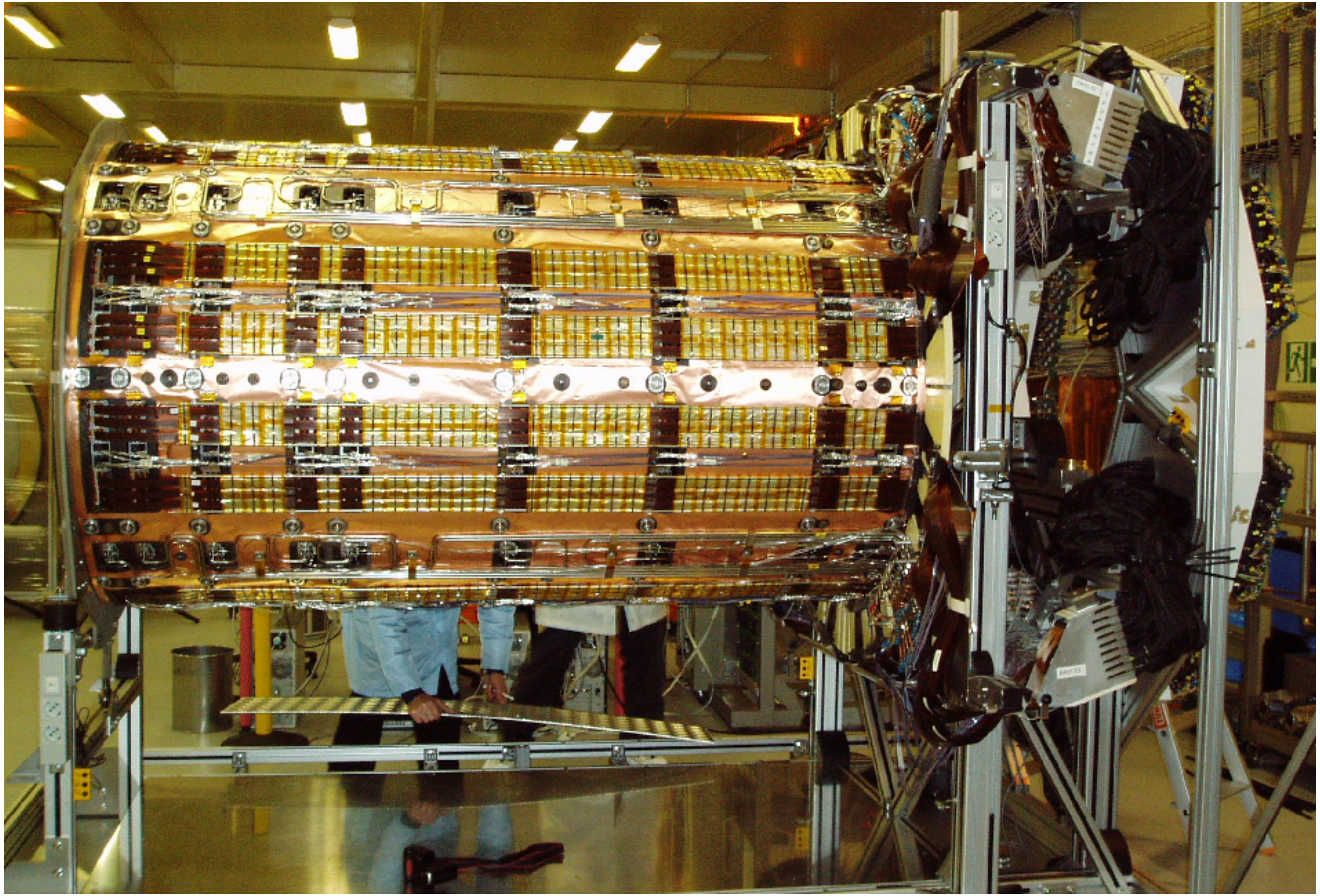


SILICON TRACKER (SCT)

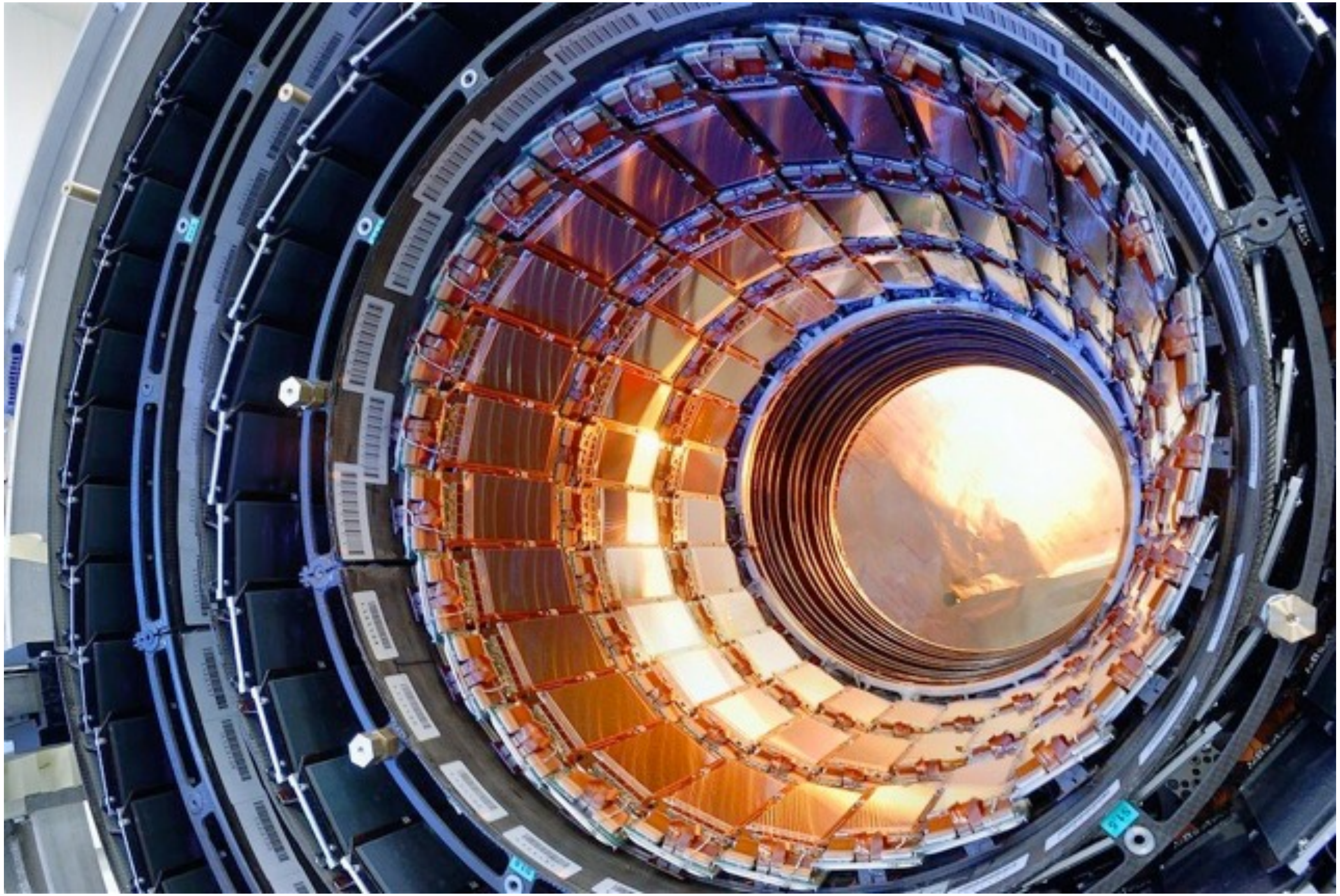


Insertion of the 3^{rd} cylinder (out of the four) into the barrel SCT

SCT BARREL



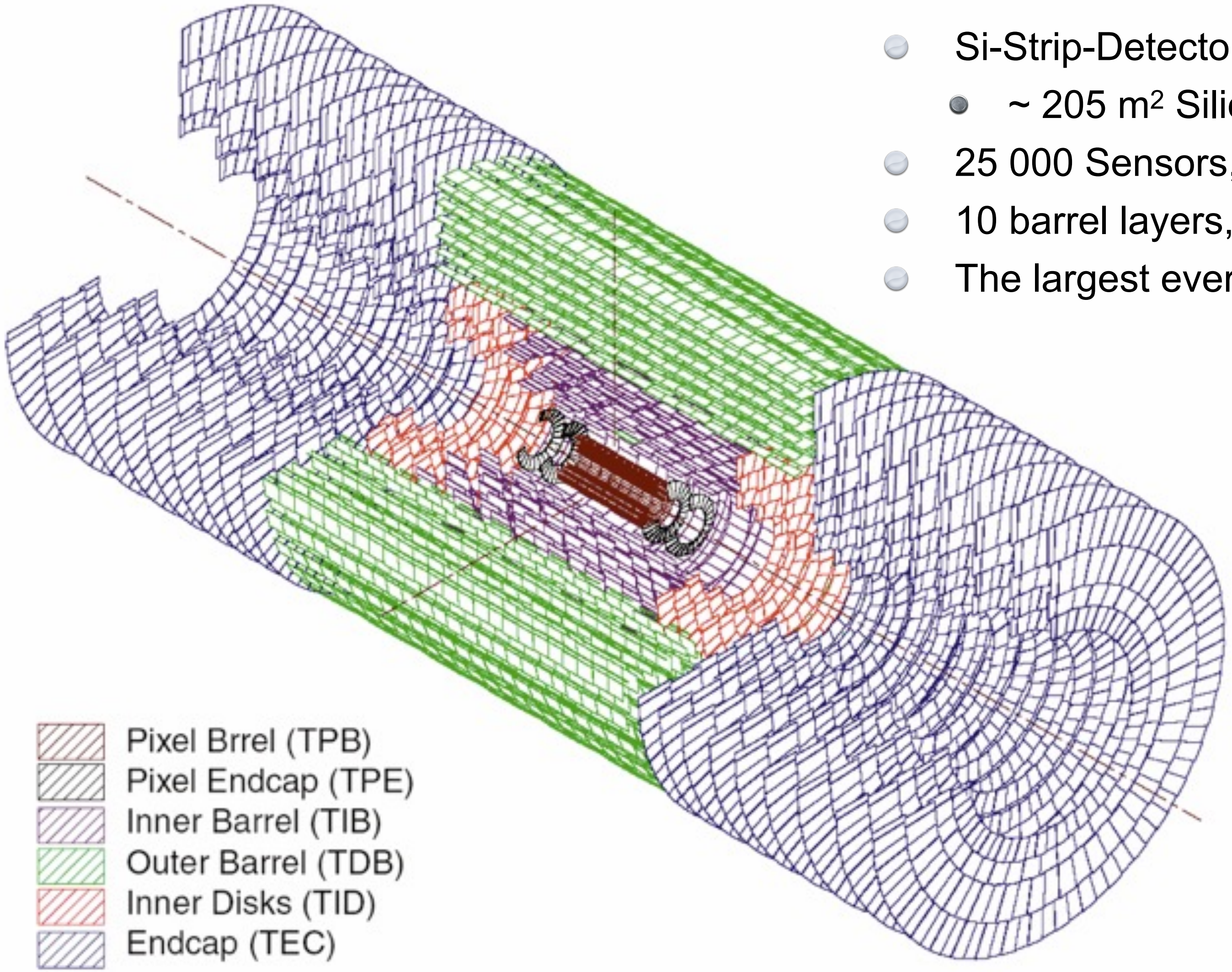
CMS TRACKER - BEAUTY SHOT

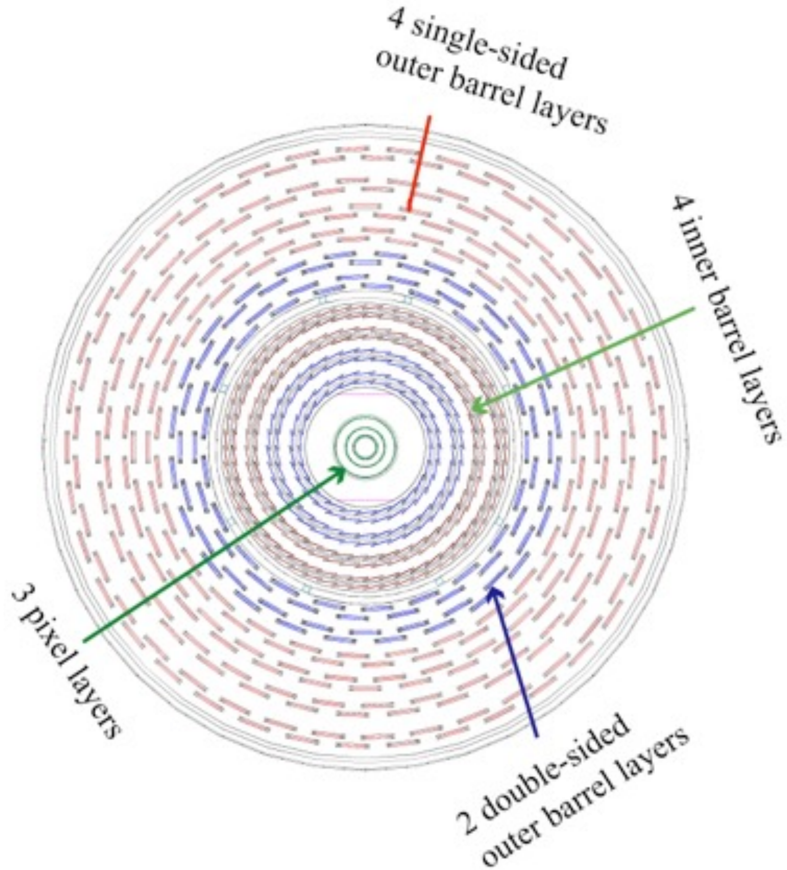


Pic: CERN

CMS Si-Tracker

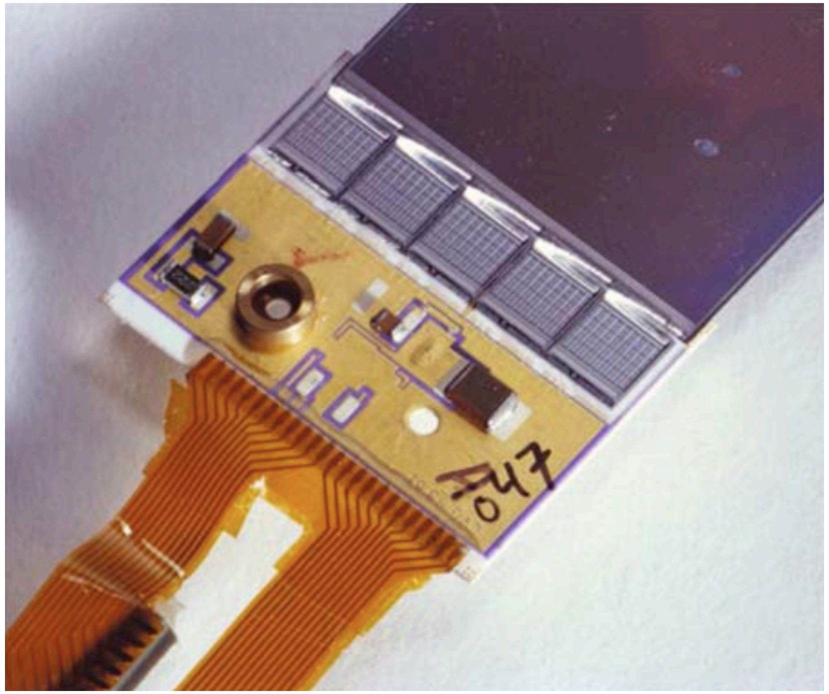
- Si-Strip-Detector:
  - ~ 205 m² Silicon
- 25 000 Sensors, 9.6 M channels
- 10 barrel layers, 2x 9 discs
- The largest ever built silicon tracker

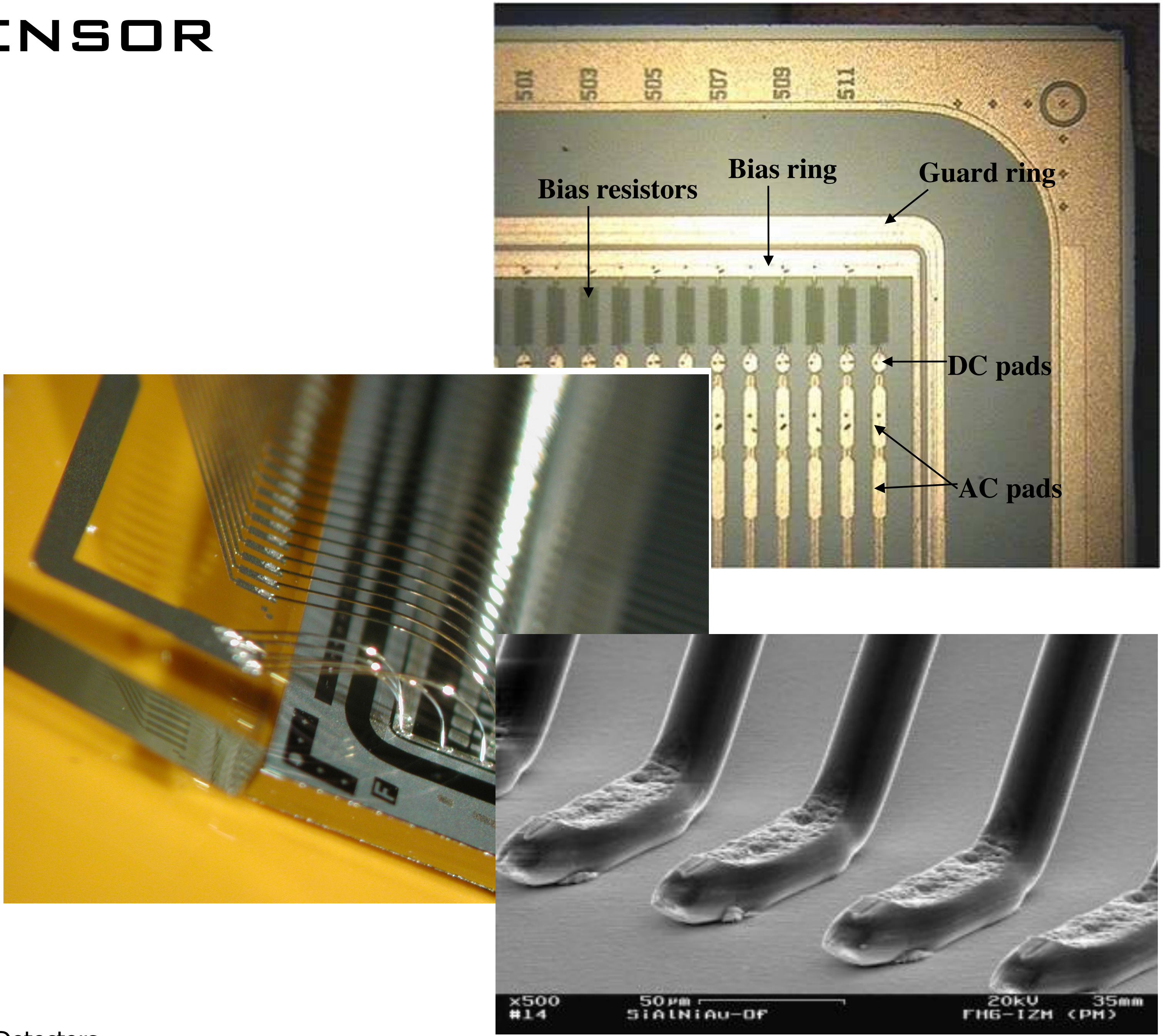




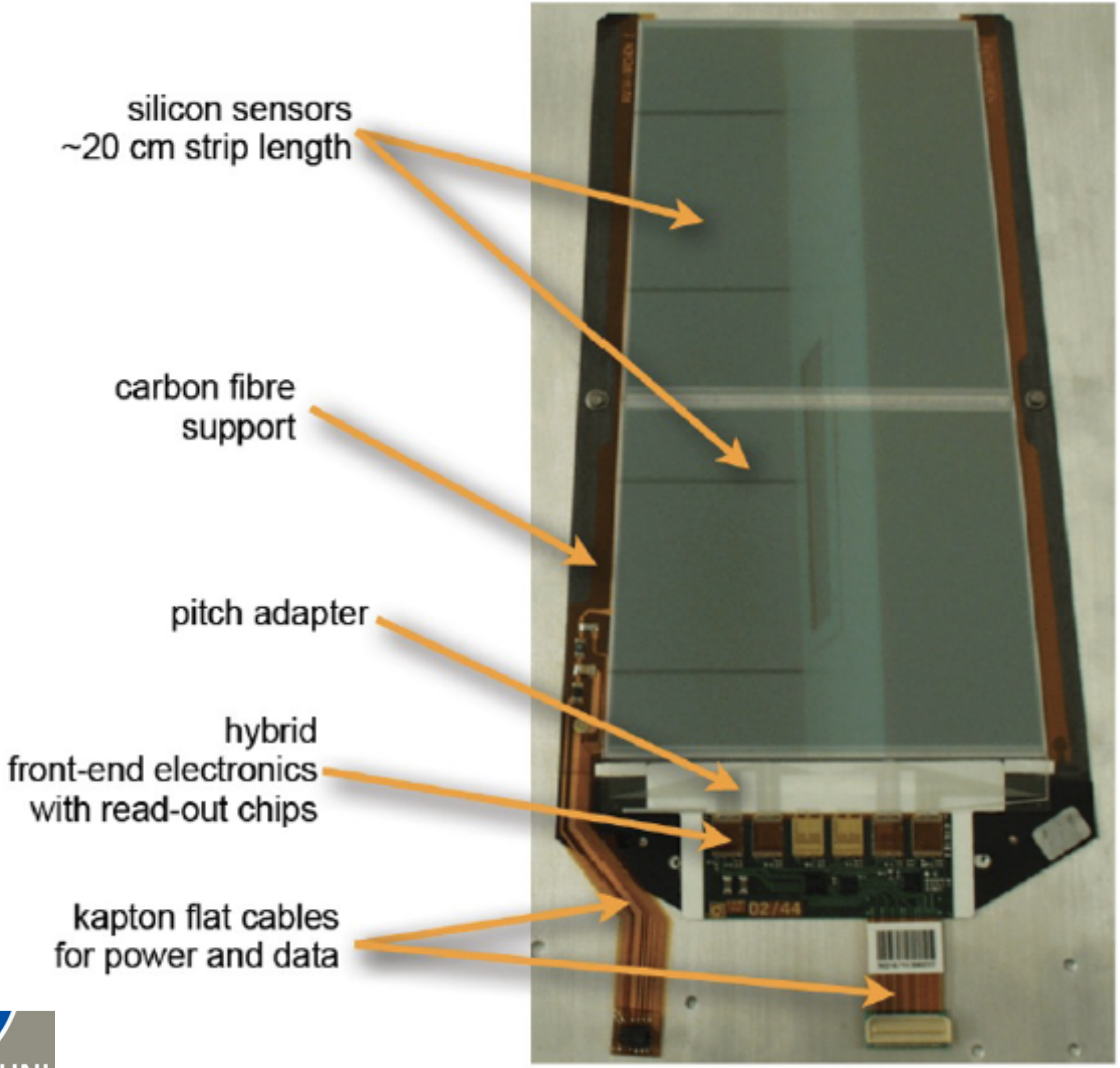
SILICON STRIP SENSOR

CMS-Microstrip-Detektor:
View of a corner with polysilicon resistors, probe pads, strip ends





STRIP MODULE CMS



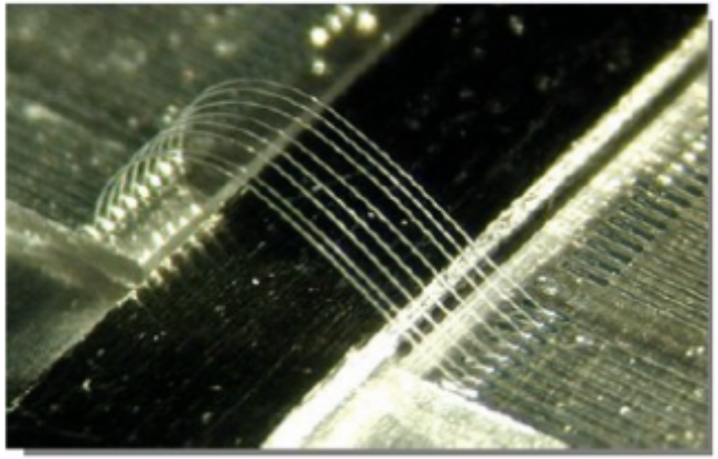
silicon sensors
~20 cm strip length

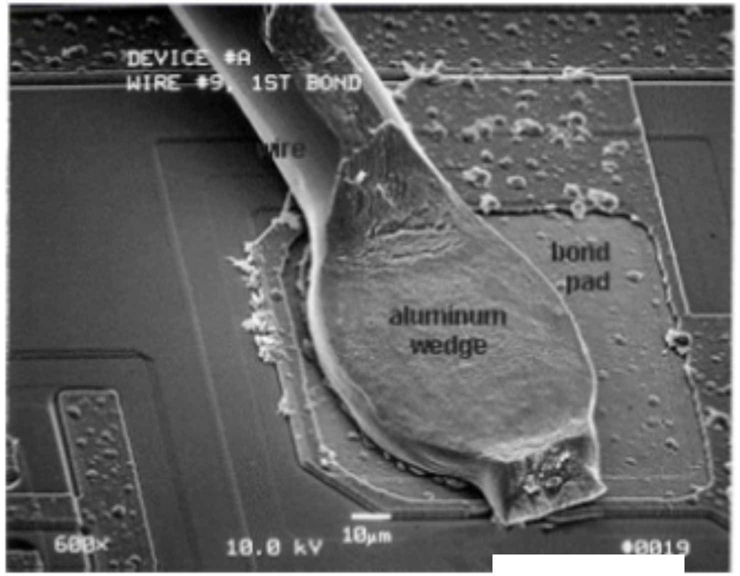
carbon fibre
support

pitch adapter

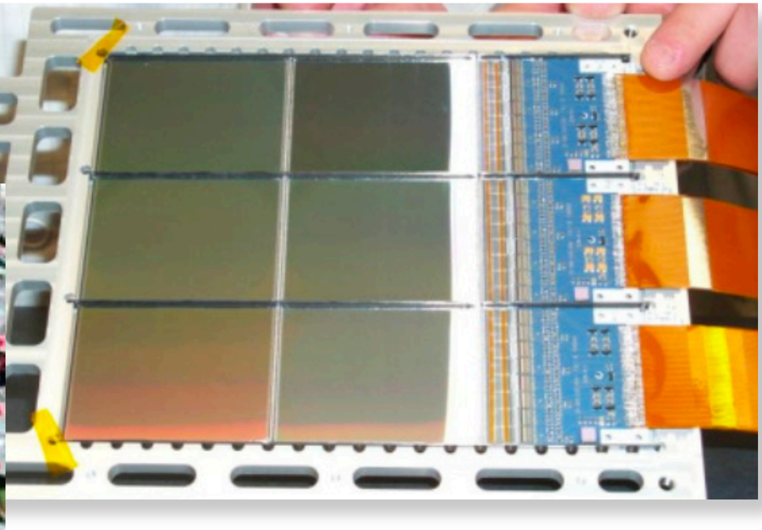
hybrid
front-end electronics
with read-out chips

kapton flat cables
for power and data

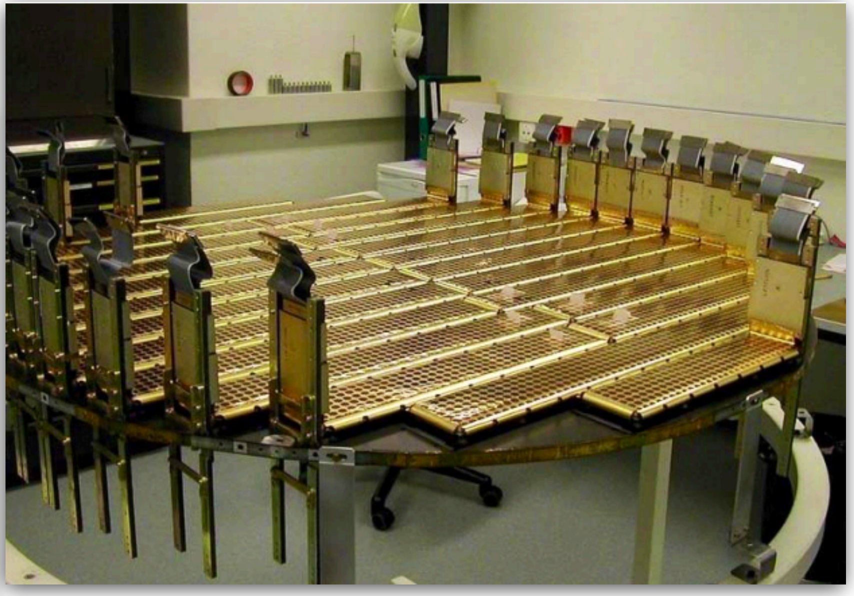




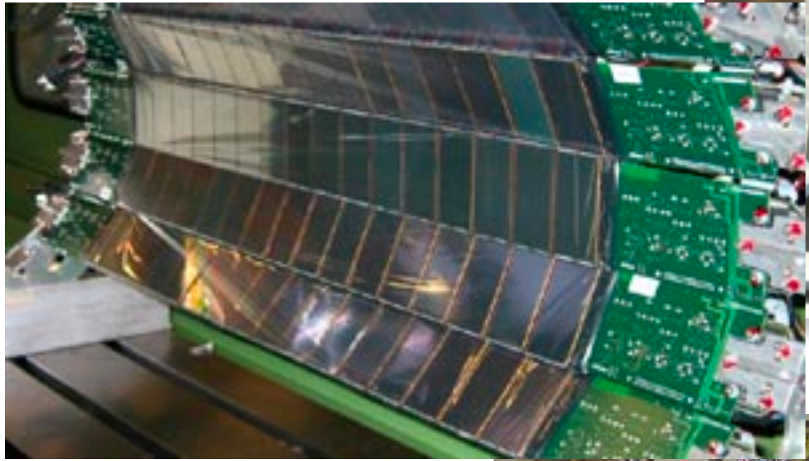
STRIP DETECTORS



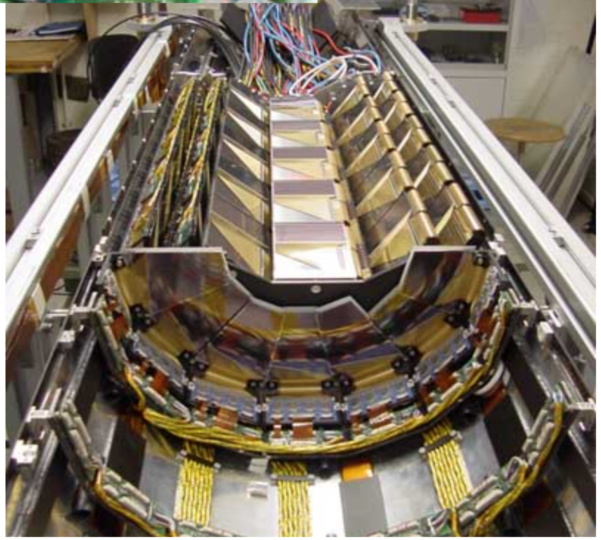
PAMELA satellite experiment



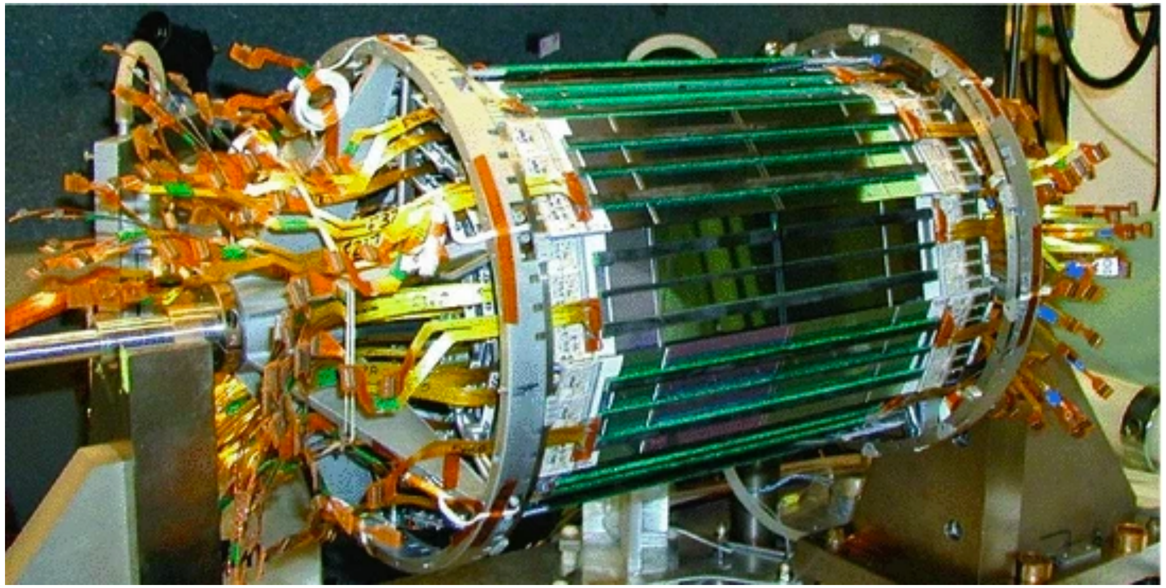
AMS-02 silicon strip tracking detector



STAR Strip Tracker



ZEUS MVD 2000

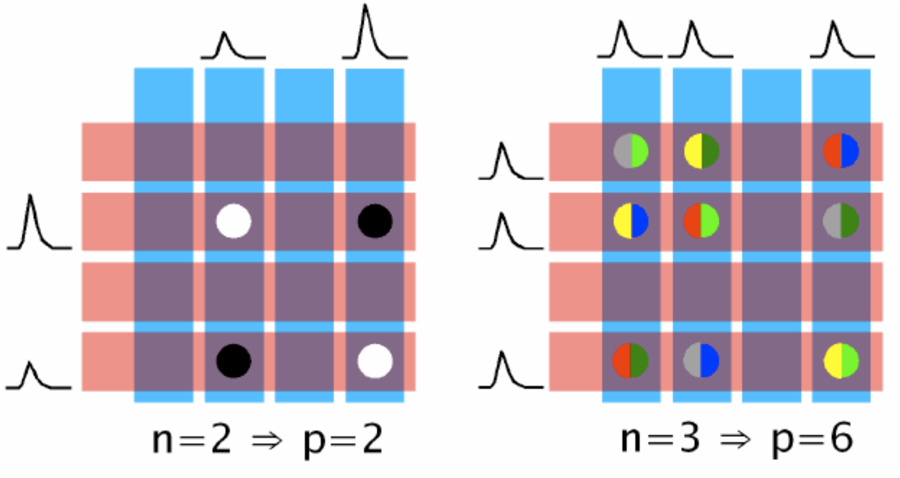


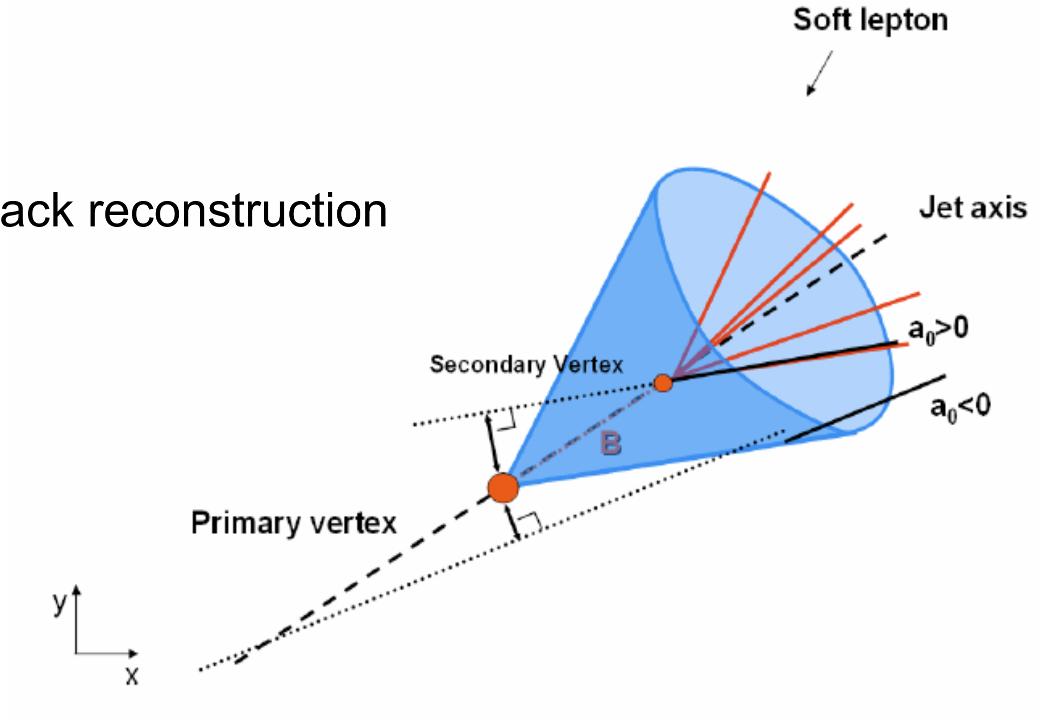
SVX-2 CDF Strip Detector

SILICON PIXEL DETECTORS

LIMITS OF STRIP DETECTORS

- In case of high hit density ambiguities give difficulties for the track reconstruction

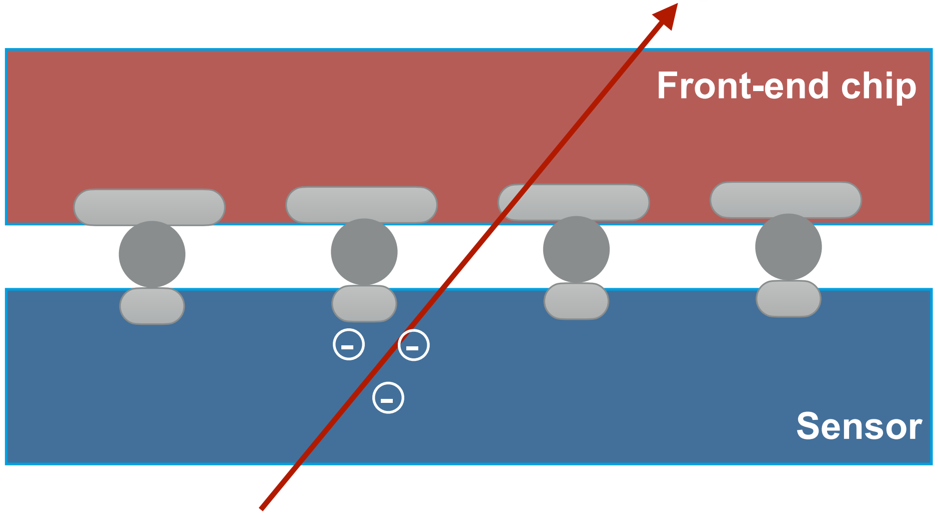




- Deriving the point resolution from just one coordinate is not enough information to reconstruct a secondary vertex
  - Pixel detectors allow track reconstruction at high particle rate without ambiguities
  - Good resolution with two coordinates (depending on pixel size and charge sharing between pixels)
  - Very high channel number: complex read-out
  - Readout in active area a detector

First pixels (CCDs)
in NA11/NA32: ~1983

Hybrid Pixels – "classical" Choice

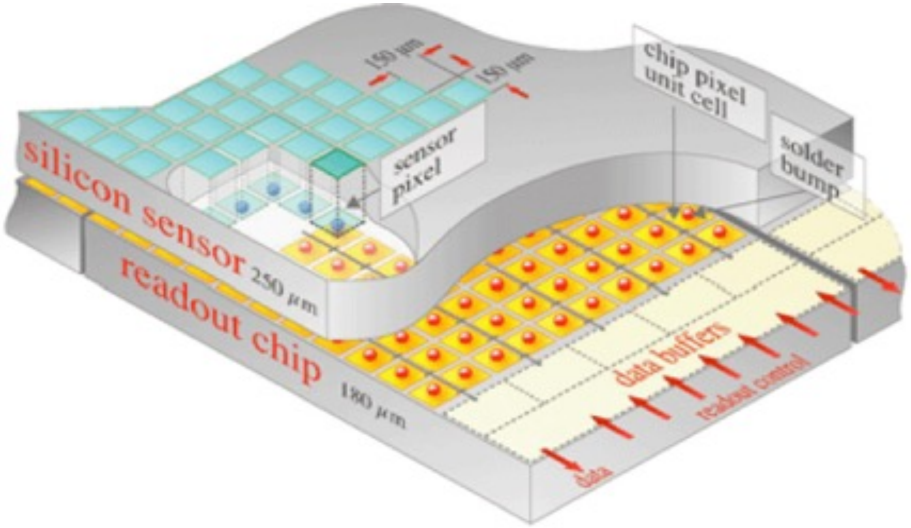


- The read-out chip is mounted directly on top of the pixels (bump-bonding)
- Each pixel has its own read-out amplifier
- Can choose proper process for sensor and read-out separately
- Fast read-out and radiation-tolerant

… but:

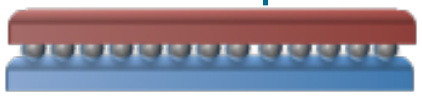
- Pixel area defined by the size of the read-out chip
- High material budget and high power dissipation

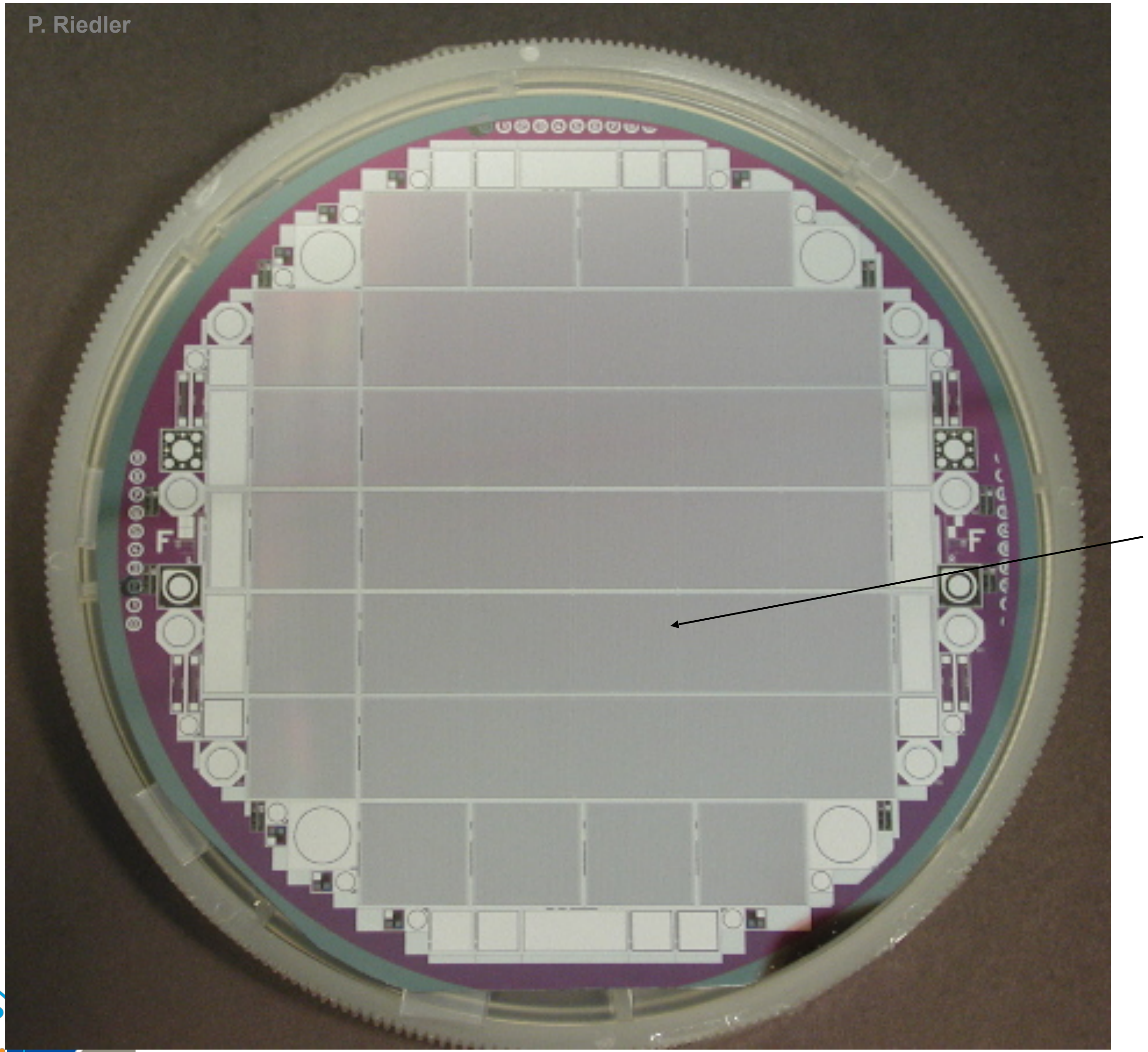
Hybrid Pixel
(CMS)



- CMS Pixels: ~65 M channels
  150 µm x 150 µm
- ATLAS Pixels: ~80 M channels
  50 µm x 400 µm (long in z or r)
- Alice: 50 µm x 425 µm
- LHCb
- Phenix@RHIC
- ….

Pixel Sensor



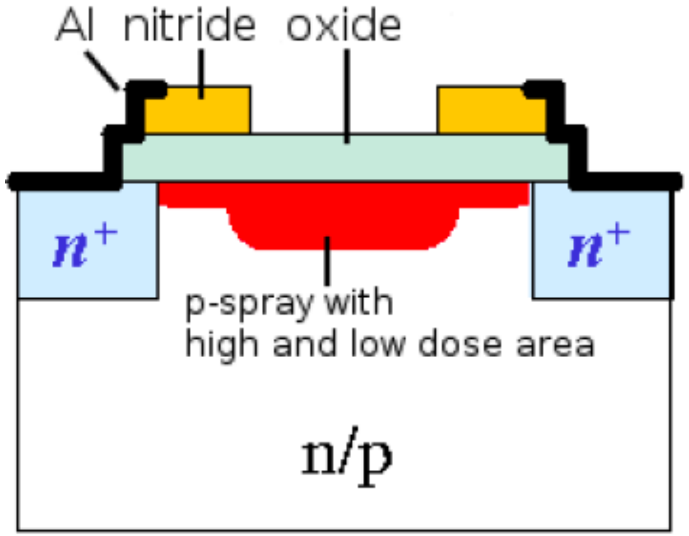

P. Riedler

Different sensor materials can be used: Si, CdTe, GaAs, …

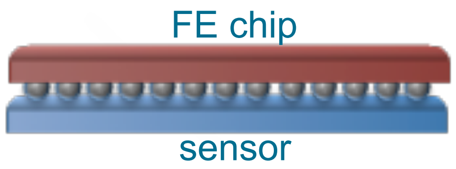
Depending on application (tracking, single photon counting, ..)

Usually several readout chips are connected to one sensor.

Pixel cell (50µm x 425µm)

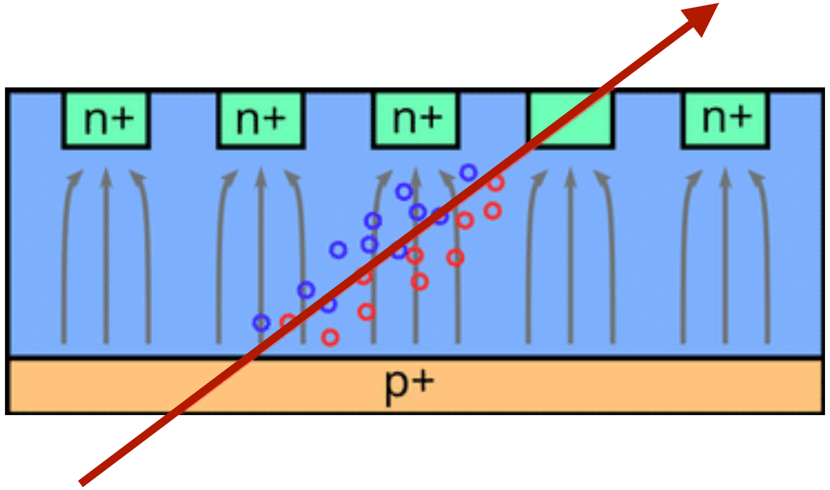


Typical Sensors for Hybrid Pixels



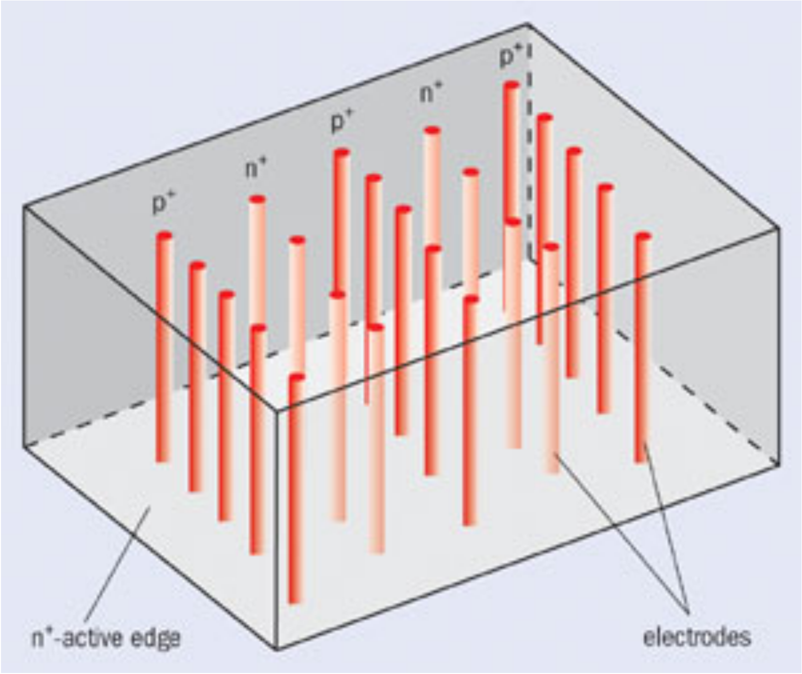
Planar Sensor

- Silicon diode (on-junction)
- Current LHC sensors mostly **n-in-n** planar sensor
- For HL-LHC different concepts were studied (n-in-n; n-in-p ….)
- Radiation hardness proven up to 5 x10^{16} p/cm^2
- Problem: HV might need to exceed 1000V



3D Silicon

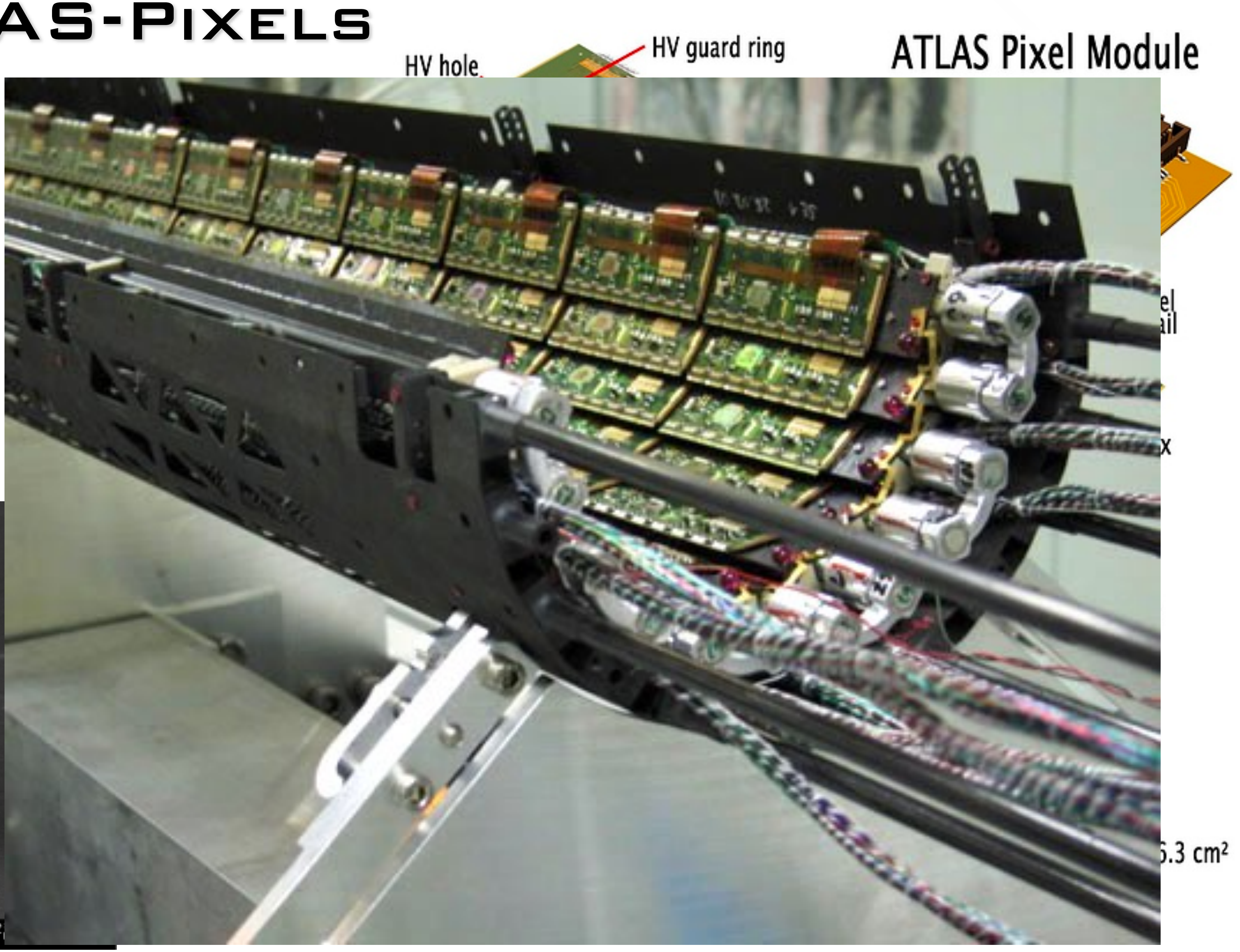
- Both electrode types are processed inside the detector bulk instead of being implanted on the wafer's surface.
- Max. drift and depletion distance set by electrode spacing
- Reduced collection time and depletion voltage
- Intrinsically higher radiation tolerance
- Low charge sharing
- In current detectors only in ATLAS IBL @high eta

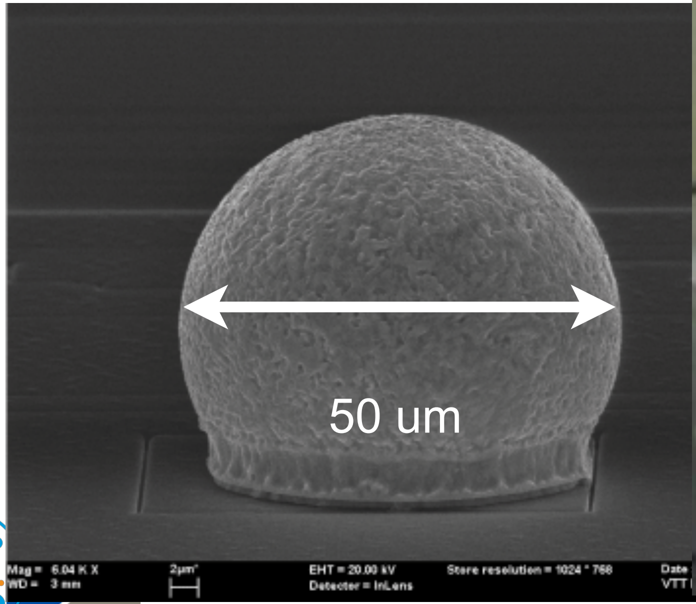


Example: ATLAS-Pixels

A pixel module contains:

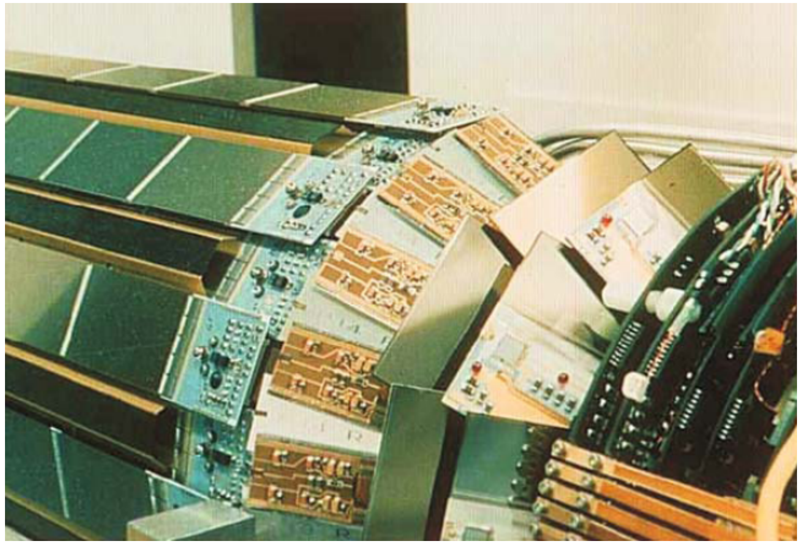
1 sensor (2x6cm)
  ~40000 pixels (50x500 mm)
16 front end (FE) chips
  2x8 array
  bump bonded to sensor
Flex-hybrid
1 module control chip (MCC)
There are ~1700 modules

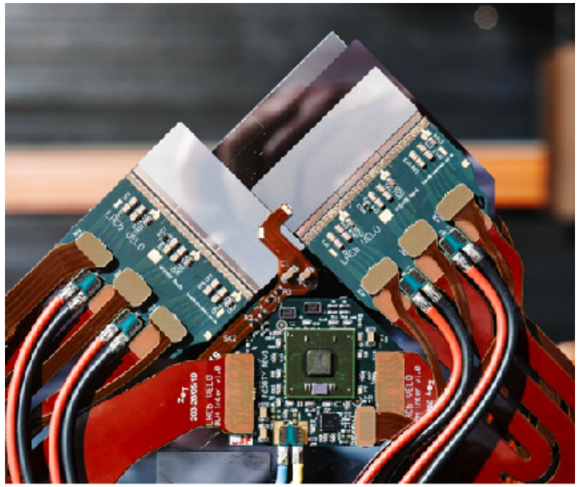


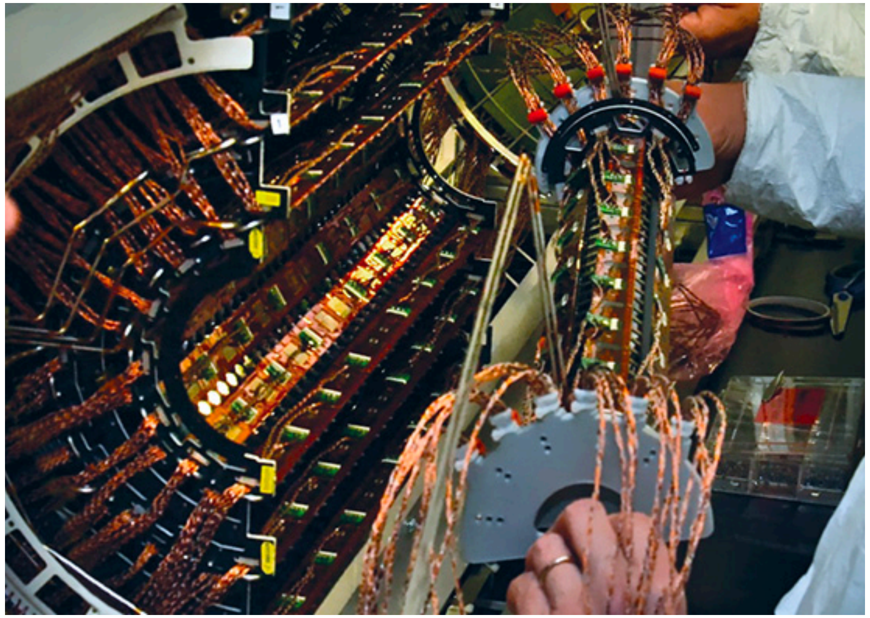


Picture: VTT

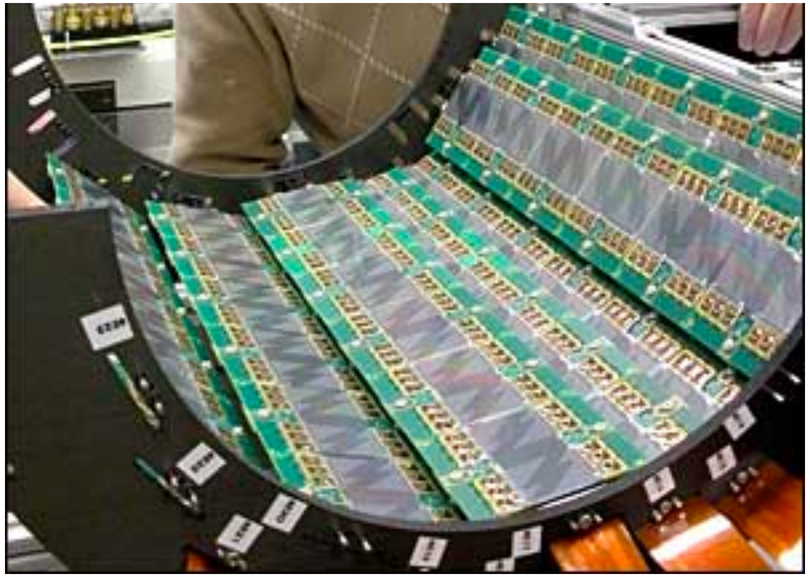
HYBRID PIXEL DETECTORS

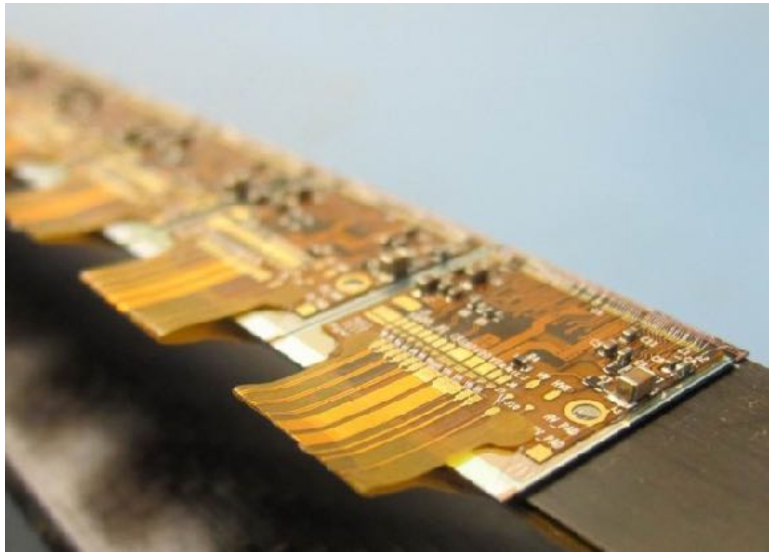

DELPHI VFT 1996


LHCb Velo


CMS Phase1 Pixel Detector

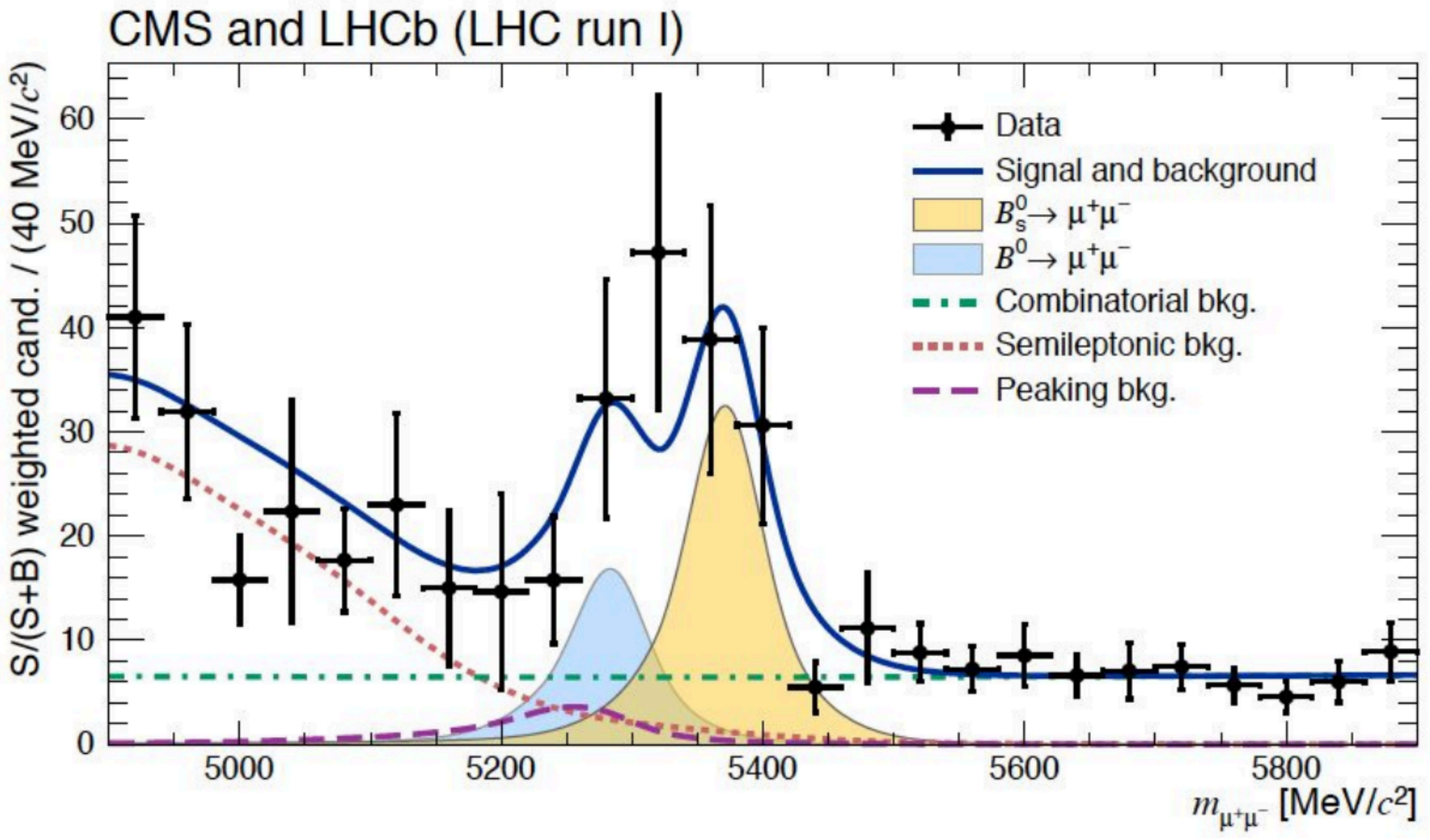
ALICE ITS


PHENIX pixel detector


ATLAS Insertable B-Layer

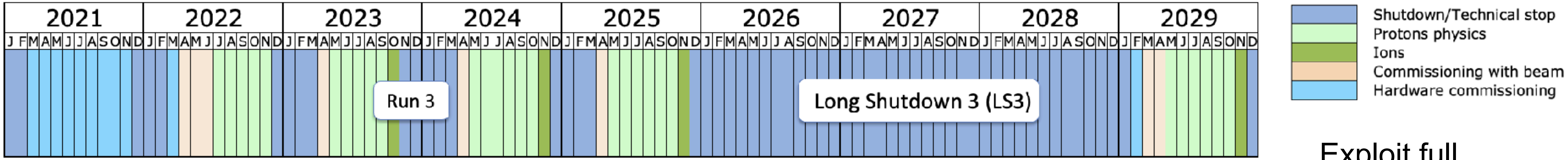
NEXT GENERATION SILICON-DETECTORS

LHC HIGH LUMINOSITY → HIGH PRECISION



- Much better precision for Higgs coupling strengths and measurements like $B_s^0 \to \mu^+\mu^-$
- B → μμ measurements are expected to achieve 6.8σ precision

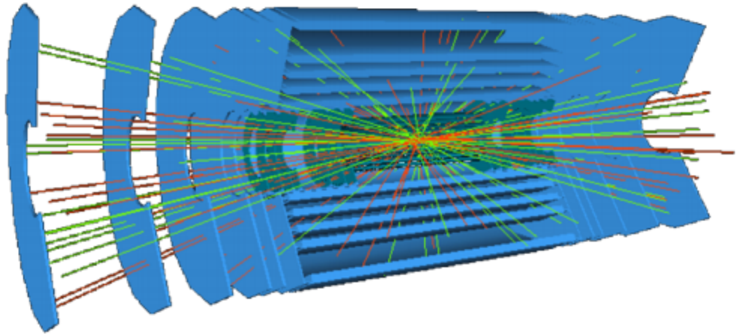
AT LHC NEW TRACKER NEEDED … WHY ?



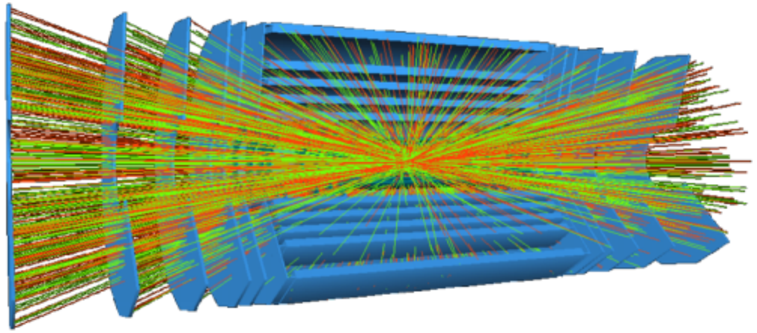
Exploit full potential of LHC

- **HL-LHC implies significant scaling of design parameters:**
  - Peak luminosity: 5-7 x 10^{34} $1/cm^2s$ ➡ **x 5-7**
  - Integrated luminosity: 4000 fb-1 ➡ **x10**
  - Fluences up to $2x10^{16}$MeV n_{eq} $/cm^2$ ➡ **x10**
  - Average pile-up: up to ~200 ➡ **x 8**

New sensor & readout require more radiation hardness



LHC, 20 - 55 pile-up events

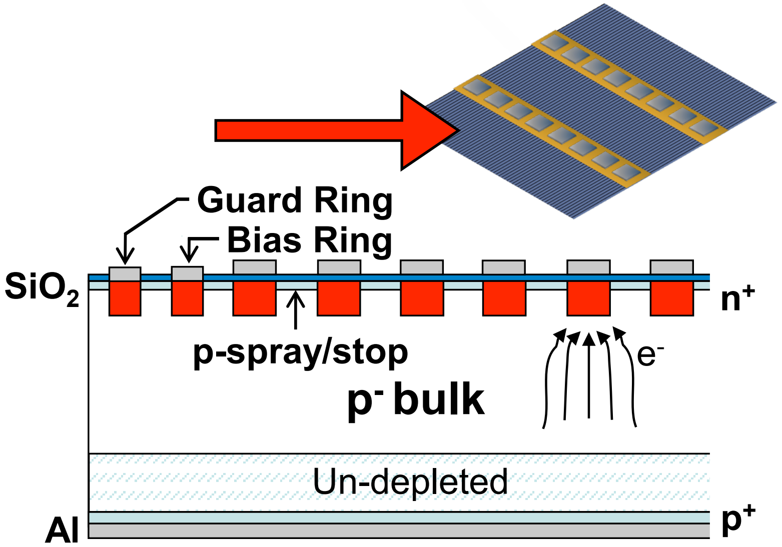


HL-LHC, 140 - 200 pile-up events

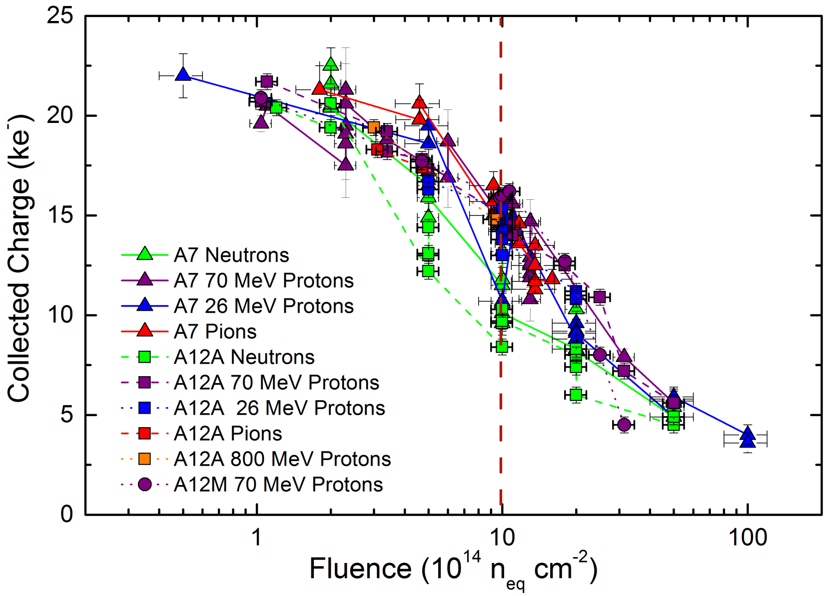
Silicon Strips Sensors

- Sensor parameters defined: **n-in-p with p-stop isolation**
  - Collects electrons
    -> faster signal, reduced charge trapping
  - Always depletes from the segmented side:
    good signal even under-depleted
- Single-sided process
  - Cheaper than n-in-n
  - More foundries and available capacity world-wide
- Radiation damage most important issue

Sensor	
Substrate material	p type FZ
Thickness	300-320 μm
Resistance	> 3kΩcm
Collected charge after $1x10^{15}$ n_{eq} /	> 7500 e^- per MIP



Cross-section through sensor

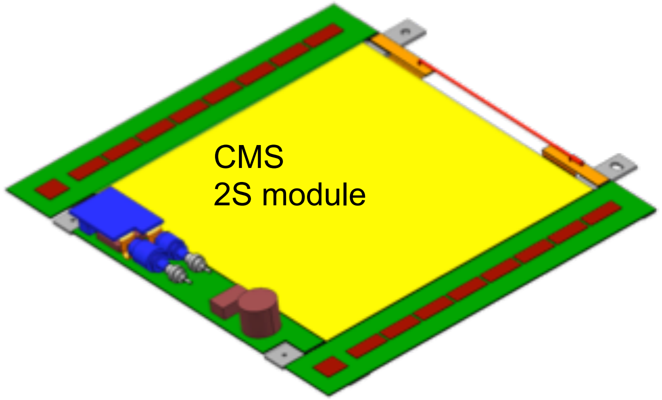


Collected charge versus irradiation

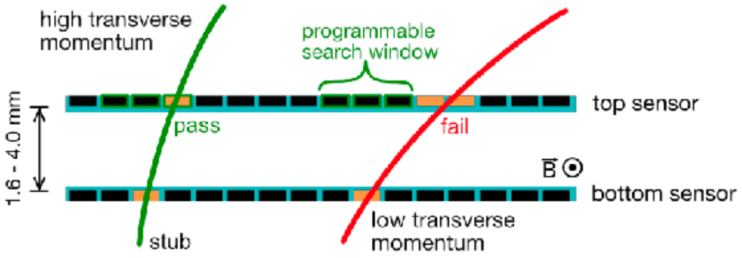
“OUTER” TRACKER FOR ATLAS&CMS

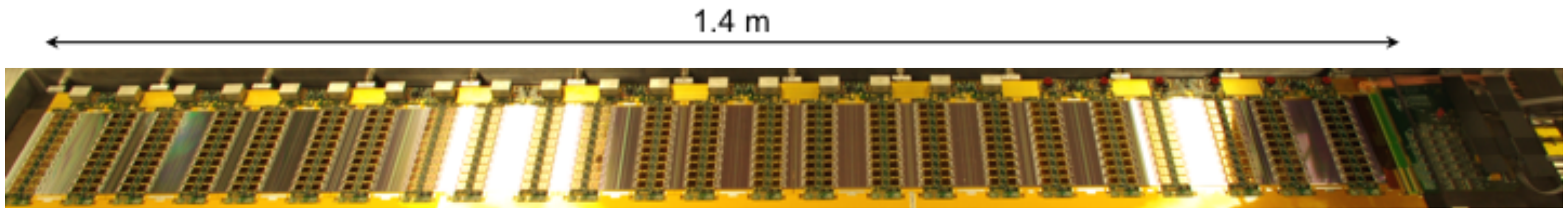
End-cap strips module

- ATLAS&CMS each plan for ~150 m^2 silicon strip detector
- Commonalities:
  - **20000** modules to be produced
  - choice of sensor technology (n-in-p)
  - radiation level (10^{15} n_{eq}/cm^2)

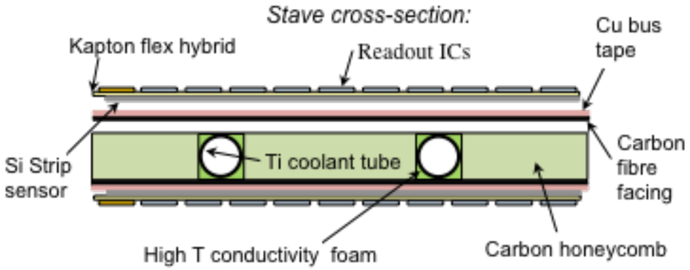


- CMS:
  - modules discriminate low-p_T tracks in the FE electronics
  - hybrid is key element: Wire-bonds from the sensors to the hybrid on the two sides
- ATLAS:
  - stave concept where silicon is directly glued onto carbon fibre



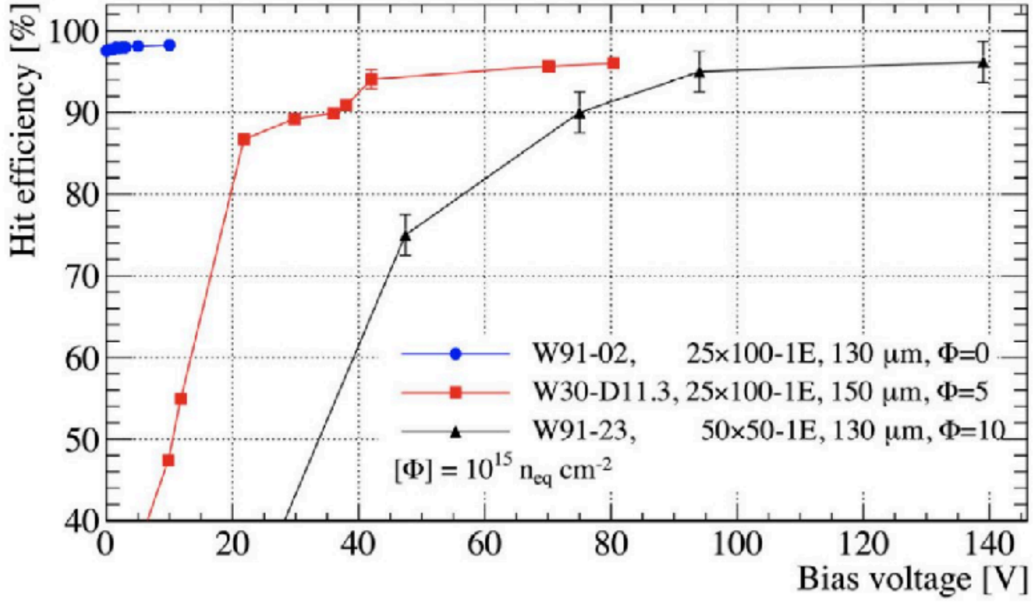


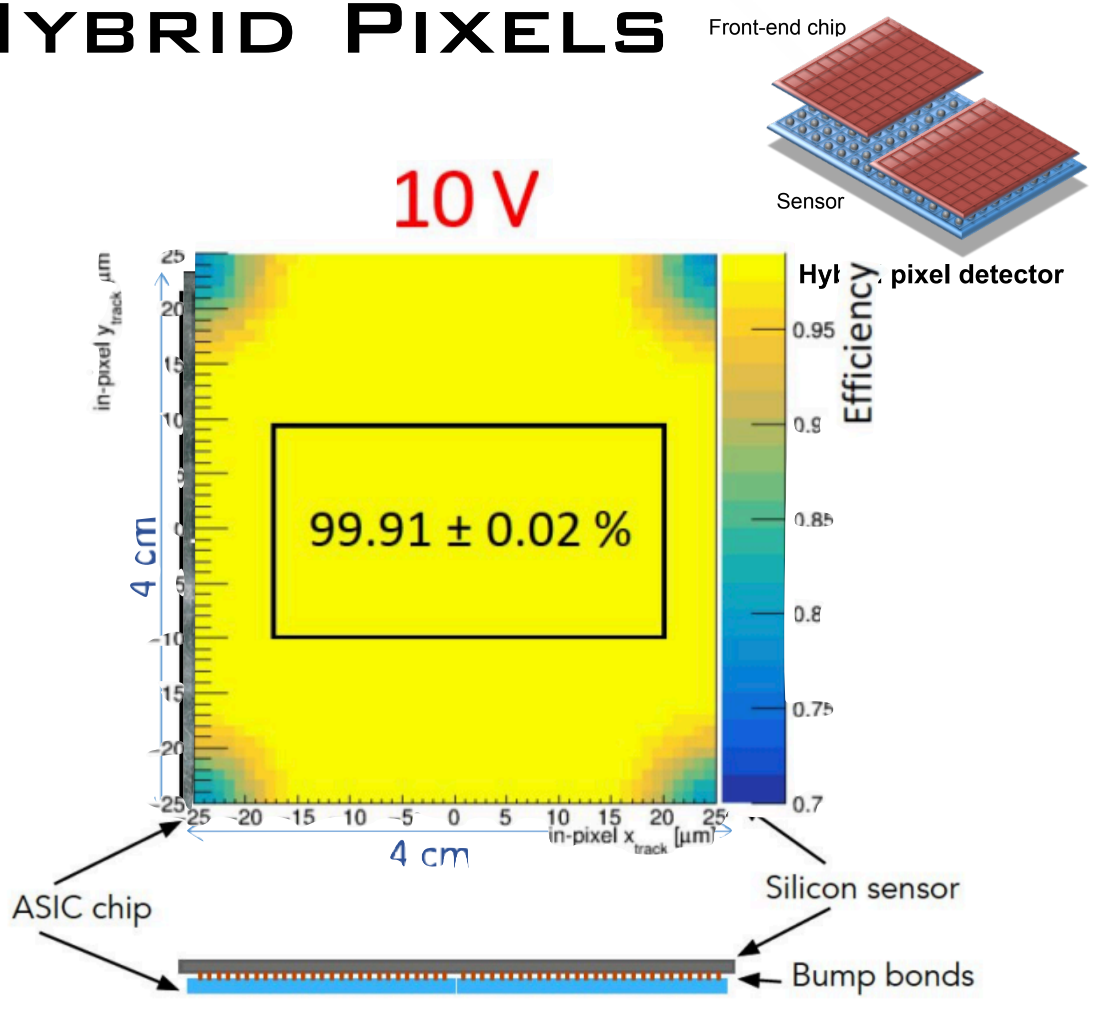
ATLAS Prototype for barrel strip stave



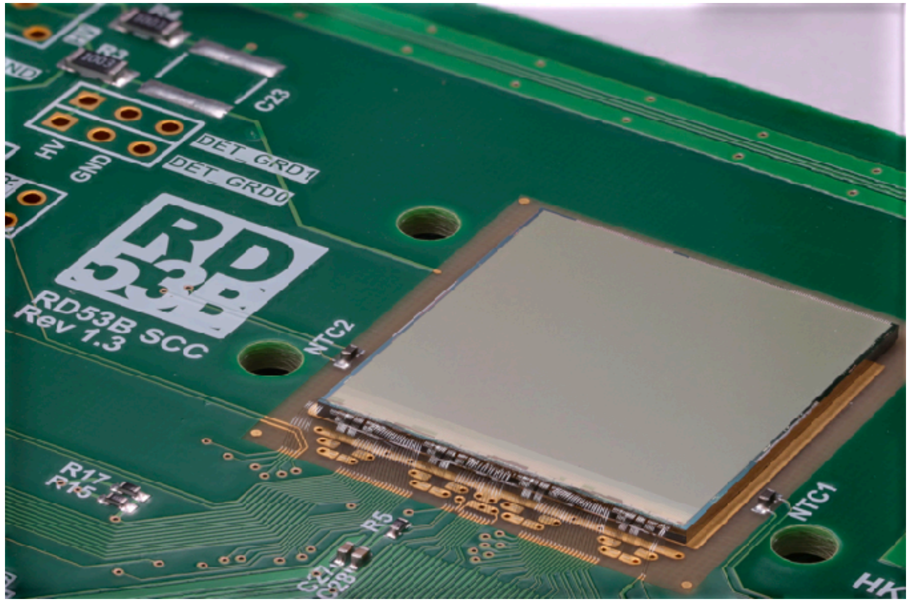
ATLAS AND CMS CHOSE HYBRID PIXELS

- Pixel sensors needed with radiation hardness up to 2x10^{16}MeV n_{eq} /cm^2
- Both collaborations: combination of
  - Planar sensors similar as in current experiments (n-in-p)
  - 3D sensors for the innermost layers



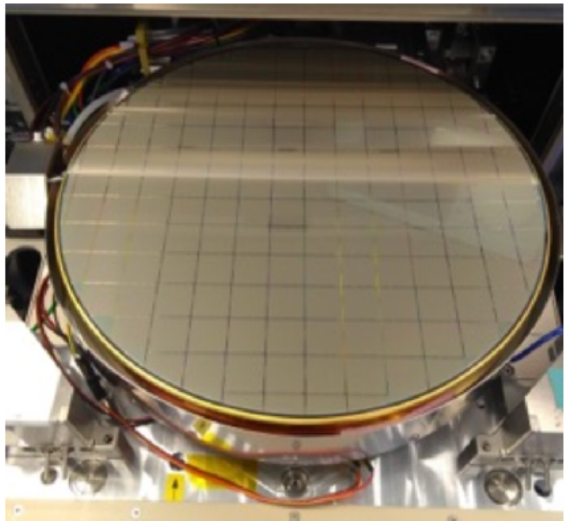


RD53 FRONT-END CHIP



- Main features:
  - 65 nm CMOS, 2x2cm^2 area
  - 384 x 400 pixels (50 x 50 µm^2)
  - Power: 0.56 W/cm^2
  - Rad-hard> 1 Grad
  - Threshold: 1000e (σ = 30e)
  - Noise: 40e
  - 40 MHz clock with 780ps phase adj.
  - 4 data links per chip at 1.28 Gb/s,
  - Digital readout with Time over Threshold

- Developed by RD53 Community
  - The Chip building blocks are in common by CMS and ATLAS, with slight differences

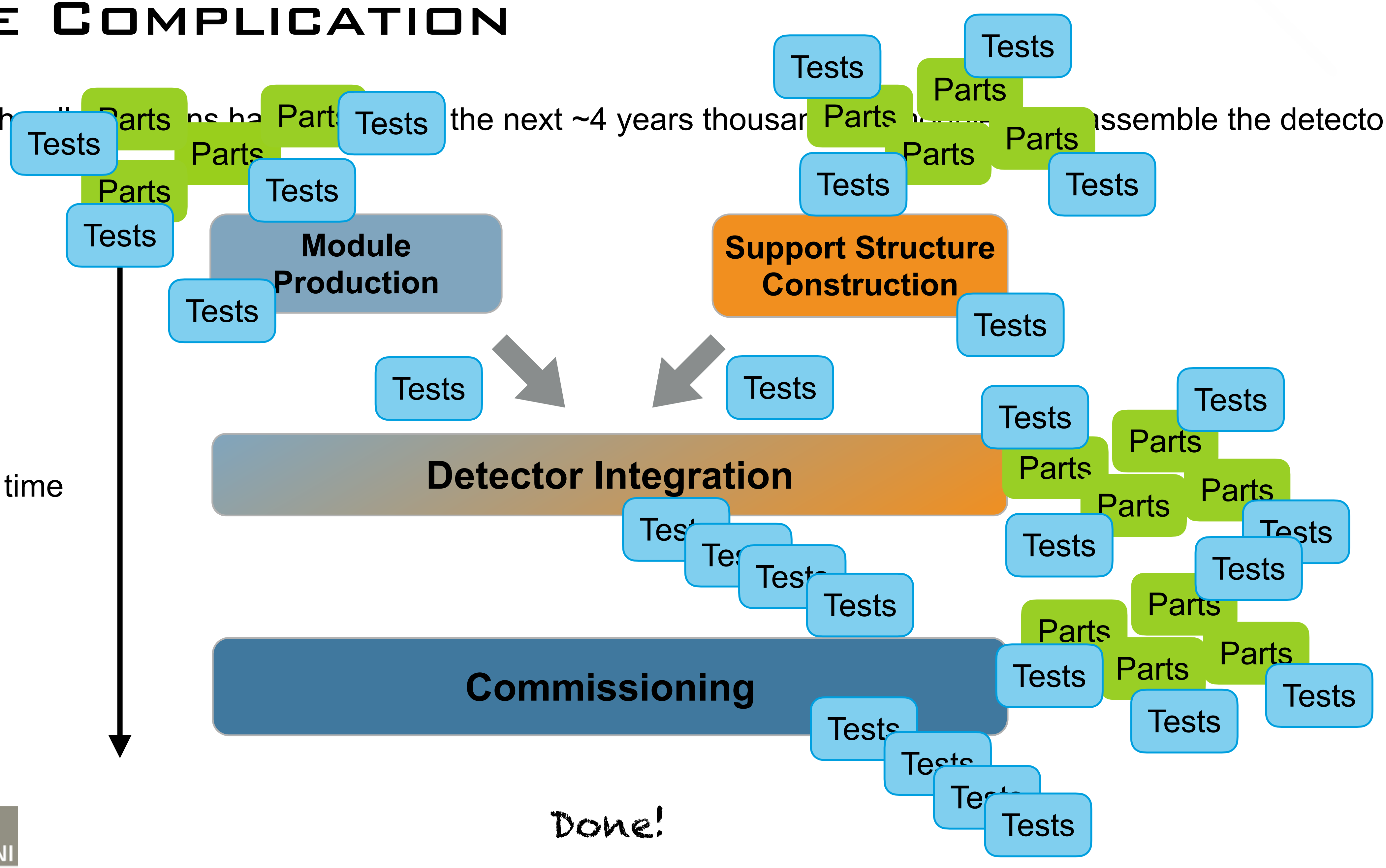


ITkPixV2 wafer

Assembled Single Chip Cards

THE COMPLICATION

- Both ll ns ha the next ~4 years thousar assemble the detectors

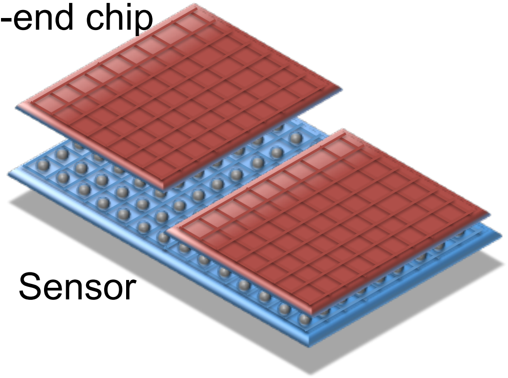


ALTERNATIVE APPROACHES

NEXT GENERATION TRACKING DETECTORS

- Extremely precise and efficient detectors to detect charged particles are needed for many application from particle physics to medical application.

smaller pixel



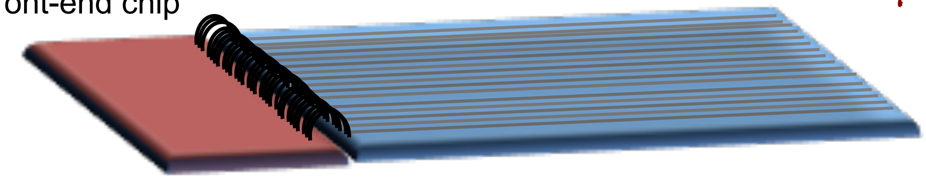
thinner

no bump-bonds

Hybrid pixel detector

no wire-bonds

finer strips



Microstrips detector

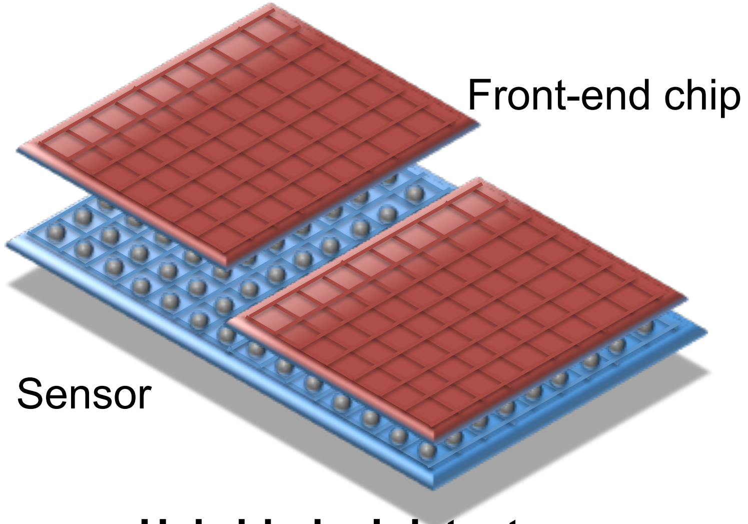
Perfect pixels and strips for next generation tracking detectors:

- very small pitch (~20 µm)
- very thin material (~50 µm)
- high readout speed
- ultra fast timing
- possibly super radiation hard
- smart readout capabilities

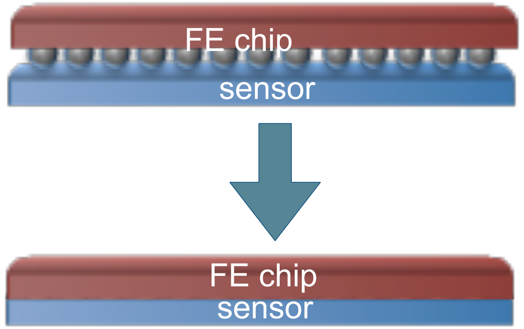
- All in one impossible with existing sensors. We need to
  - Lower the power budget
  - Compress the data on chip to compensate channel density
  - Higher in-pixel intelligence
  - Further understand radiation damage effects
- …while keeping the costs/m^2 reasonable

=> CMOS is an option!!

ALTERNATIVE APPROACH PIXELS



Hybrid pixel detector



Monolithic = front-end electronics on same substrate as active sensor

Idea:

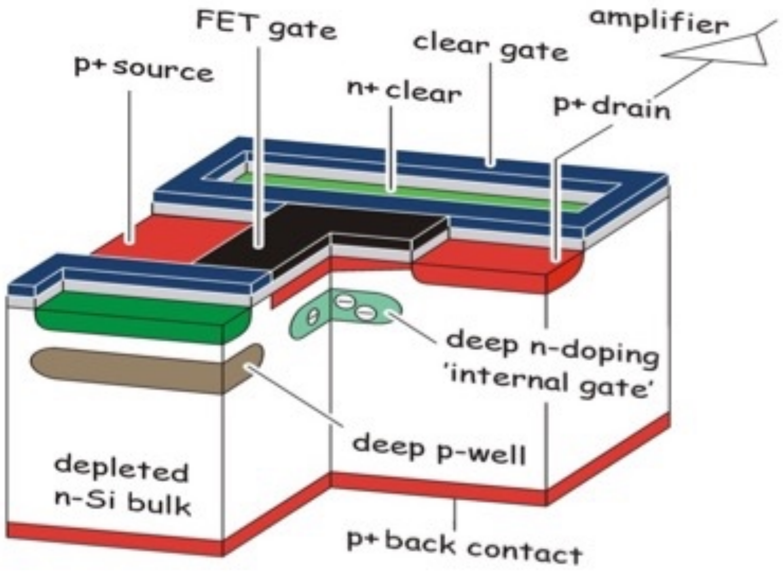
- Use of commercial technologies for replacement of sensor or even full hybrid (monolithic)
  - Currently in three experiments monolithic:
    - DEPFET in Belle-II
    - MiMOSA in STAR (only for moderate radiation suited)
    - ALICE ITS
    - …

DEPFET

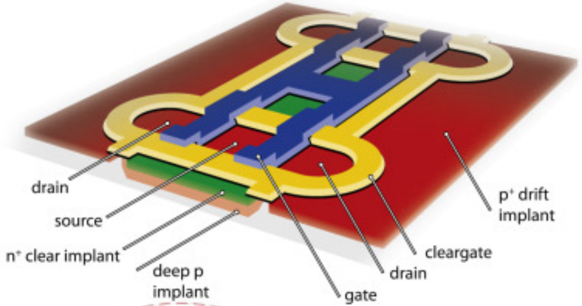
- Depleted p-channel FET on high resistivity substrate:
  - Each pixel is a p-channel FET integrated in a fully depleted bulk
  - Deep n-implant creates potential minimum under FET gate (internal gate)
  - Internal gate capacitively coupled to FET gate
  - Drain current is proportional to number of electrons collected in internal gate

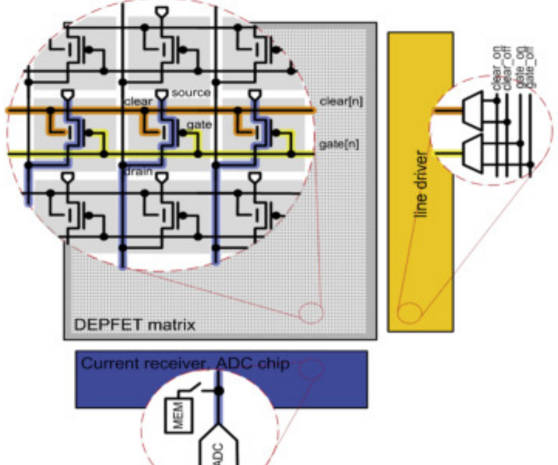
- Charge collection in “off-state”, readout on demand
- Clear process to remove stored charges
- Used in the BELLE II pixel detector upgrade

- Detection and internal amplification
- Small intrinsic noise
- Low power consumption



(Kemmer & Lutz, 1987)



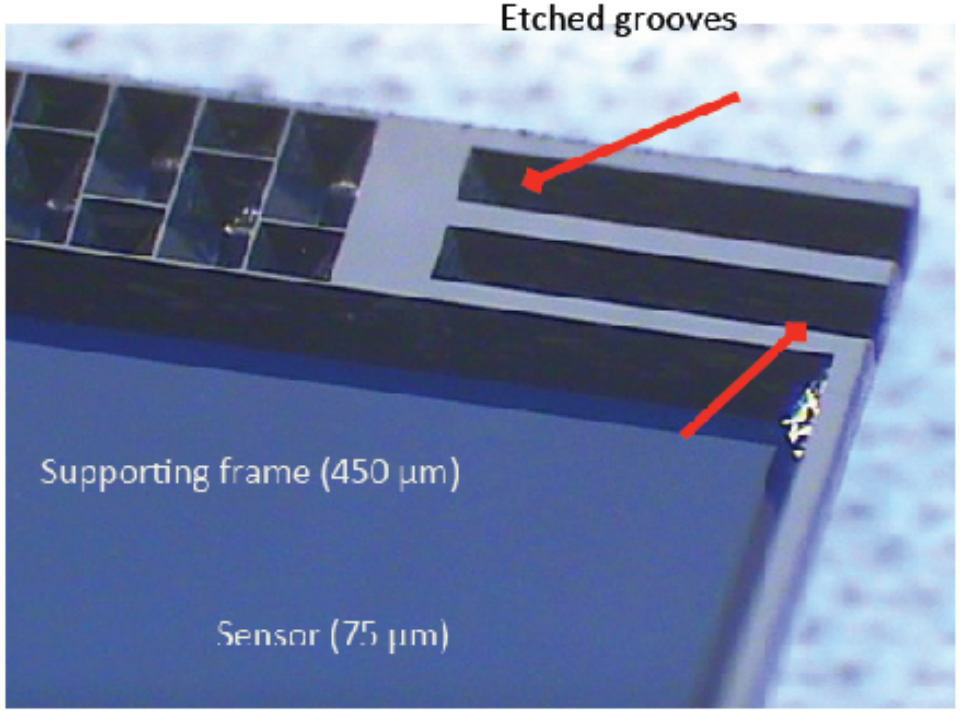


BELLE II PIXEL DETECTOR AT SUPERKEKB

Pixel detector based on **DEPFET** sensors

- 2 barrel layers (r=1.4 cm and 2.2 cm)
- Pixel size 50 µm x 75 µm
- Row-wise read-out (rolling shutter), 20 µs/frame
- Special thinning of the matrix area to reduce material budget (75 µm thick)

S. Tanaka, HSTD9, 2013



Radiation environment:

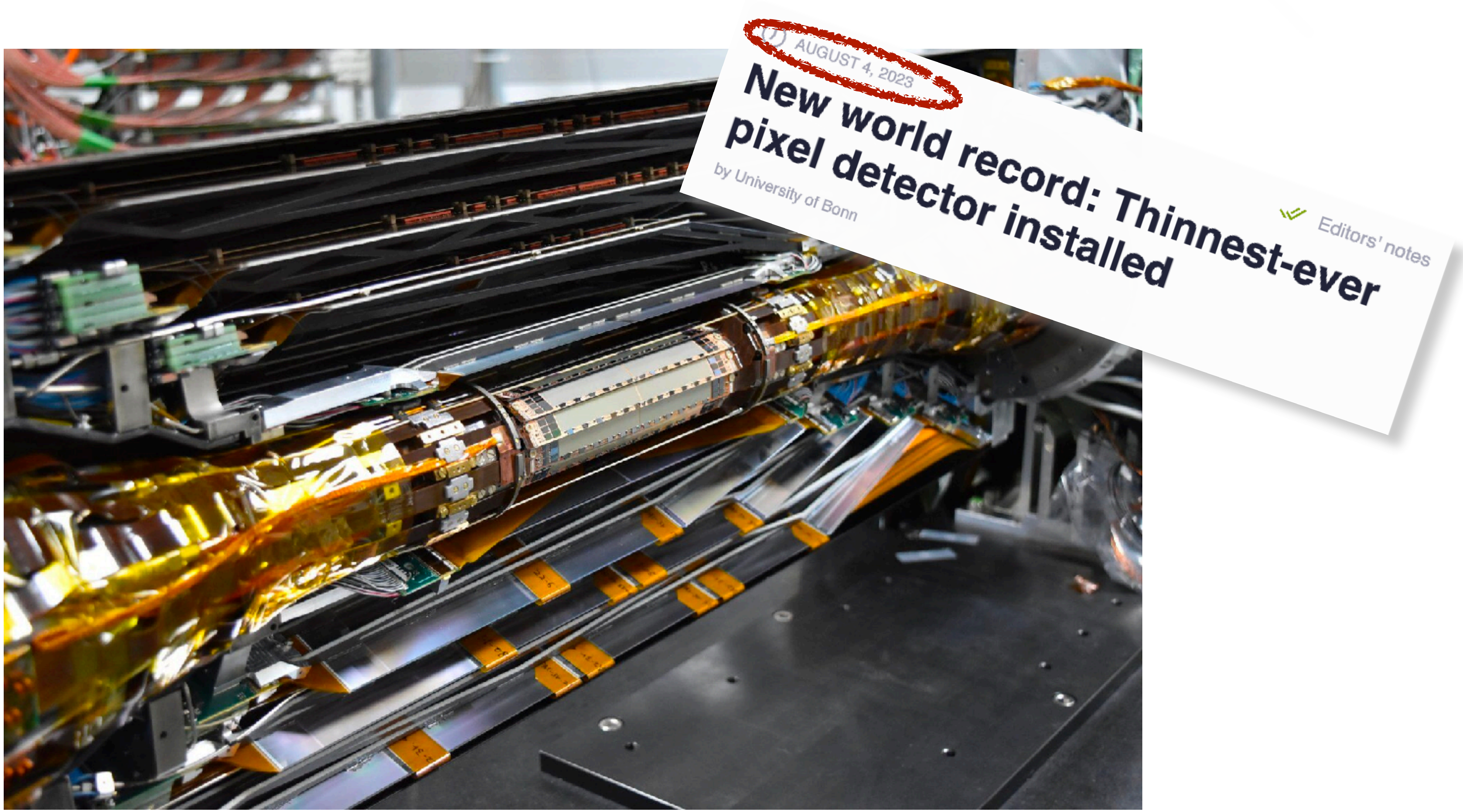
~ 1.9 Mrad / year

~ 1.2 10^{13} 1MeV n_{eq}/cm^2 per year

Material budget:

0.21 % X_0 per layer

FULL SILICON TRACKER FOR BELLE-2



AUGUST 4, 2023

New world record: Thinnest-ever pixel detector installed

by University of Bonn

Editors' notes

Drawback: very special technology which is not easily accessible

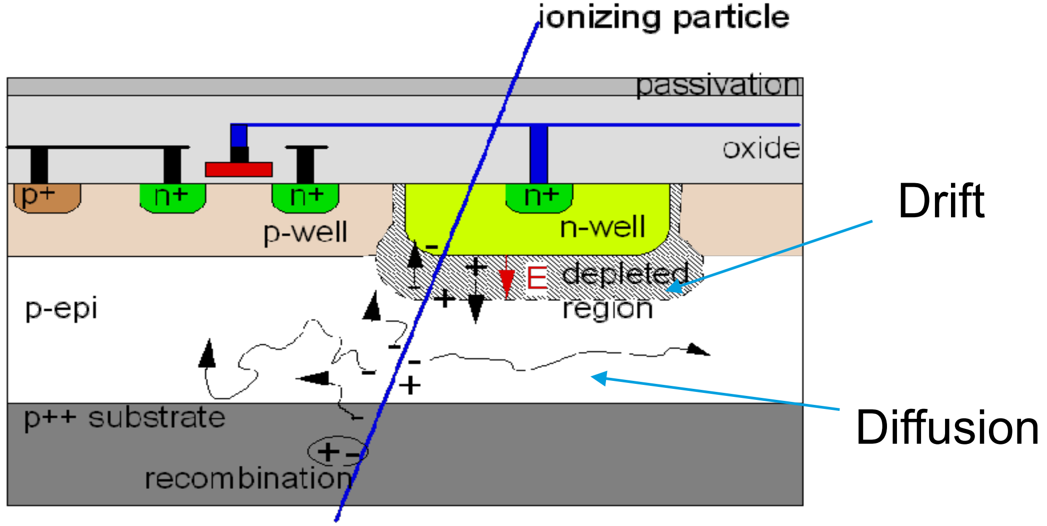
GOING FOR CMOS!!

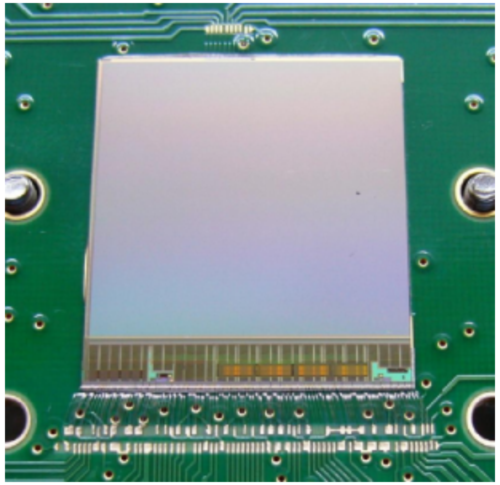
THE “CLASSIC” MAPS: MIMOSA

Monolithic = front-end electronics on same substrate as active sensor

Developments lead by IPHC created a number of monolithic pixel sensors of the MIMOSA family:

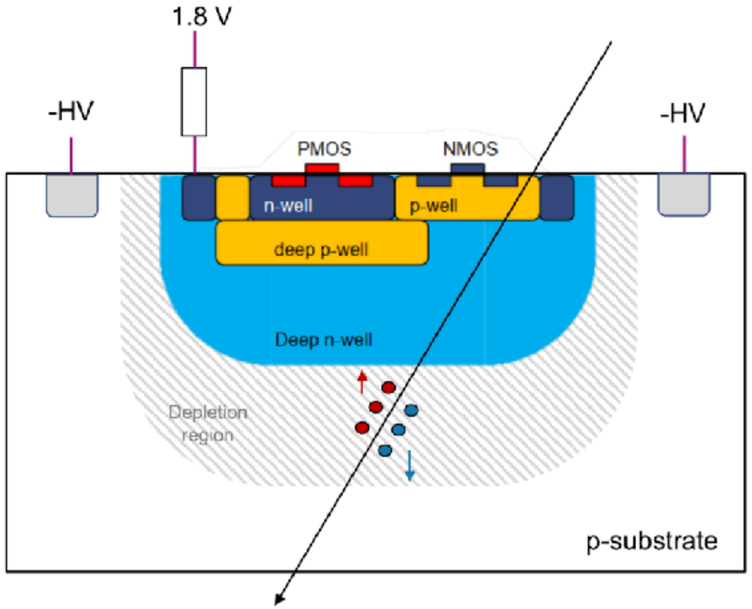
- First use of CMOS imaging process (CIS) for particle detection
- Epitaxial wafers with collection diode and few transistors per cell (size ~ $20 \times 20\ \mu m^2$), limited to NMOS transistors
- 0.35 μm CMOS technology with only one type of transistor
- Rolling shutter architecture (readout time O(100 μs))
- Limited radiation tolerance (< $10^{13}\ n_{eq}\ cm^{-2}$)





ULTIMATE chip for STAR HFT (IPHC Strasbourg)

DEPLETED MAPS (DMAPS)



Working principle of HV-CMOS sensors

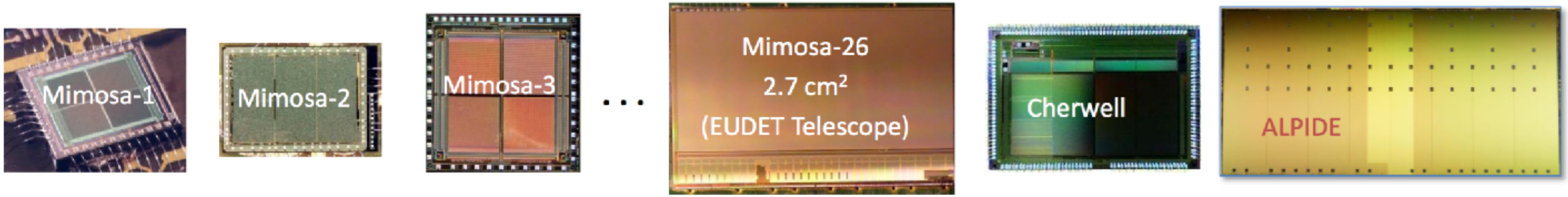
- Monolithic active pixel sensors (MAPS): in-pixel collection electrodes plus readout circuitry
- Depletion of sensitive area either through
  - high voltage (HV) with deep n-well isolating the electronics
  - high resistivity substrate (HR)
  - or both
- Charge is collected by drift, good for signal size and radiation tolerance
- But: risk of coupling circuit signals into input -> careful design required
- Being followed up by **many groups** working on next generation silicon detectors
  - Give only very few examples

A technology which could be used to build a **dream** tracker:

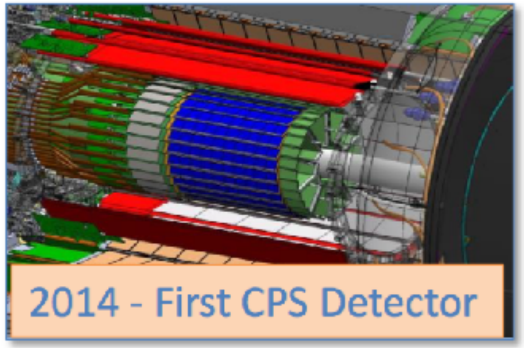
- fully monolithic
- high resolution
- thin material
- cost effective
- intelligent pixels
- possibly radiation hard

MAPS Evolution

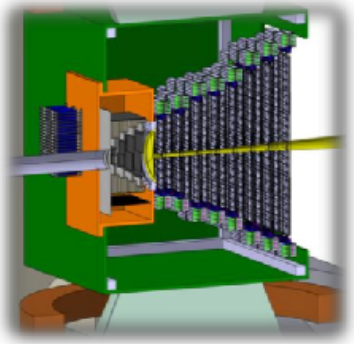
Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)



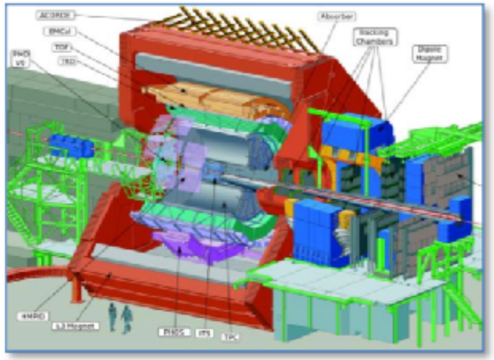
… several HI experiments have selected CMOS pixel sensors for their inner trackers



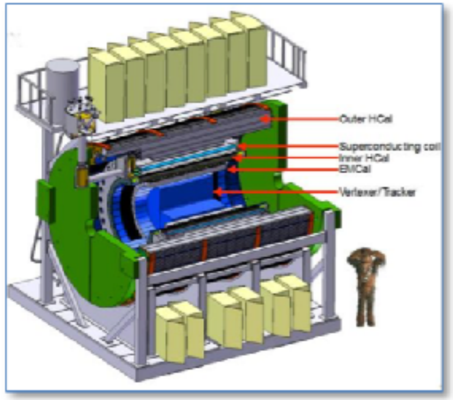
STAR HFT
$0.16\ m^2$ – 356 M pixels



CBM MVD
$0.08\ m^2$ – 146 M pixel



ALICE ITS Upgrade (and MFT)
$10\ m^2$ – 12 G pixel

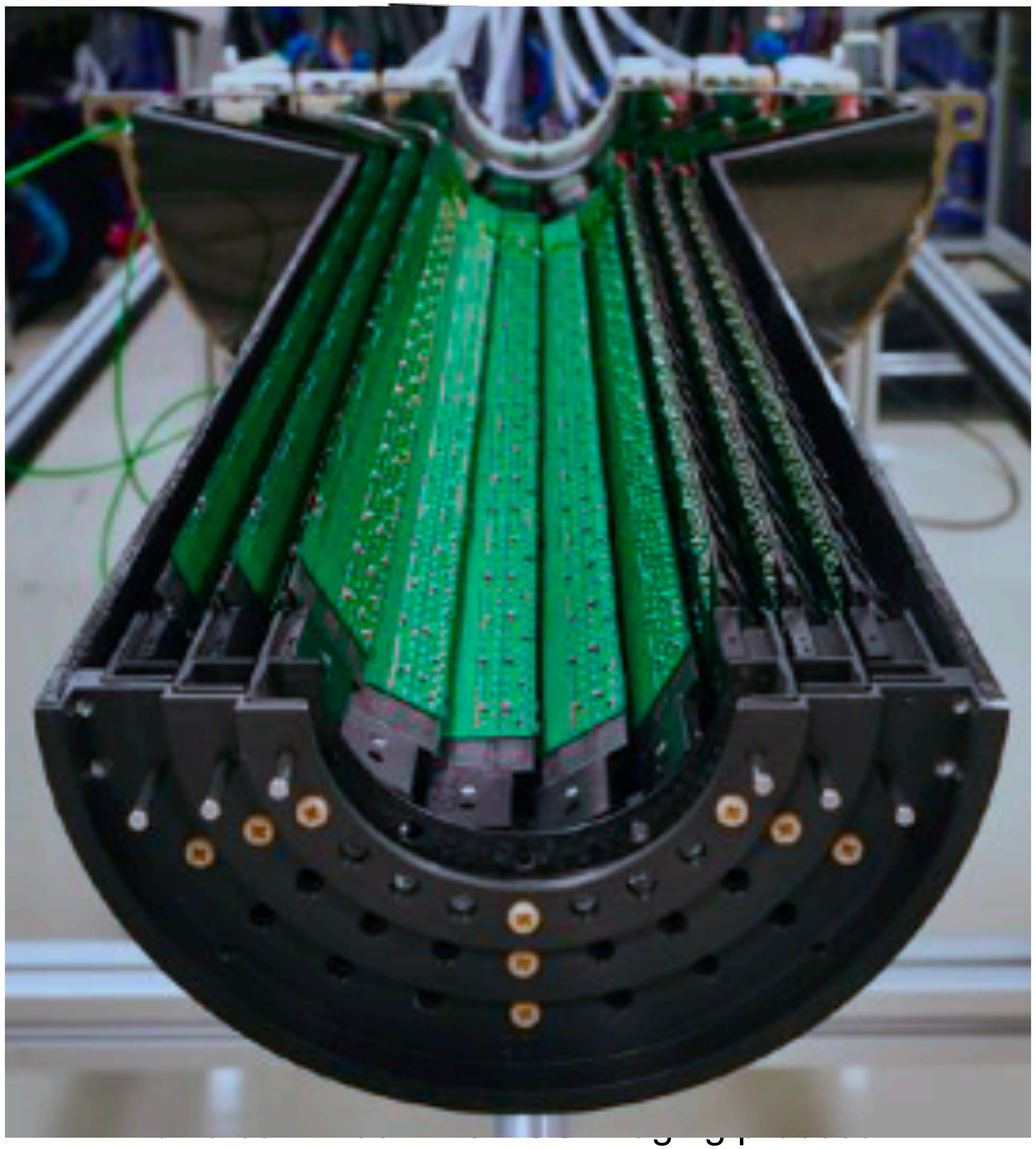


sPHENIX
$0.2\ m^2$ – 251 M pixel

ALICE INNER TRACKING SYSTEM UPGRADE

- 7 layers of CMOS **M**onolithic **A**ctive **P**ixel **S**ensors (MAPS):
  - Inner Barrel: 3 layers, 22–42 mm from IP, 0.35% X_0 per layer
  - Outer Barrel: 4 layers, 194–395 mm from IP, 1.1% X_0 per layer
- 10 m^2 of MAPS with about 12.5 GPix
- 50 kHz readout rate for Pb–Pb collisions

- **ALPIDE sensor:**
  - 180 nm CMOS imaging process by TowerJazz
  - 3 cm x 1.5 cm (1024 x 512 pixels) with thickness 50 µm for IB
  - Size of pixel pitch: 29 µm x 27 µm
  - Power consumption **less than 40 mW/cm^2**



InnoPool Project Tangerine

Towards Next Generation Silicon detectors

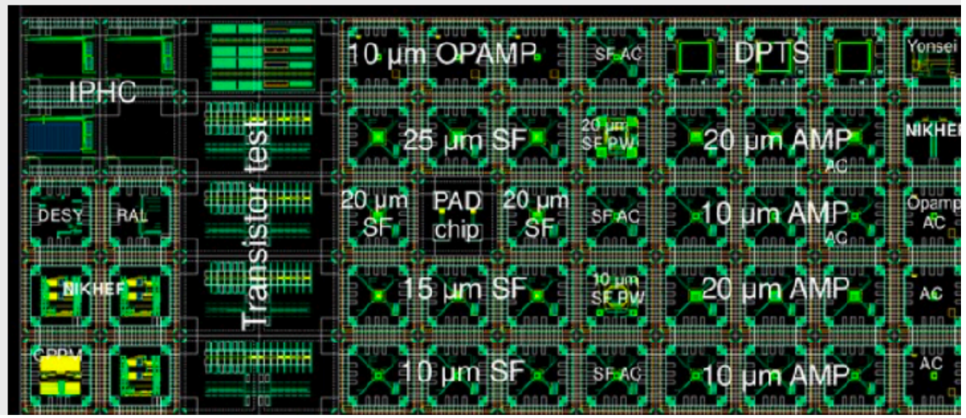
- Goal: develop next-generation low-material high-precision pixel detectors
  - Development & system integration for these technologies
  - Integrate hardware-based approaches for data reduction / AI on-chip
  - Foster expertise by networking & training next generation of detector physicists

Performance goals for MAPS

Position resolution	< 3um
Timing resolution	~ 1-10 ns
Material budget	~ 50um
Charge measurement for interpolation	

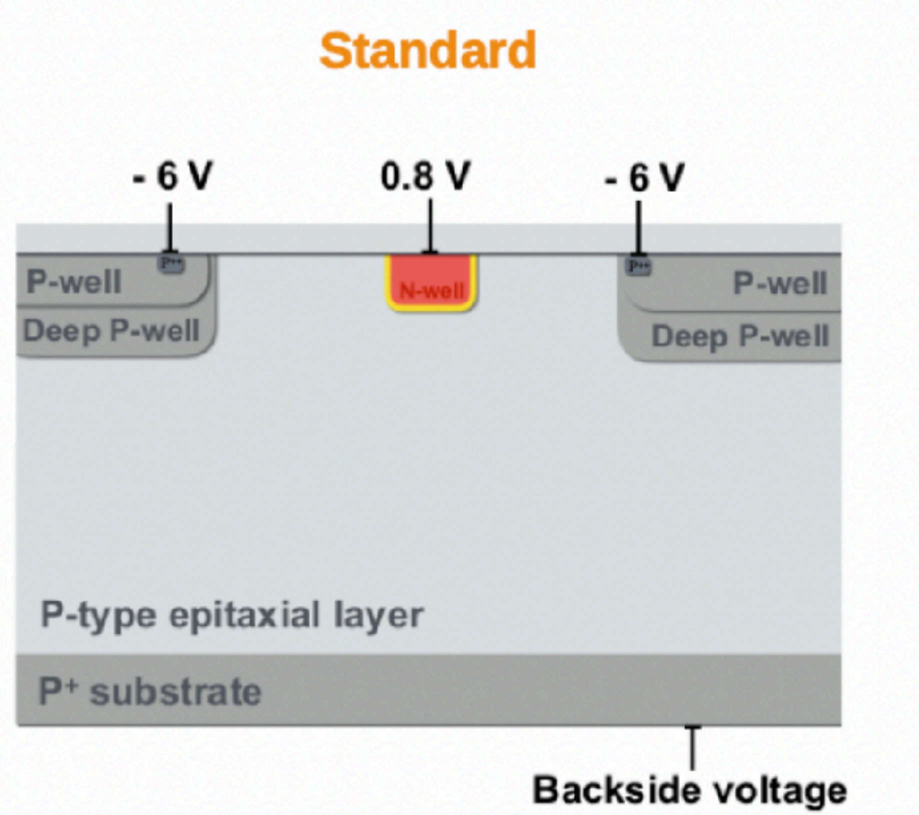
DESY - Monolithic pixel detectors in novel CMOS imaging technology

- Formed international collaboration for common submissions to foundry
- Common design effort for prototypes & test structures
  - Transistor test structures
  - Analog test pixels
  - Rolling shutter matrices
  - Front-end amplifiers

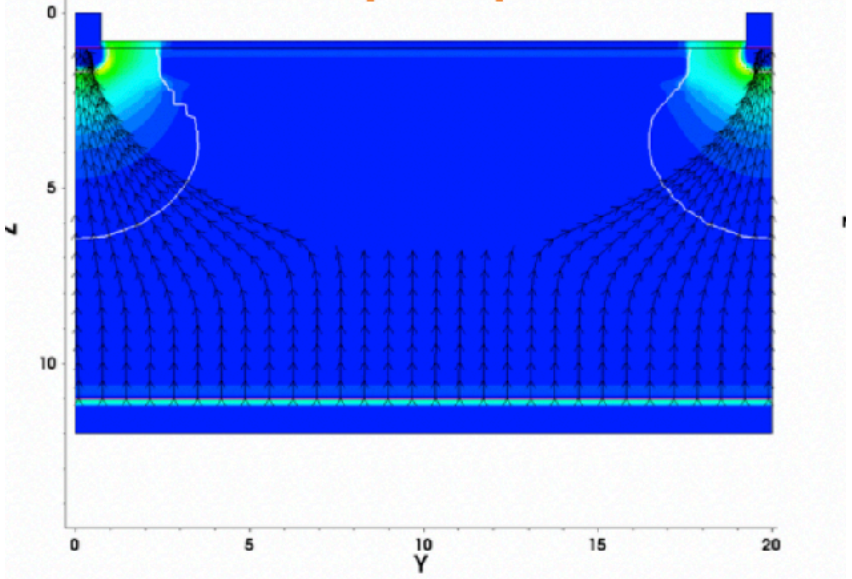


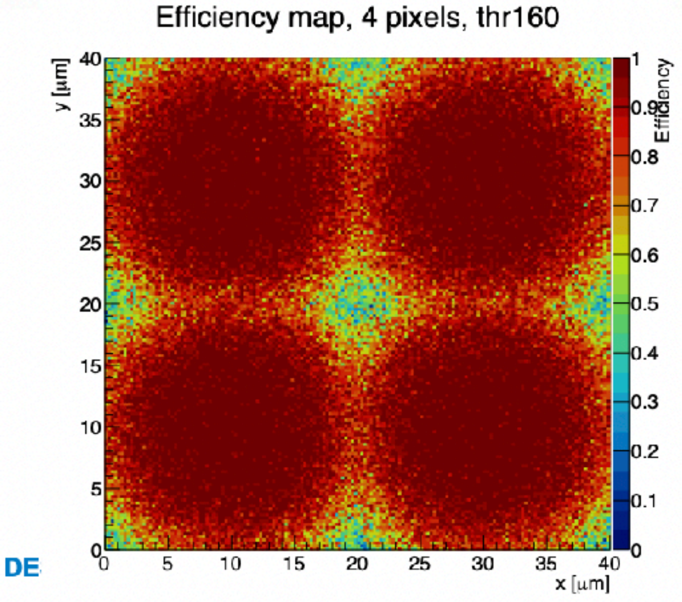
ONGOING

- Extensive simulations now being validated with testbeam data from first prototypes
- New prototypes H2M, D-I, D-II back from dicing and currently being investigated



TCAD and Allpix Squared

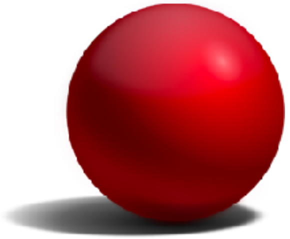




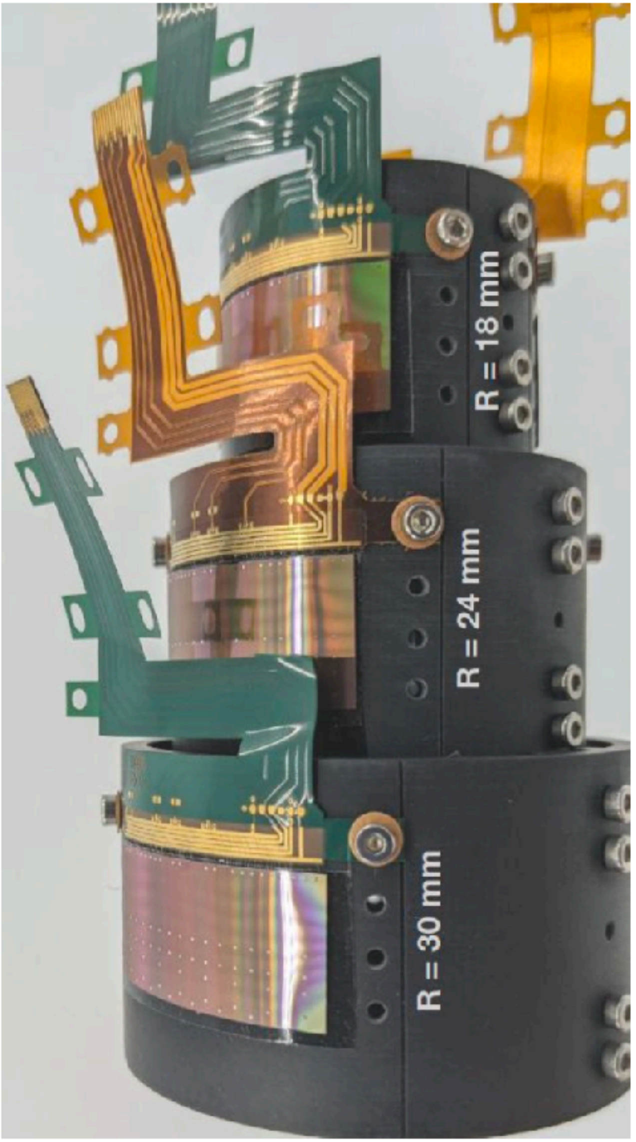
Really Cool Stuff

GOING BENT

- Perfect detector layer:



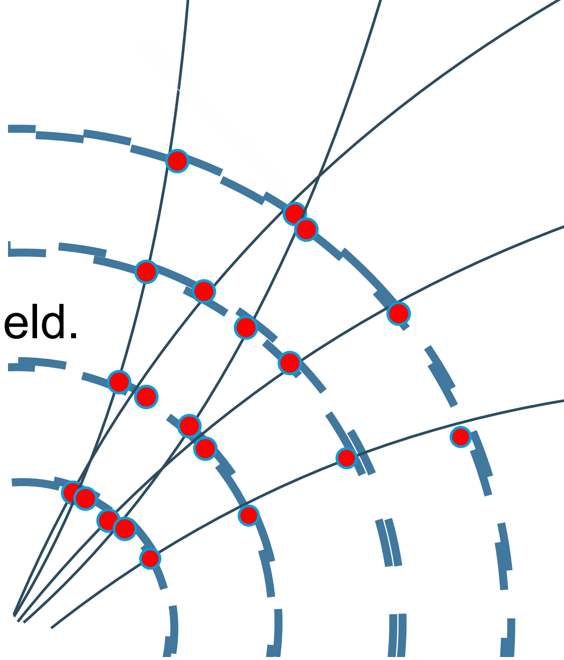
- Best approximation (as of now): half-cylinders of bent, ultra-thin Si sensors
- ALICE collaboration for ITS3:
  - MAPS sensor based on **65 nm technology**
  - Wafer-scale chips (up to 28 x 10 cm), fabricated using **stitching**
  - Sensor thickness 20–40 µm
  - Open-cell carbon foam spacers
  - Air cooling
  - Extremely low material budget: 0.07% X_0 per layer



Stay tuned!
Or better: join the fun in silicon detectors

ALICE upgrades LS2 arXiv:2302.01238 ITS3 Letter of intent CERN-LHCC-2019-018

SUMMARY

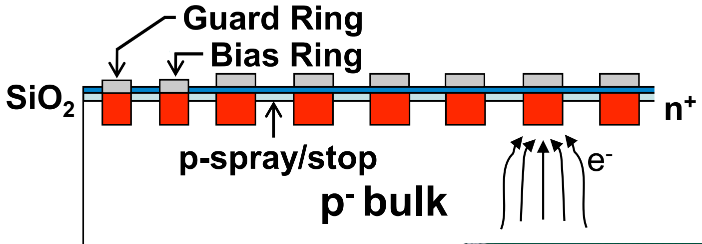


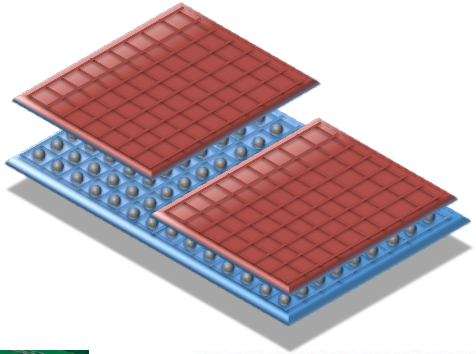
Tracking Detectors

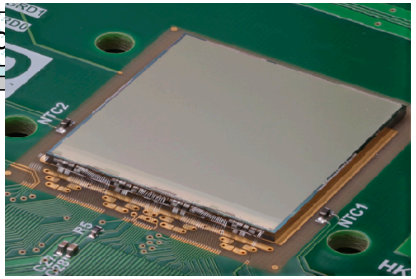
- Precise measurement of track and momentum of charged particles due to magnetic field.
- Mostly based on ionisation

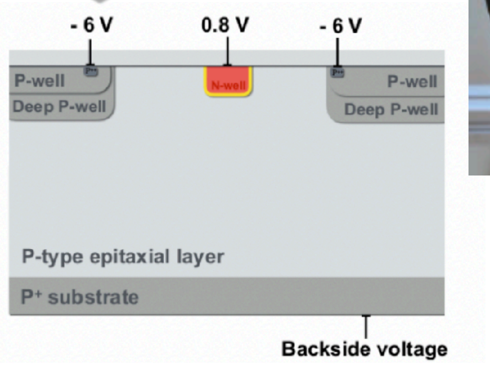
Semiconductor Detectors

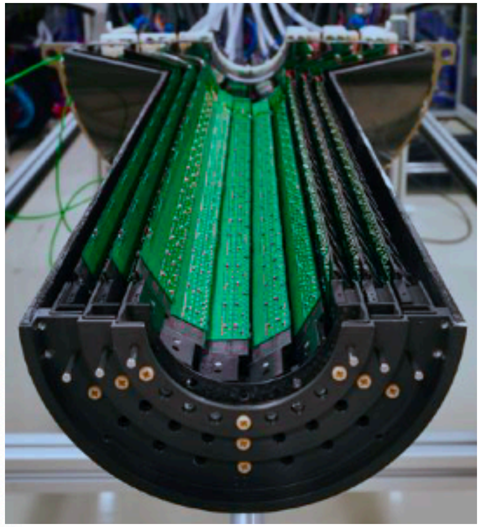
- In particle physics mostly based on silicon
- Pixel and strip detectors for innermost regions of experiments

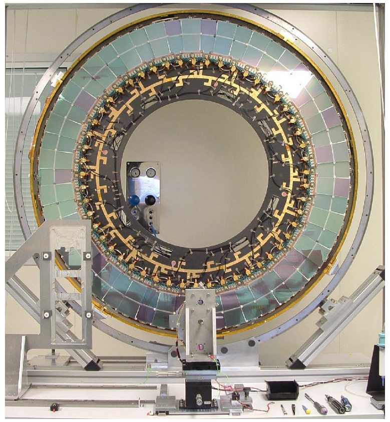


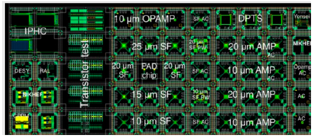












WHAT IS CMOS?

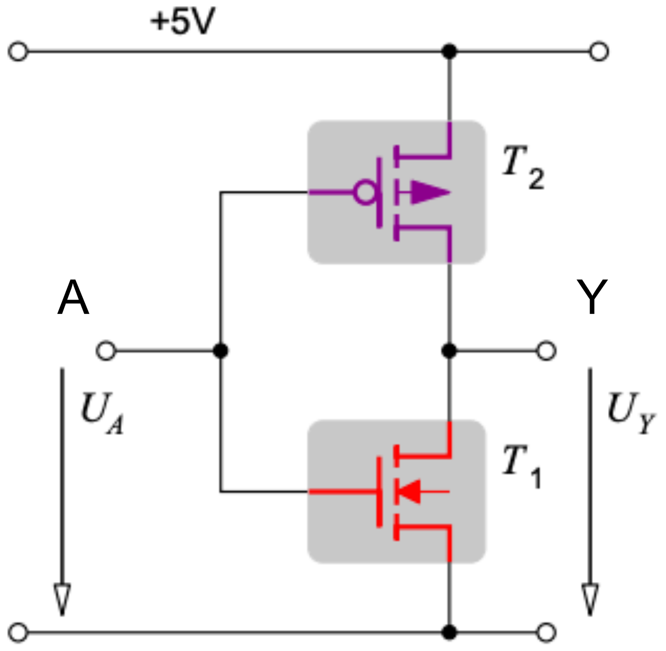
Complementary **M**etal **O**xide **S**emiconductor

- Integration of n-channel (NMOS) and p-channel (PMOS) field-effect transistors on a silicon chip
- Semiconductor process for the cost-effective production of integrated digital, analogue and mixed-signal circuits
- Production in the wafer process

Lithography: process used to transfer patterns to each layer of the IC

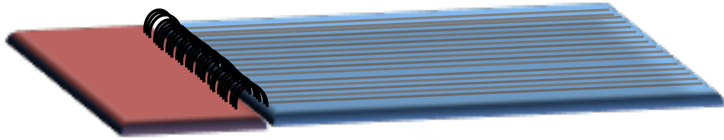
- Designer:
  - Drawing the layer patterns on a layout editor
- Silicon Foundry:
  - Masks generation from the layer patterns in the design data base
  - Printing: transfer the mask pattern to the wafer surface
  - Process the wafer to physically pattern each layer of the IC

Simple Example: NOT-Gatter

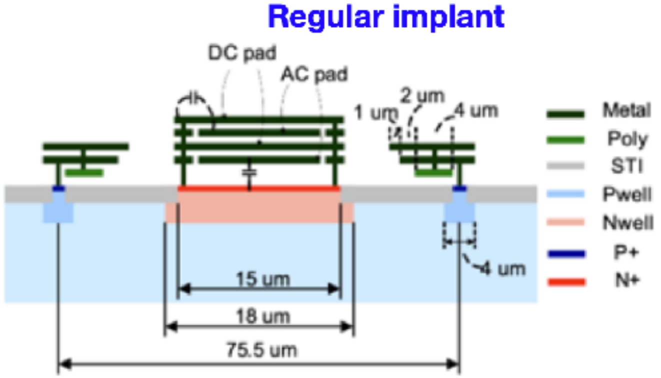


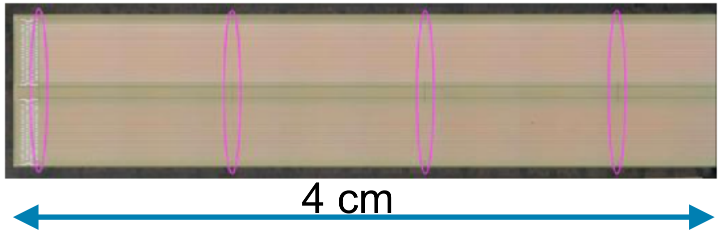
- ➡ One of the transistors is always disabled
- ➡ Low power consumption
- ➡ Hardly any current flow through both transistors

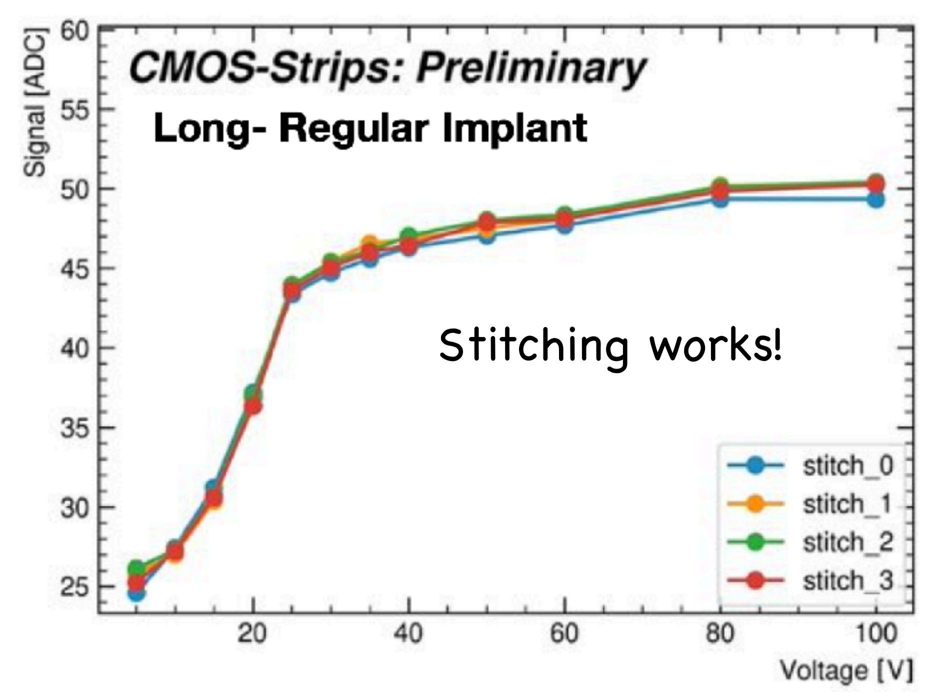
STRIPS - PASSIVE CMOS



- How to address large area silicon detectors in future ? CMOS, fully monolithic ?
  - First stitched strip sensors produced on 8" wafer by a commercial high volume foundry
    - overcomes the exposure-field limitation by merging multiple design structures
  - L-Foundry 150 nm process (deep N-well/P-well)
    - Wafer Resistivity: > 2 kΩ·cm
    - Float-Zone silicon
    - Backside passivation

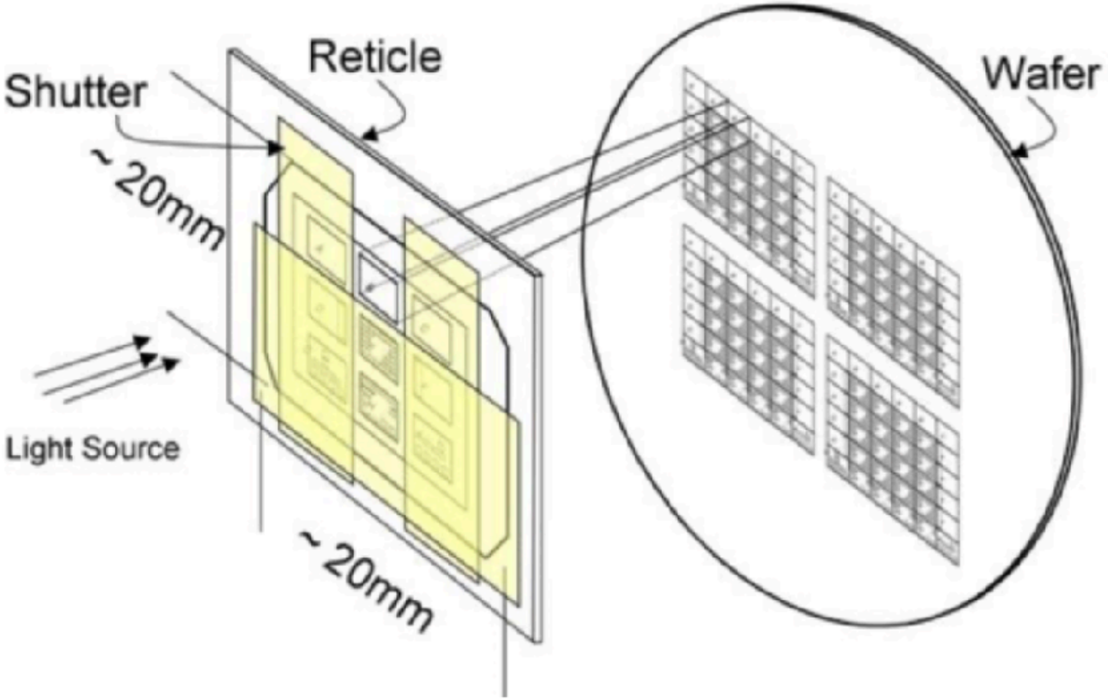


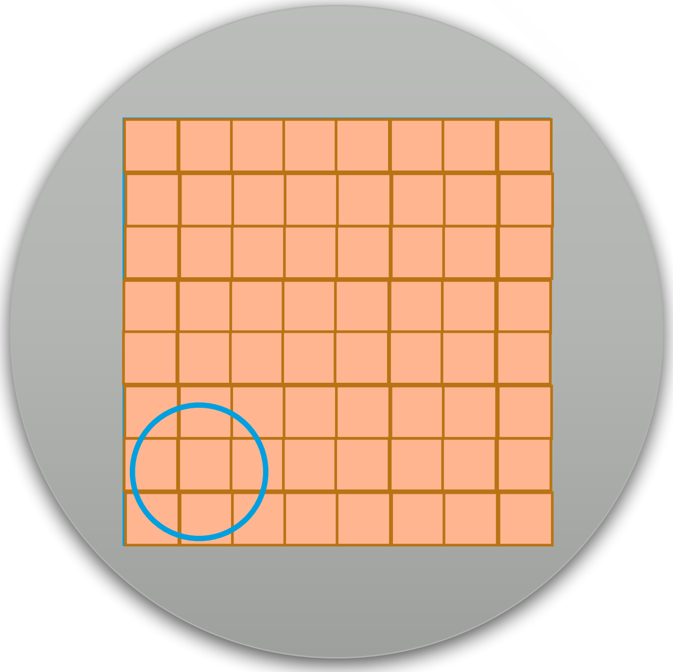




Very promising results for IV, CV, source measurements and test beam.
Also after irradiation looks good …

WHAT IS RETICLE STITCHING ?





- Stitching merges multiple design structures on a wafer during the photolithographic process -> creates large sensors/chips
- Requires that design can be subdivided into smaller blocks (e.g. corner, edge and centre region) which can be separately implemented on a reticle