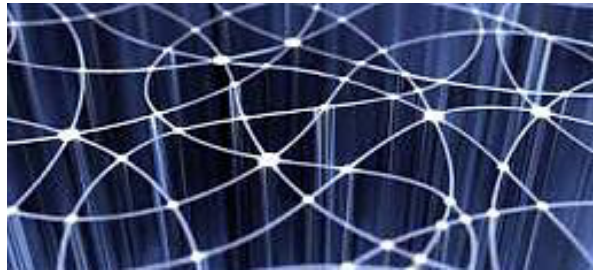


High-performance Signal and Data Processing: Challenges in Astro- and Particle Physics and Radio Astronomy Instrumentation



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The RHINO Digital Processing Skills Development Initiative: An integrated review of the platform, resources and training structures

This paper presents an integrated perspective, and progress review, of the Reconfigurable Hardware Interface for computing and radio (RHINO) project[1] and the skills development programme and related development resources for this initiative. The RHINO platform is designed around providing a comparatively low cost FPGA-based reconfigurable computing platform suited for a variety of Software Defined Radio (SDR) and Radio Astronomy (RA) back-end processing applications. RHINO is planned to provide a level of compatibility with the more powerful Reconfigurable Open Architecture Computing Hardware (ROACH) platform, and is intended to accommodate a trajectory for novice developers that decide to delve more deeply into RA processing to transition to ROACH and other high-end FPGA-based platforms.

The work carried out on the RHINO HDL skills development initiative is separated into four main interdependent aspects: 1) development of firmware and software, and hardware revisions, of the RHINO platform and its system software; 2) establishing an effective tool flow (integration and configuration of existing tools) and programming solutions that are appropriate for both training and development of applications; and 3) providing compatibility with existing frameworks such as the CASPER MSSGE Simulink toolflow[2] - tools and GNU Radio[3], and 4) example applications, performance testing, and preparation of training materials including support for migration to, and integration with, other platforms. A holistic systems view of these components is explained, and briefly mentions the various projects that fit into this higher-level initiative.

The paper proceeds to report on the progress achieved, challenges encountered and proposed solutions to these. We hope that this presentation will inspire comment and feedback to us in terms of our design choices, and we invite requests or suggestions for training support resources, either at the undergraduate or postgraduate level, which would be useful to the broader field of reconfigurable computing data processing.

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Primary author: Dr WINBERG, Simon (University of Cape Town)

Presenter: Dr WINBERG, Simon (University of Cape Town)