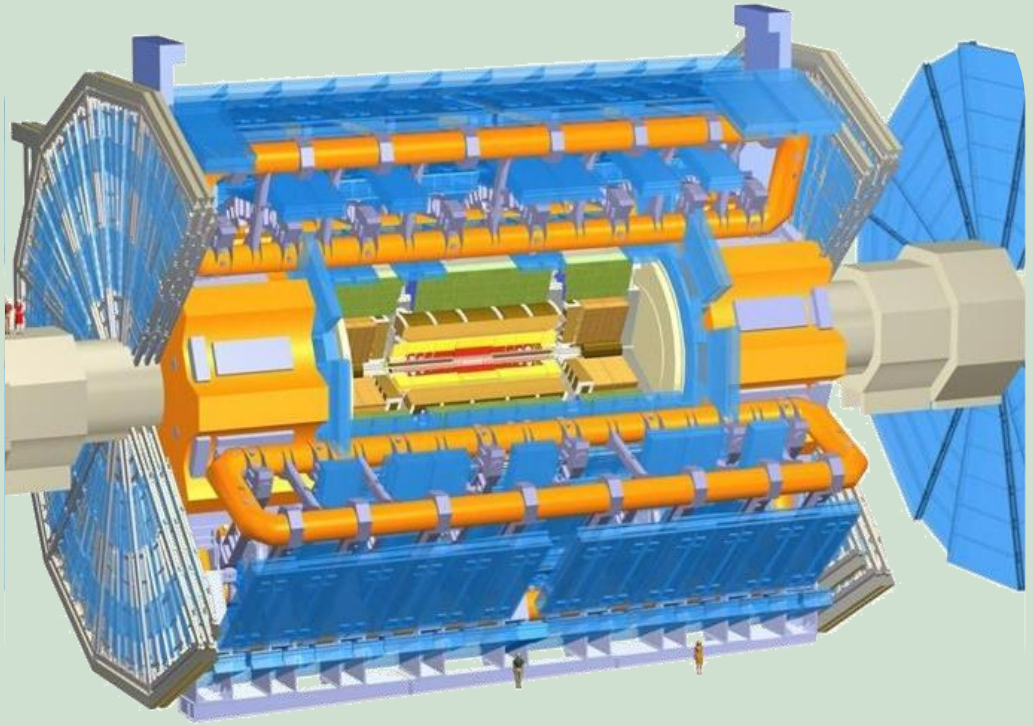
An Overview of the TileCal Upgrade

Robert Reed on behalf of ATLAS TileCal Community

OVERVIEW

- Introduction
- Upgrade Motivation
- Old/New Architecture
- Demonstrator Project
- Summary

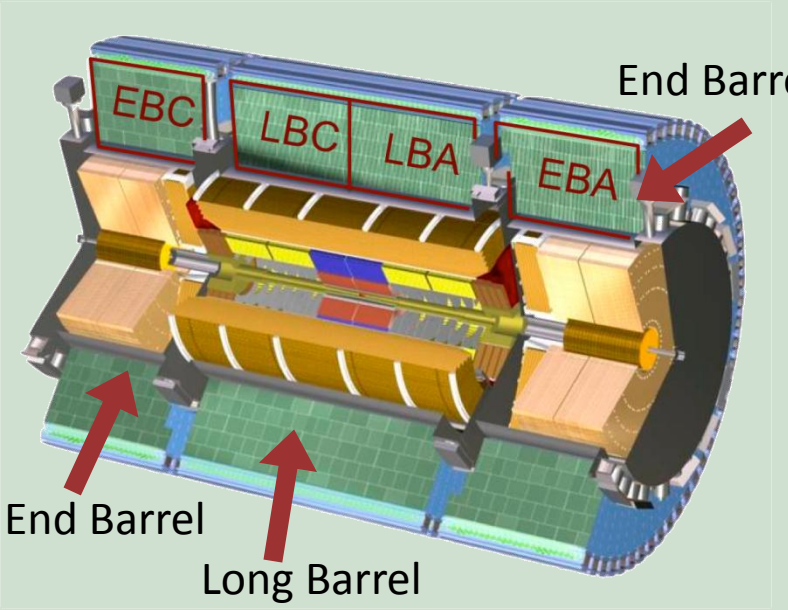


ATLAS

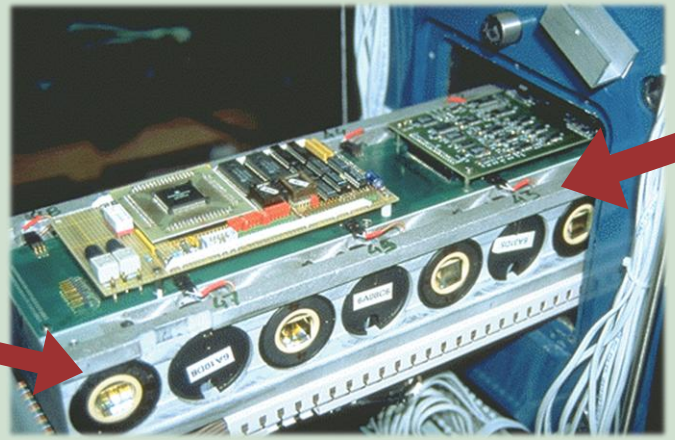
Length : 46 m
Diameter : 25 m
Weight : 7000 t
100 million channels

3km cables
Over 4000 members
38 Countries
174 Universities and labs

TILE CALORIMETER

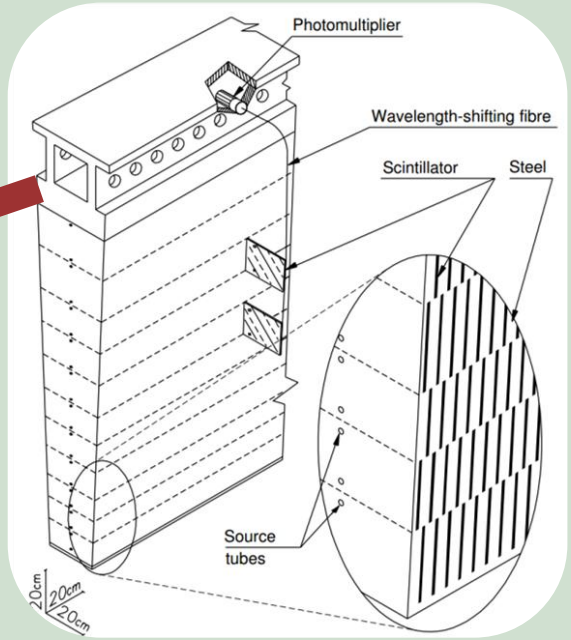


- Four logical partitions
  - EBC, LBC, LBA, EBA
- Measures energies of Hadrons and Jets
- Sandwich of steel absorber and plastic scintillating tiles
- Wavelength Shifting Fibres to PMTs on each side

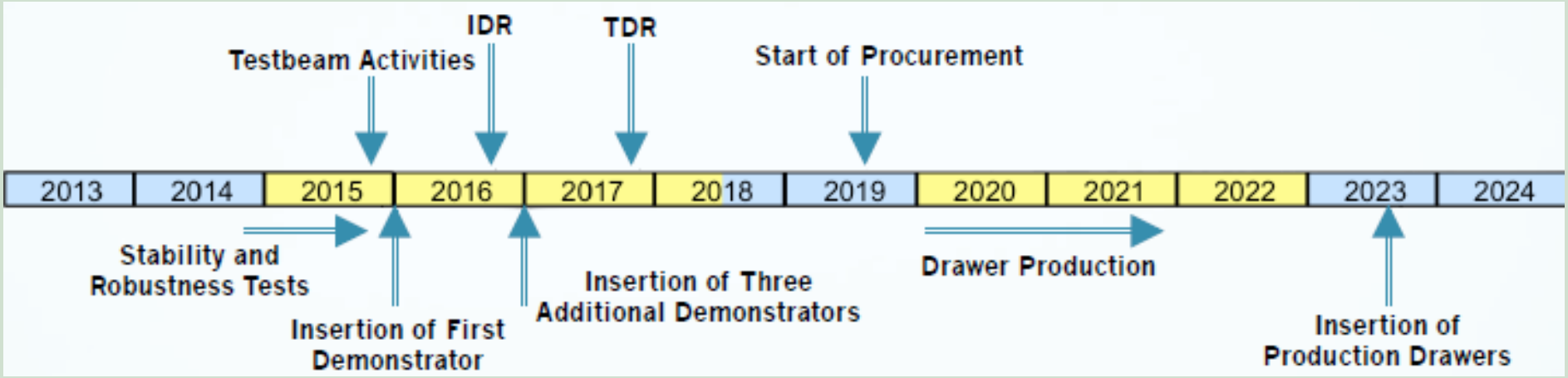


PMTs
Totalling 9852

Super-drawer
in outer layer



MOTIVATION FOR UPGRADE

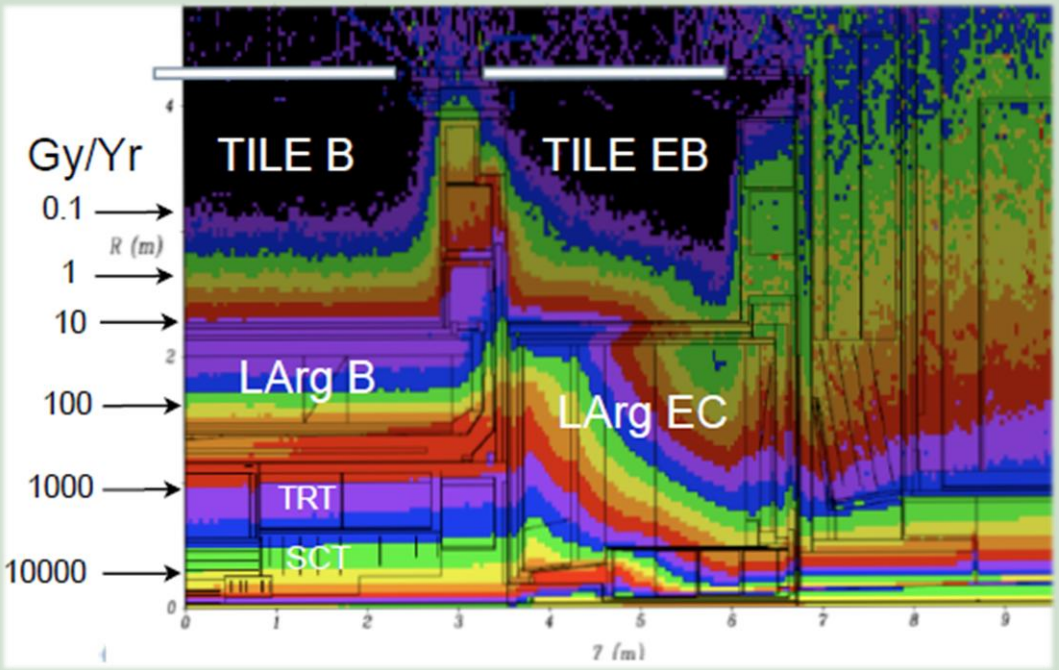


- Phase II in 2023 – High Luminosity LHC
- Increased designed luminosity by a factor of 5 from $10^{34}cm^{-2}s^{-1}$
  - More events accepted with current criteria
  - More data generated ~500X
  - Better precision and granularity needed
    - Triggering and event selection

	Present	Phase-II
Total BW	~165 Gbps	~80 Tbps
No. Fibres	256	8192
BW/drawer	640 Mbps	320 Gbps

MOTIVATION FOR UPGRADE

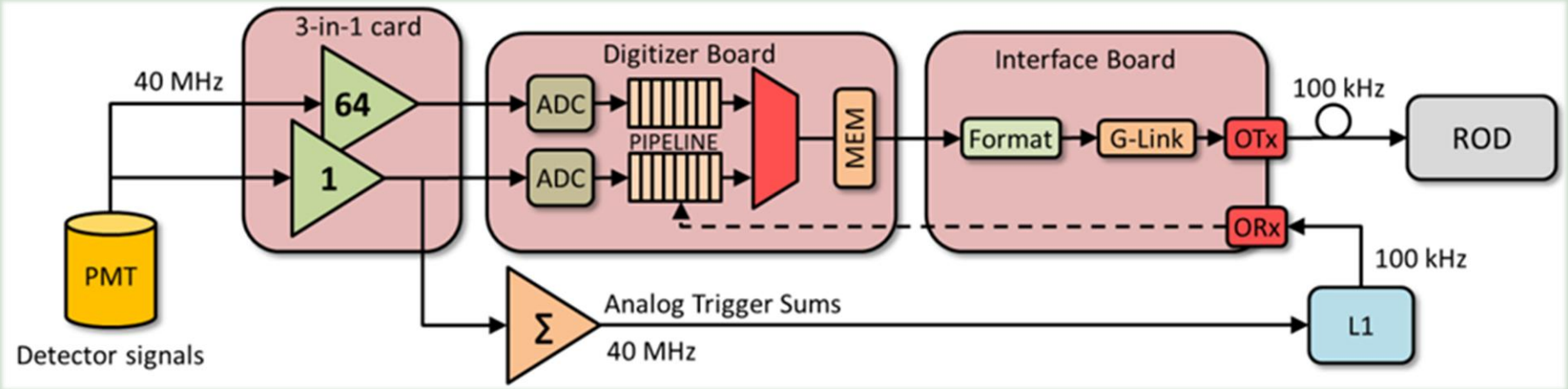
- Need better radiation tolerance
  - SEE (Single Event Effects)
  - NIEL (Non-Ionizing Energy Loss)
  - TID (Total Ionizing Dose)
- Ageing of components (>10 years)
- Simplify and Reduce maintenance needs
- Accessibility for ALARA considerations
  - As low as reasonably achievable



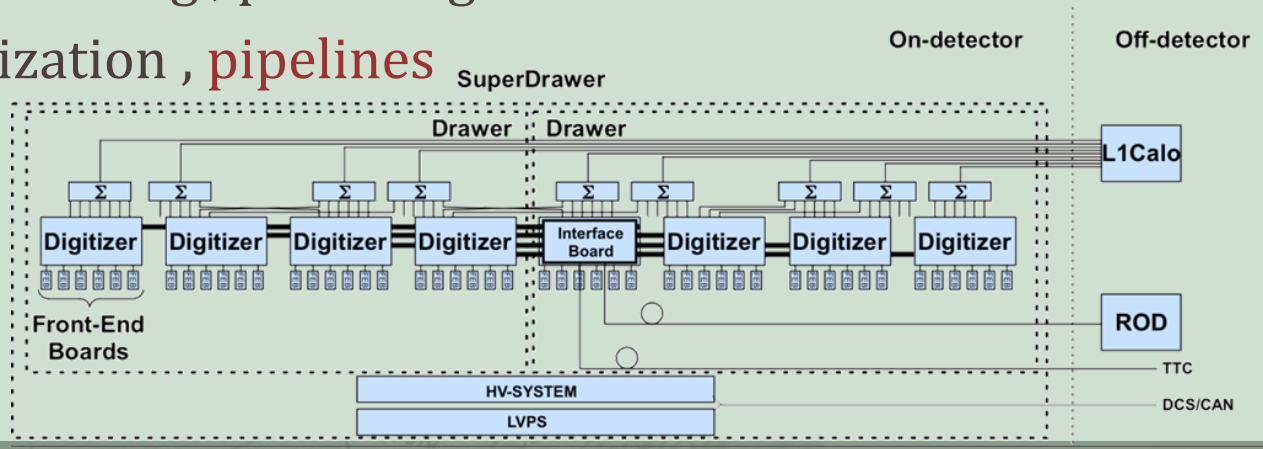
Phase 2 Radiation Tolerance Requirements (Estimate), TileCal HV_Opto					
Type	Simulated Dose/Yr	Simulation Safety Factor	Low Dose Rate Safety Factor	Lot Variation Safety Factor	Total 10 Year Operation
TID	8.13E-01 Gy/yr	1.5	5	4	2.44E+02 Gy
NIEL	7.62E+10 n/cm^2/yr	2	1	4	6.10E+12 n/cm^2
SEE	1.85E+10 p/cm^2/yr	2	1	4	1.47E+12 p/cm^2

CURRENT ARCHITECTURE

Present Architecture

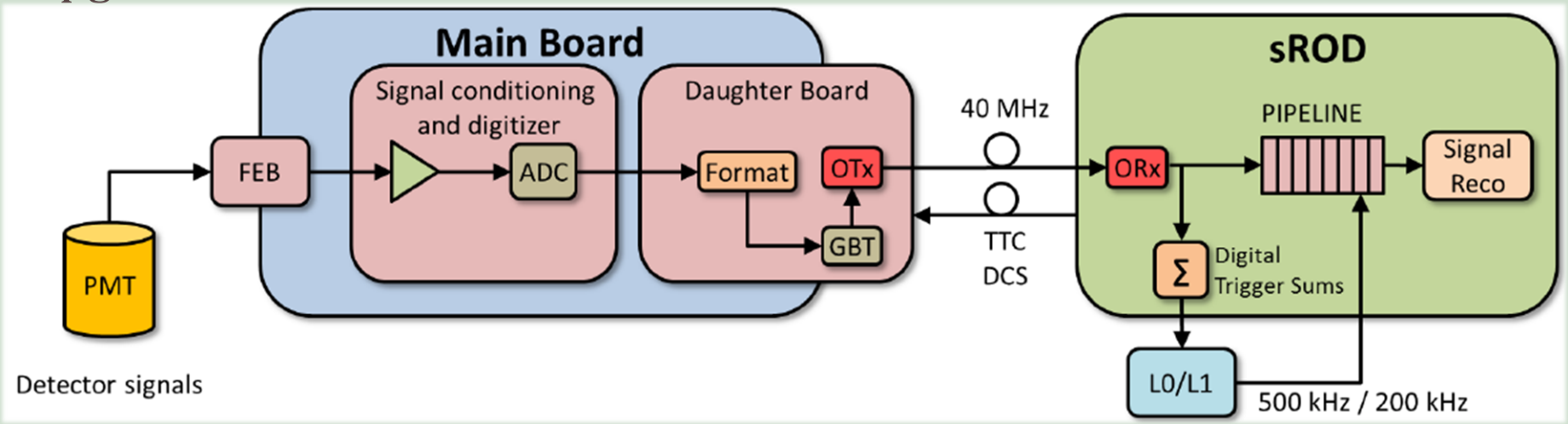


- 3-in-1: shaping, amplification and integrating
  - Trigger sums have 1 GeV energy precision
- Mother board: programming , powering of FE boards
- Digitizer cards: Digitization , pipelines
- Interface card:
  100 kHz to ROD

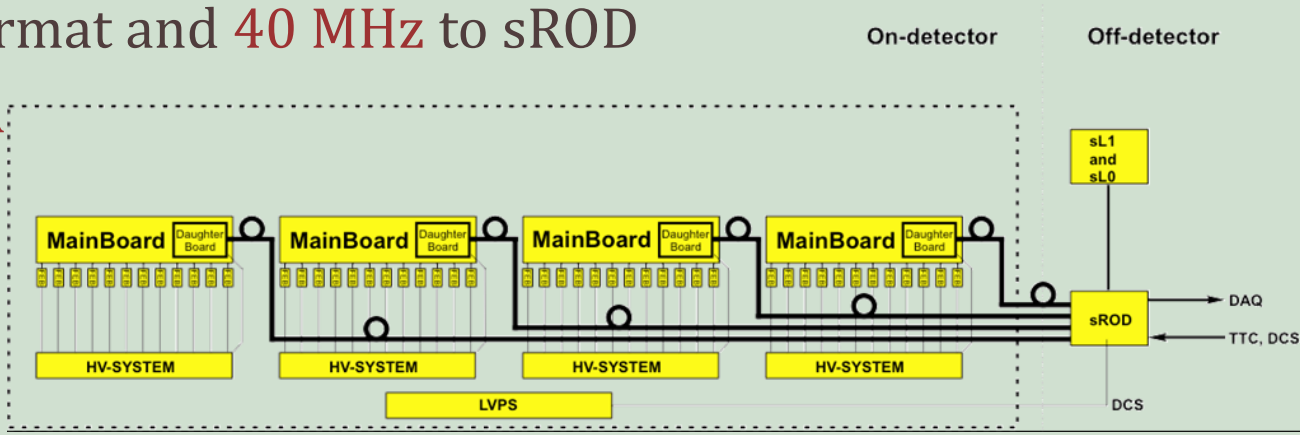


PHASE-II ARCHITECTURE

Upgrade Architecture

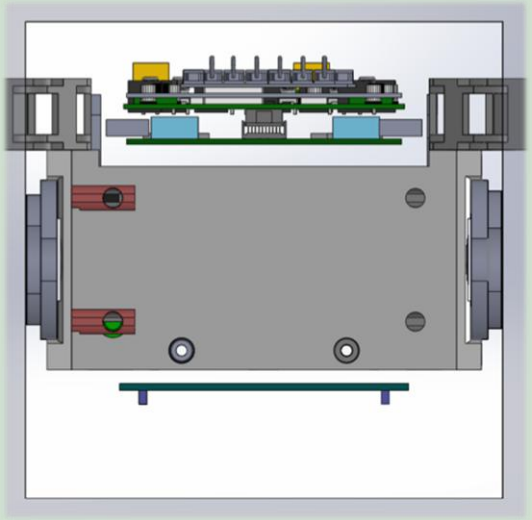


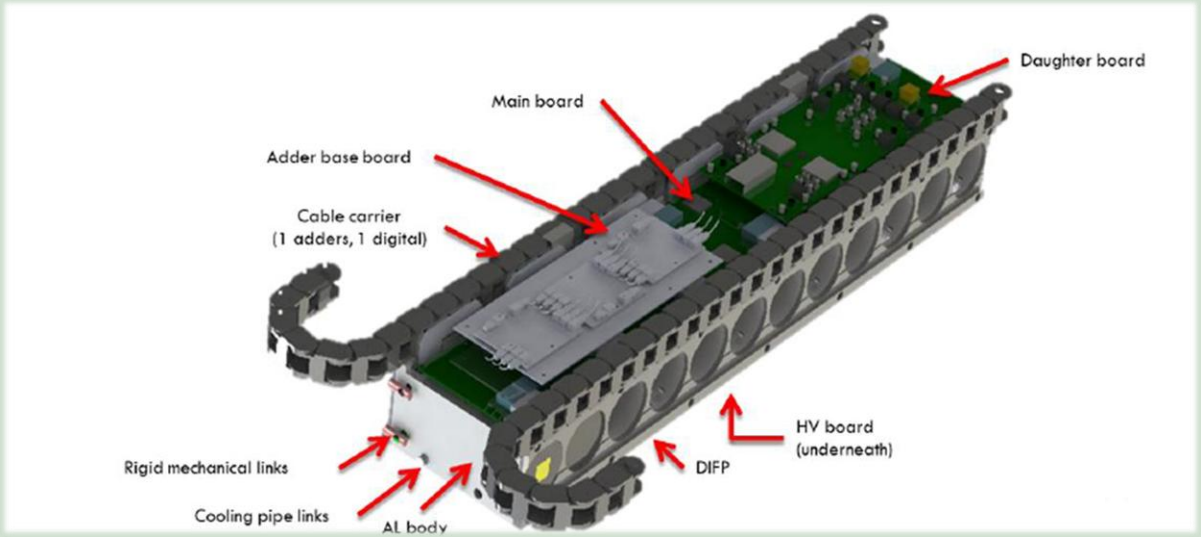
- Front end board: Three options available
- Main board: Conditioning and digitization
- Daughter board: Format and 40 MHz to sROD
- sROD: Pipeline, L0A
  - Digital Precision at tile cell energy reconstruction



MINI-DRAWERS

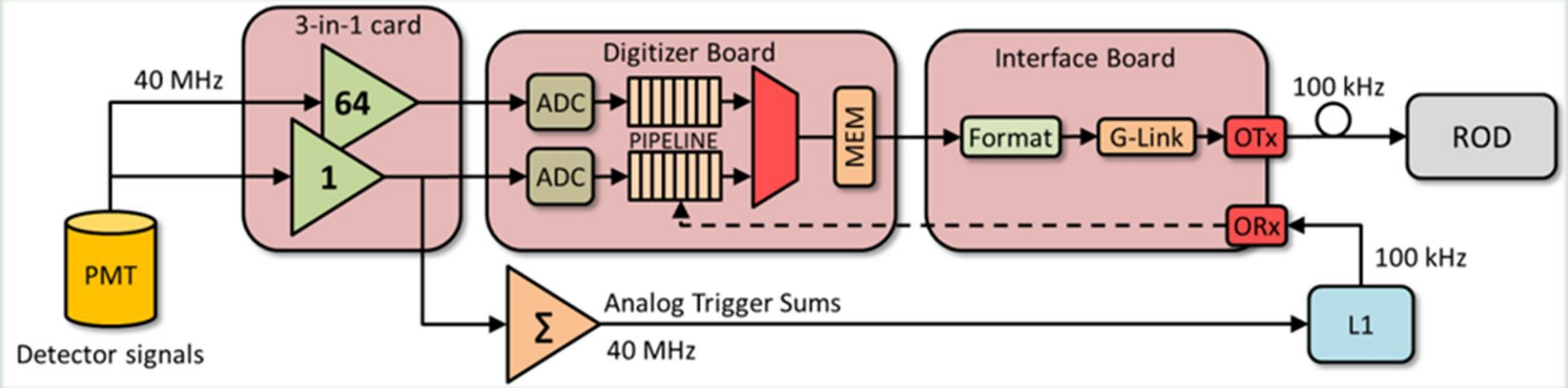
- Super drawer splits into 4 mini-drawers
  - Improves operation, maintainability and handling
  - Internal cooling
  - Cable carrier for easier insertion/extraction
- Each draw has:
  - 12 Photo Multiplier Tubes (PMTs) connected to 12 front end boards
  - 1 Main Board + 1 Daughter Board
  - 1 HV regulation board
  - 1 Adder base board + 3 adder cards (demonstrator only)



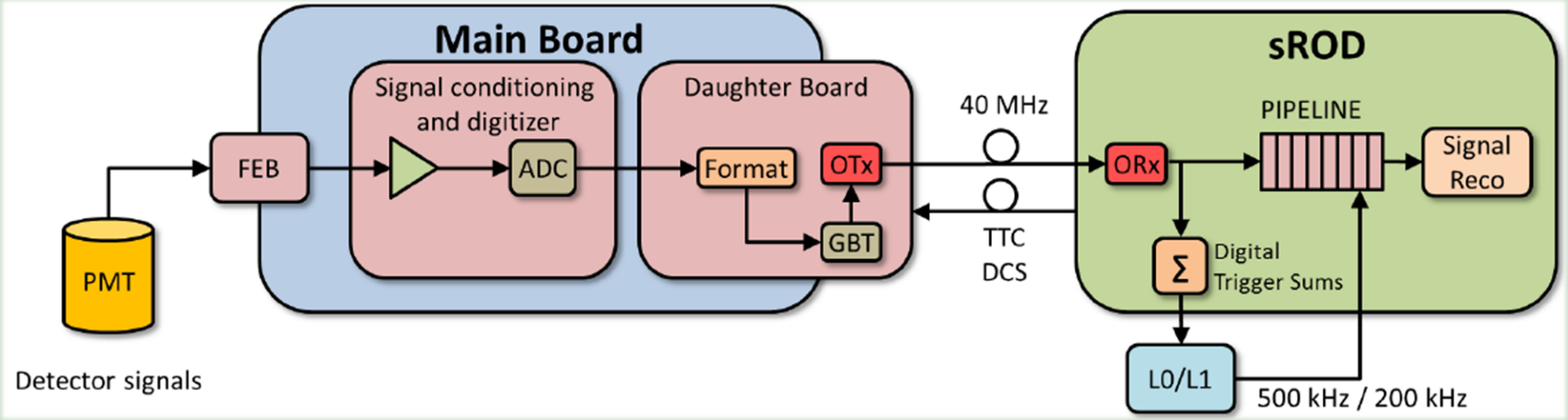


ARCHITECTURE COMPARISON

Present Architecture

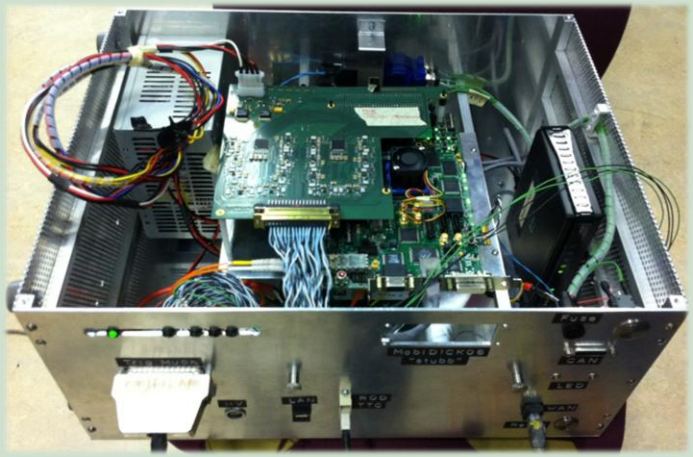


Phase-II Architecture



TILE DEMONSTRATOR PROJECT

Test bench at CERN containing demonstrator proto-type

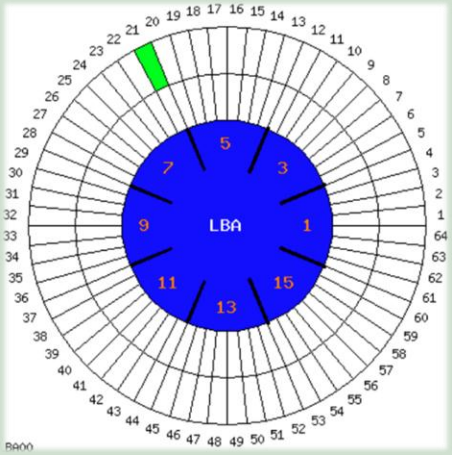


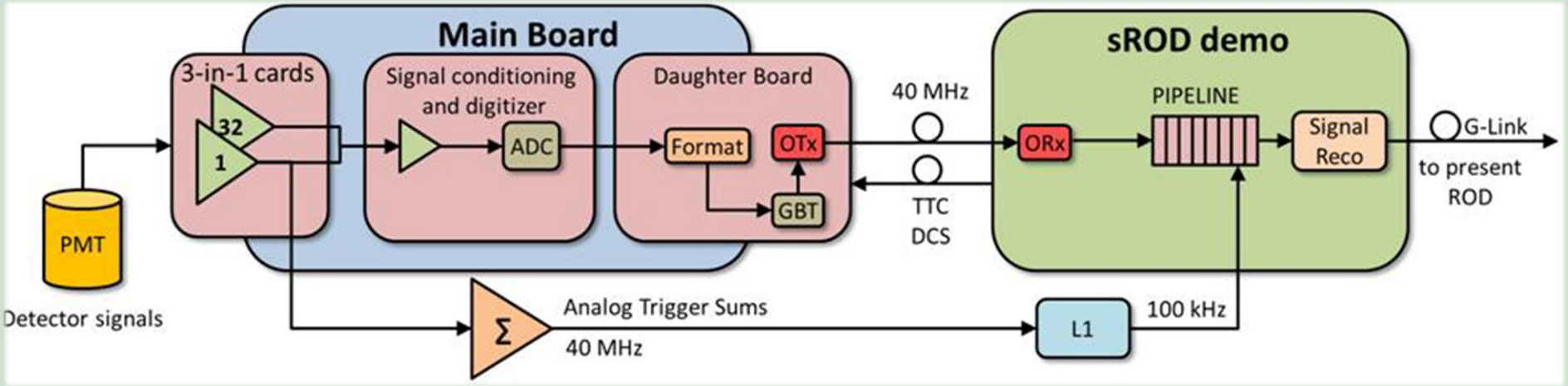
Mobile unit to test and consolidate new front end electronics

A Portable ReadOut ModulE for Tilecal ElectrOnics
PROMETEO

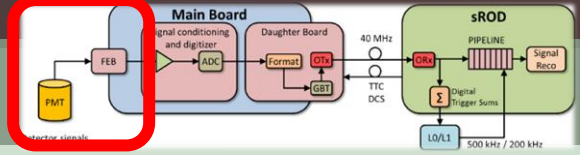
TILE DEMONSTRATOR PROJECT

- Evaluation and qualification of the technology before the complete replacement associated electronics
- Similar as possible to Phase-II with backward compatibility (analog trigger = 3-in-1 FEB)
- Hybrid of the current and future architectures
- Provide analog and digital triggers
- Planned insertion in TileCal in 2015/2016 shutdown



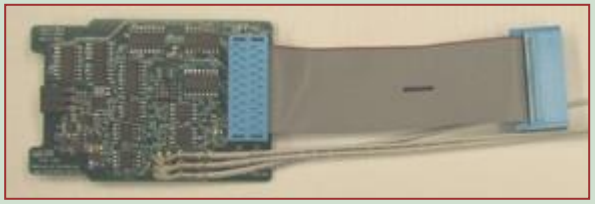


FRONT END BOARDS



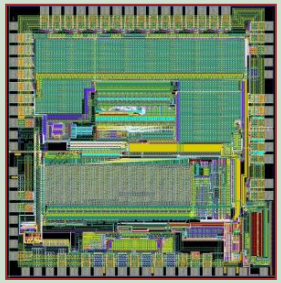
Modified 3-in-1

- Receive and shape
  - Provides analog outputs (2 gains)
  - Charge injection
  - Integrator
- Based on current 3-in-1 cards
  - Commercial off the shelf
- Improved
  - Radiation tolerance
  - Noise performance
  - Linearity performance



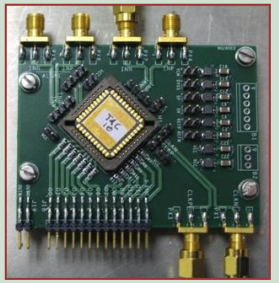
QIE ASIC

- Charge Integrator from Fermilab
- Different approach
  - Current splitter
  - Gated integrator
- Four different gains, but without shaping
  - No dead time
  - Useful for pile-up
- 17-bit dynamic range
- Clean measurement every 25 ns (40MHz)

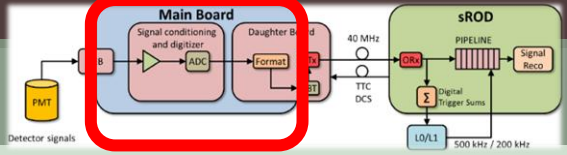


FATALIC

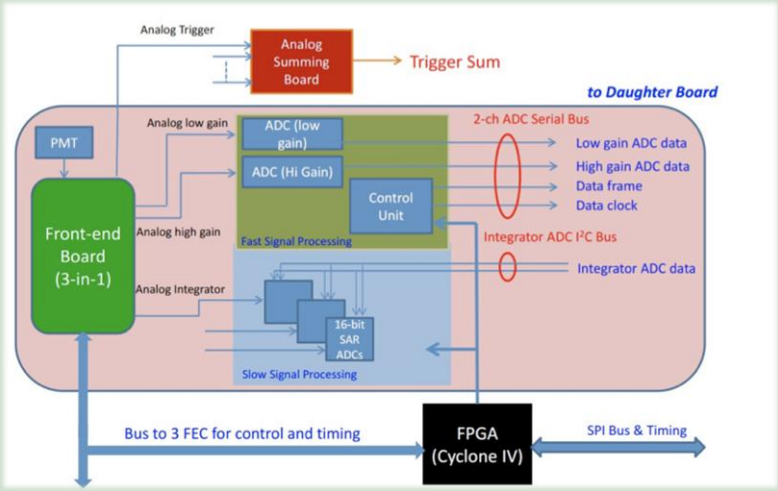
- Combines two ASIC solutions (TACTIC and FATALIC)
- FATALIC
  - Shaping stage with 3 gain ranges (1,8,64)
- TACTIC
  - 12-bit pipelined ADC
  - 40 MHz operations

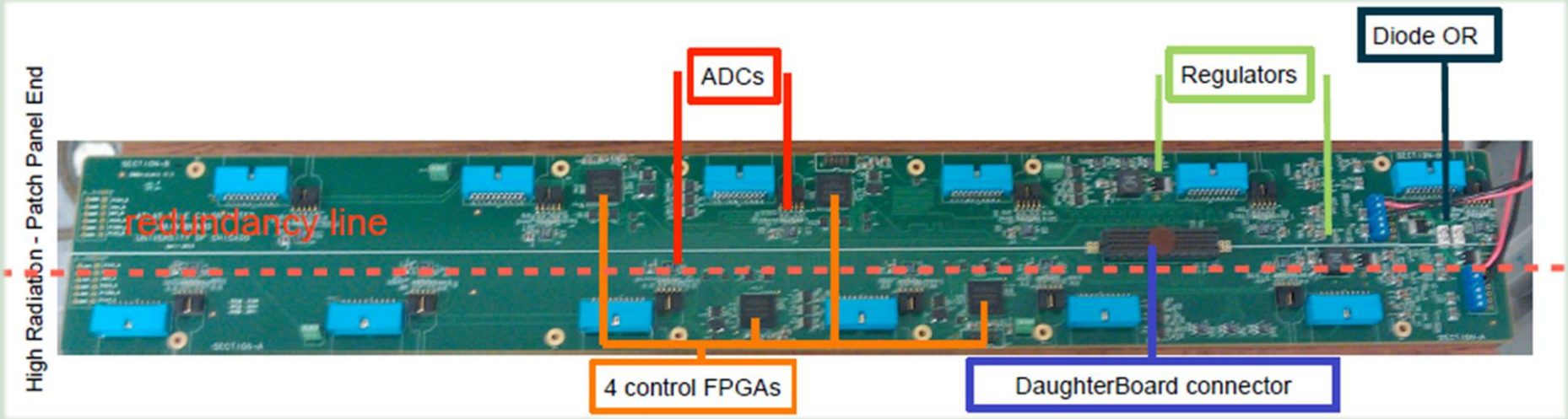


MAINBOARD

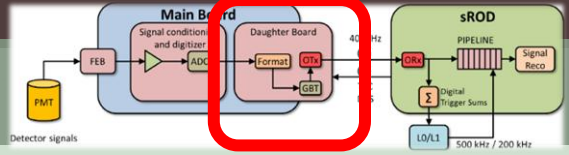


- MB-1 (Modified 3-in-1)
  - Digital control of 3-in-1 with 4 FPGAs
  - Digitization and transmission to Daughter Board via FMC connector
  - Redundant design (all levels)
- MB-2 and MB-3 (QIE & FATALIC)
  - Minor modification from MB-1
  - No ADCs needed

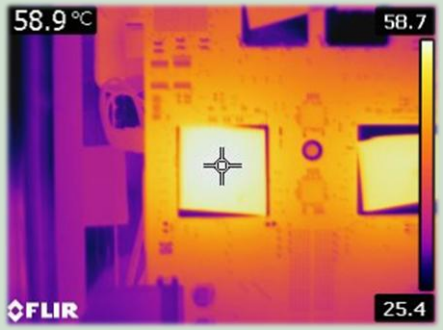


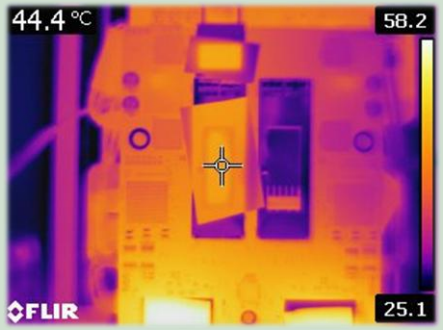


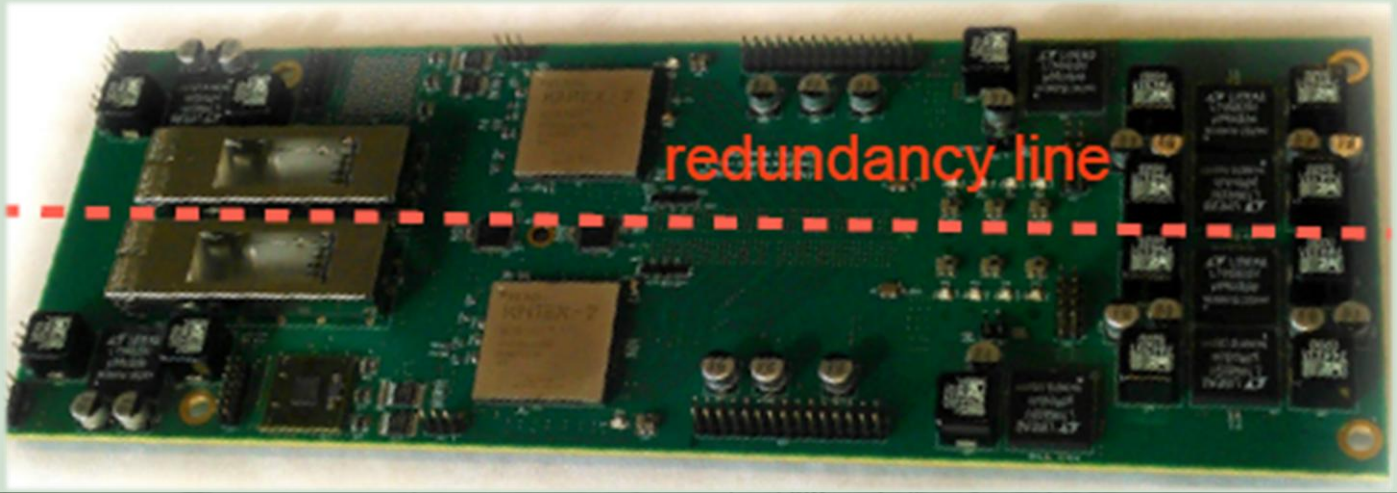
DAUGHTER BOARD



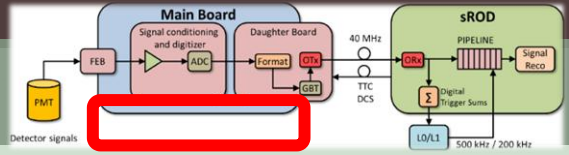
- High speed communication with back-end electronics
  - Formats and transmits read out and Detector Control System (DCS) data
  - Receives configuration and control commands from DCS
  - Configurable via optical link
- Complete two fold redundancy
- Temperature tests done



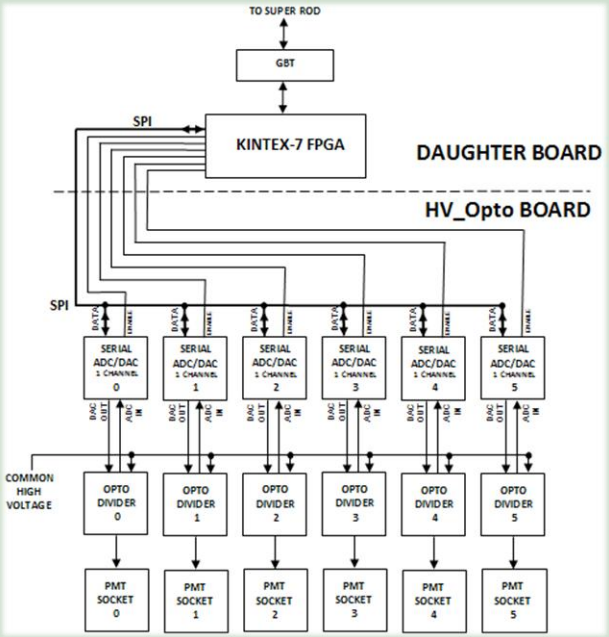


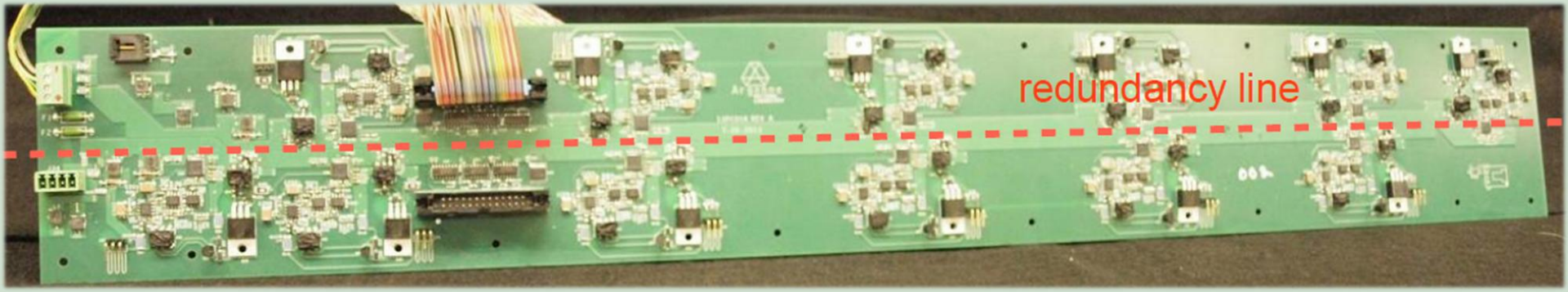


HIGH VOLTAGE BOARD

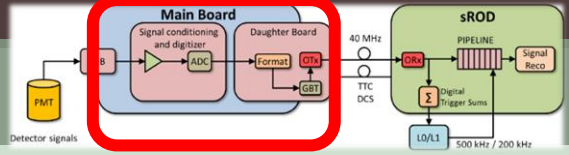


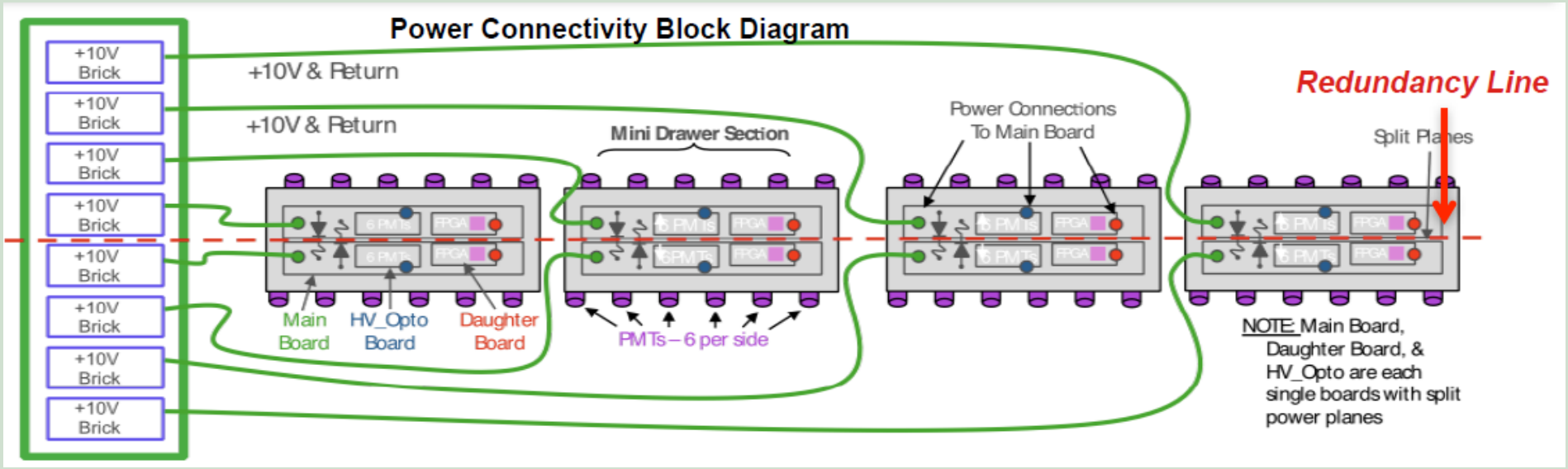
- Two solutions available
  - Local or Remote
- Local (HVOpto) chosen for demonstrator
  - Remote still under investigation for Phase-II
- HV fully controlled by daughter board
- Redundancy plane





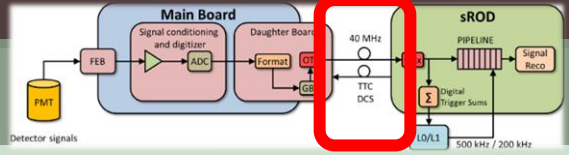
POWER DISTRIBUTION



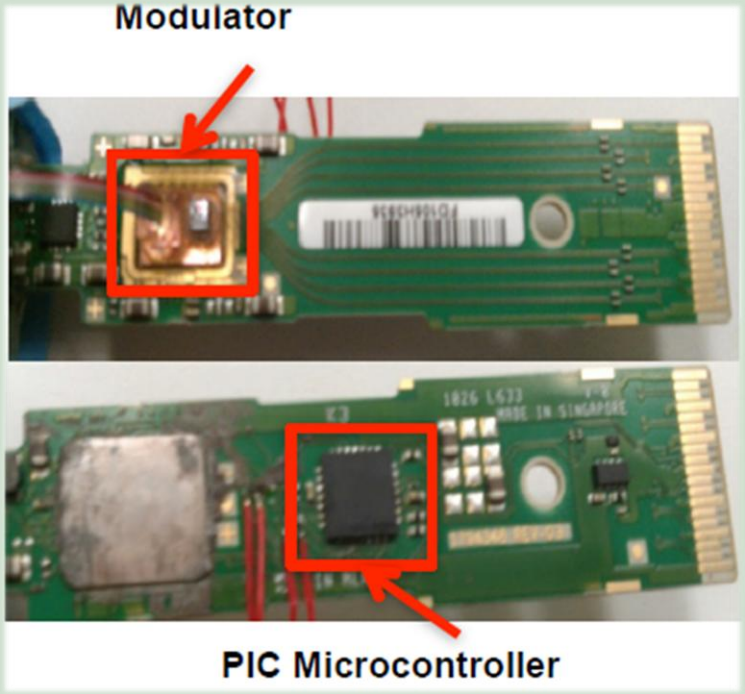


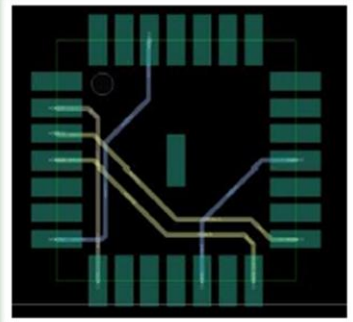
- Three stage power distribution
  - Bulk 200 V_{DC} (Off detector)
  - Low Voltage Power Supplies in front end detector
    - 8 separate units providing +10V
    - Powers half a mini-drawer but can power entire drawer if needed
  - Point of load regulators
    - Each component has dedicated power lines

OPTICAL LINKS



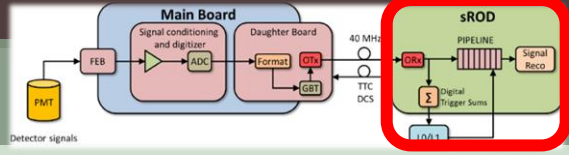
- 8 fibres per super drawer
  - (1+1) x4 mini drawer
- Two links considered:
- Vertical Cavity Surface Emitting Lasers (VCSEL)
  - Qualified at ~10 Gbps per link with error ratio ~10^{-12} which is ~900 errors / day
  - Increased bandwidth = increased problems
- Quad Small Form-factor Pluggable (QSFP+)
  - Qualified at ~40 Gbps (4X10) with error ratio of 10^{-18} which is ~1 error in 1000 days
  - PIC microcontroller used for configuration and monitoring of QSFP
  - Used in demonstrator



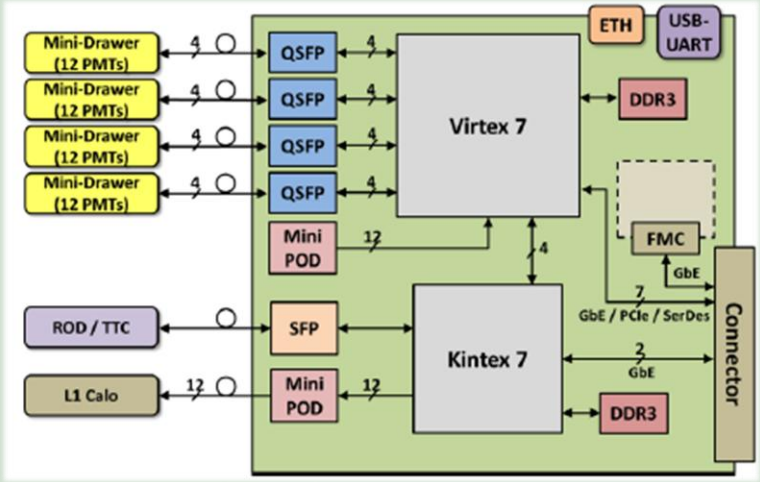


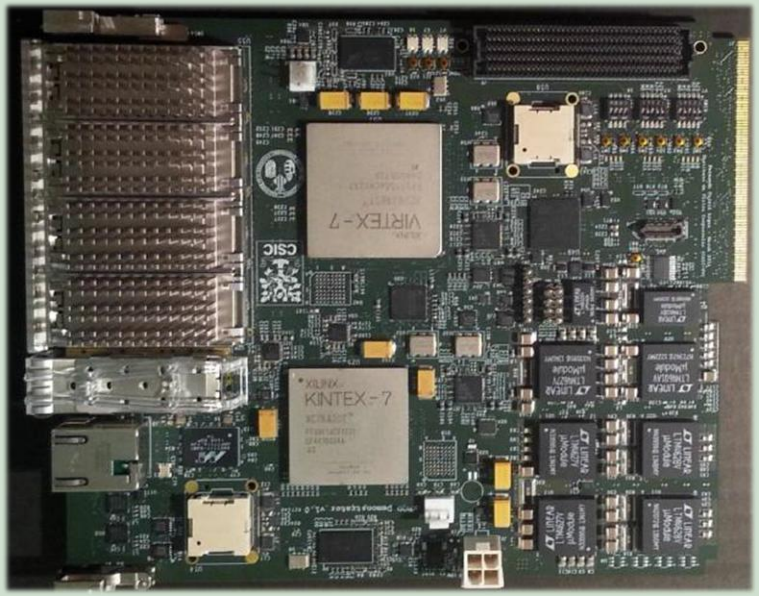
PIC Replacement Board

SROD DEMONSTRATOR



- Main interface for front-end to triggering system
  - Completely digital means better resolution
- Main functionality
  - Main data read out
  - Trigger and Timing Control distribution
  - DCS commands to front-end
- Reads out of 4 mini-drawers
- Designed for new back end infrastructure

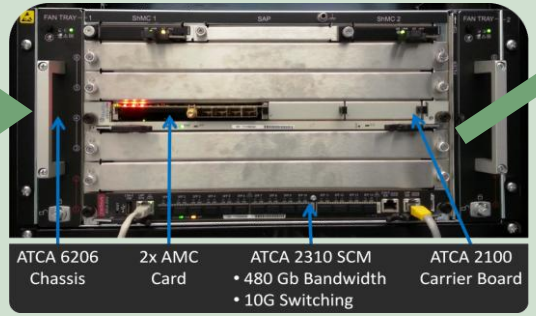




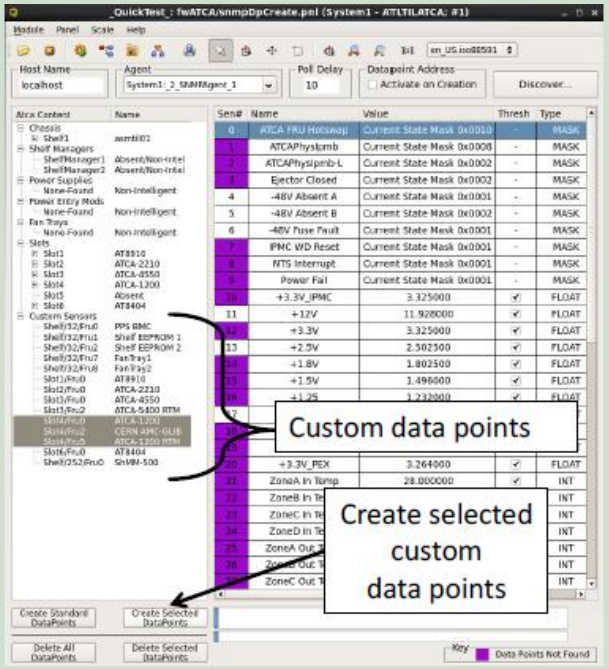
BACK END INFRASTRUCTURE

The ATCAs will house the back end electronics

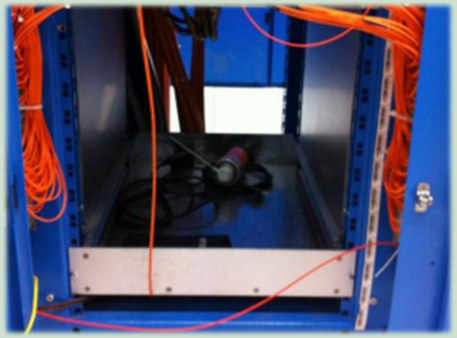
sROD



ATCA Chassis



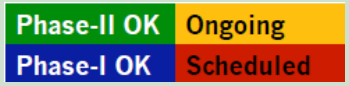
- Pioneered the integration of ATCAs into the ATLAS DCS with a new framework tool
- Control and monitor chassis and all components through Simple Network Management Protocol

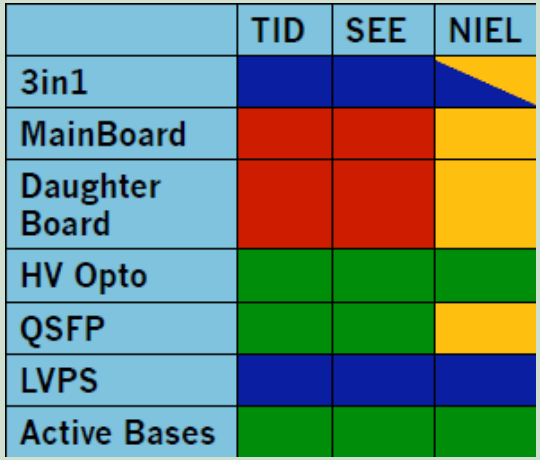


ATCA location for off detector electronics in the ATLAS cavern

RADIATION TESTS

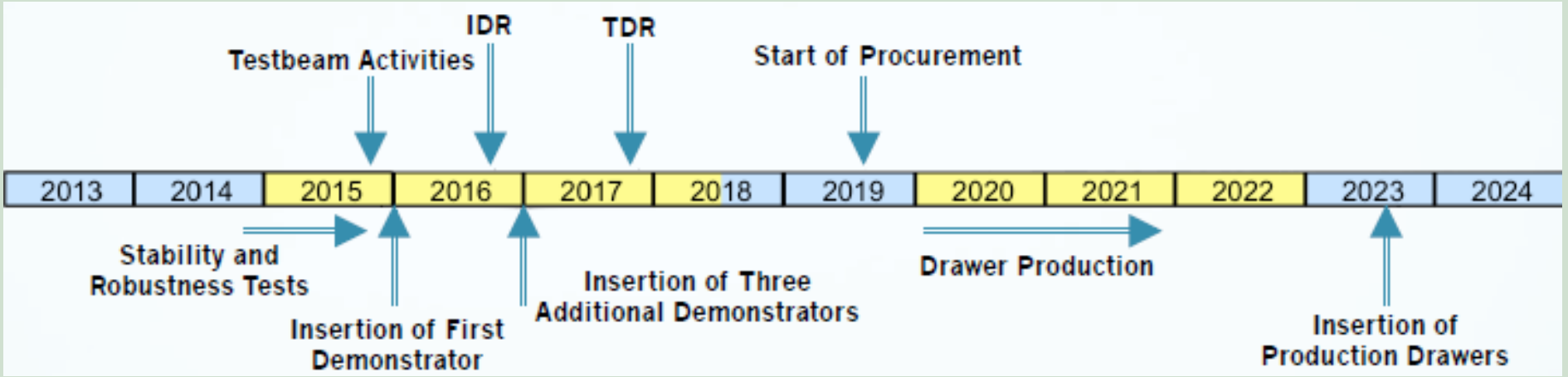
- 3-in-1
  - Sensitive analog switch replaced
- Mainboard:
  - Large number of components tested. Still need to test FPGAs
- Daughter board:
  - Internal Scrubbing and external partial reconfiguration for memory
  - Triple Mode Redundancy will catch errors in distributed memory
- HVOpto:
  - Tested for TID, SEE, NIEL (OK)
- LVPS
  - Same parts as current design
  - Must test at higher energies
- COTS Regulators
  - Tested for TID (-5V tests needed)
- QSFPs
  - Some SEUs but no failures





SUMMARY

- Upgrade of Tile Calorimeter for HL-LHC is progressing well
  - Positive ATLAS review
  - Complete redesign of the front and back end electronics
- Still some alternative solutions that will be tested
  - Extensive evaluation and system calibration in Building 175
- Test beams begin 2015 to 2016
- Early insertion scheduled for 2015/2016 in next detector opening



Questions

Robert Reed on behalf of ATLAS TileCal Community

Back Up

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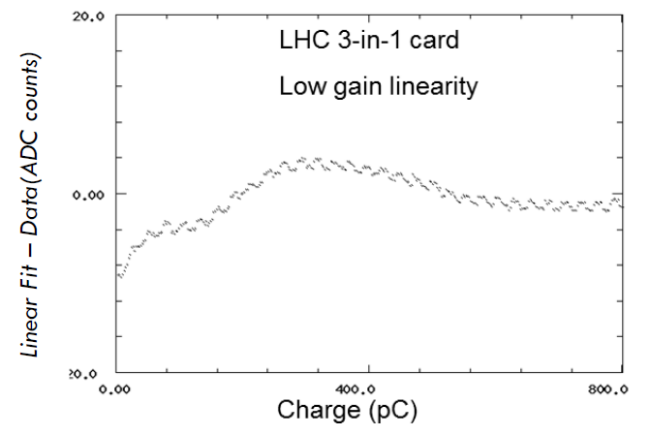
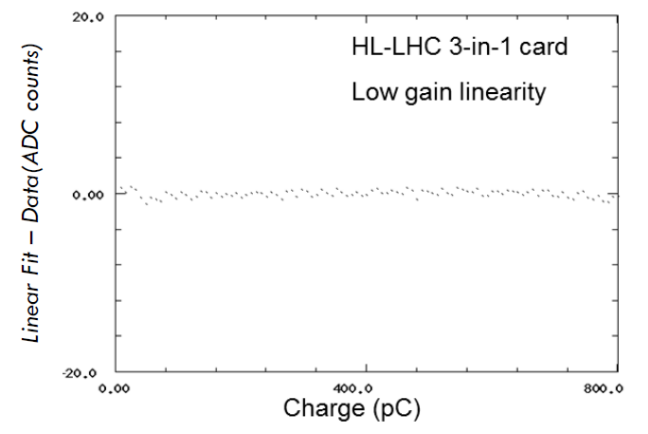
3-IN-1 RESULTS

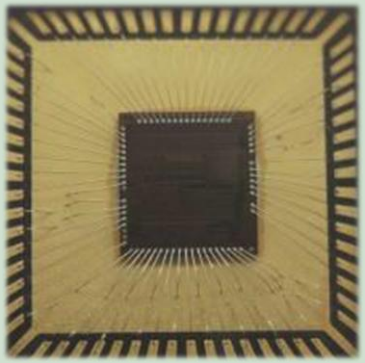
- Design based on the original 3-in-1 cards
  - Discrete COTS components
- Selected for the Demonstrator project
  - Unique option which can provide analog output to the Level-1 trigger
- Reception and shaping of PMT signals
  - Fast signal processing
    - 7 pole LC shape: 50 ns FWHM shaping time
    - Bi-gain readout: gain ratio of 16
    - Digitization in Main Boards using 12-bit ADC
  - Slow signal processing
    - Integrator to read out Cesium calibration data
  - Charge injection calibration and controls
- Better linearity and lower noise than previous version
- Status:
  - Prototype tested using COTS components
  - Passed radiation tests

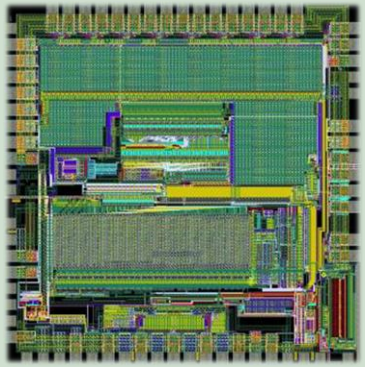


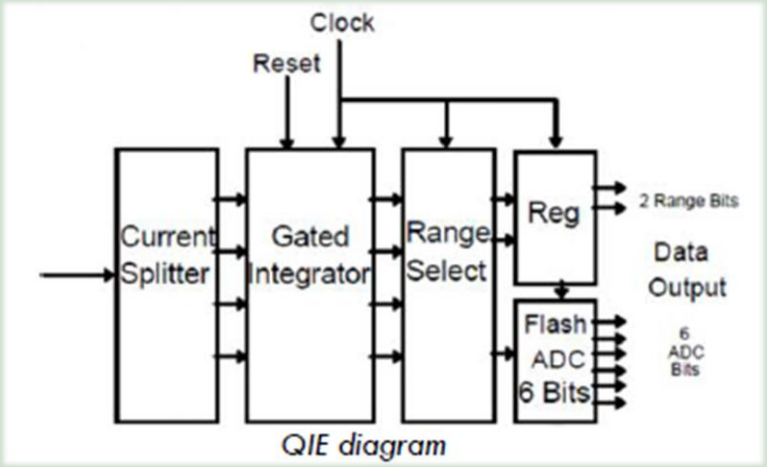


QIE

- Charge (Q) Integrator and Encoder (QIE) chip from Fermilab
- Current splitter with multiple ranges and gated integrator with on-board flash ADC
  - Needs 4 clock cycles to acquire data
  - 40 MHz operation
  - 17 bit dynamic range in 10 bits
    - 6 bit ADC value
    - 2 bit range (4 different gain ranges)
    - 2 bits CAPID
- Dead-timeless digitization
  - No pulse shaping
- Also includes
  - Charge injection for calibration
  - Integrator for calibration with source
- Status:
  - 20 chips in hand, another 40 coming
  - Passed noise, dynamic response and TDC tests
  - TID test up to 50 kRad showed good results
  - No Single Event Upsets in Shadow Register up to $6 \cdot 10^{12}$ p/cm^2



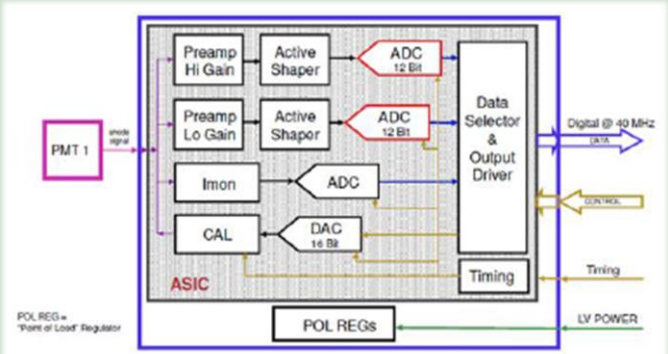




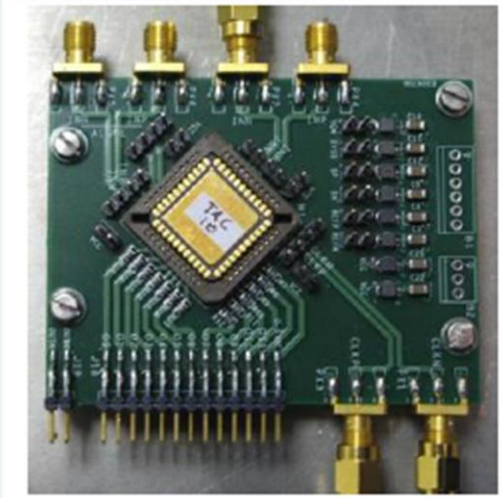
QIE diagram

FATALIC

- Combined ASIC solution: FATALIC 3 + TACTIC
  - FATALIC 4 will include both ASICs
  - IBM CMOS 130 nm technology
- FATALIC 3 main features:
  - Current conveyor
  - Shaping stage with 3 different gain ratios (1, 8, 64)
  - 80 MHz operation
- TACTIC ADC main features:
  - 12-bit pipelined ADC
  - 40 MHz operation
- Status:
  - First prototypes of FATALIC 1 and 2 validated
  - Testing FATALIC version 3
  - Designing second version of TACTIC



Conceptual Design of FE-ASIC Front-End Board


TACTIC ADC v1

ADC OPERATION TESTS

- Simple operations of FADC read-out to test alignment

A. Valero